PHONON-ENERGY-COUPLING-ENHANCEMENT EFFECT
AND ITS APPLICATIONS

ABSTRACT OF DISSERTATION

A dissertation submitted in partial fulfillment of the requirements for the degree of Doctor of Philosophy in the College of Engineering at the University of Kentucky

By

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Lexington, Kentucky

Directors: Dr. Zhi Chen, Professor of Electrical Engineering Department

Lexington, Kentucky
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ABSTRACT OF DISSERTATION

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Silicon Oxide/Oxynitride (SiO₂/SiON) has been the mainstream material used for gate dielectric for MOS transistors for the past 30 years. The aggressive scaling of the feature size of MOS transistor has limited the ability of SiO₂/SiON to work effectively as the gate dielectric to modulate the conduction of current of MOS transistors due to excess leakage current dominated by direct quantum tunneling. Due to this constraint, alternative gate dielectric/high-k is being employed to reduce the leakage current in order to maintain the rate of scaling of MOS transistors. However, the cost involved in the implementation of these new gate dielectric materials are high due to the requirements of a change in the process flow for device fabrication. This work presents the results of a novel processing method implementing the use of rapid thermal processing (RTP) on conventional SiO₂/SiON gate dielectric to reduce the gate leakage current by three to five orders of magnitude. Electrical properties of the effect were characterized on fabricated MOS capacitors using semiconductor parameter analyzer and LCR meter. Material characterization was performed using FT-IR to understand the mechanism involved in this novel processing method, named PECE (Phonon-Energy-Coupling-Enhancement). By implementing this novel process, the use of SiO₂/SiON as gate dielectric can be scaled further in conventional process flow of device fabrication.

KEYWORDS: Gate Leakage Current, Direct Tunneling Current, Silicon Oxide, Energy Coupling, FT-IR

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DISSERTATION

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This dissertation is dedicated to my father, my mentor, as well as my best friend, Mr. Ong Hoi-Sach, who provided exceptional guidance and support throughout my PhD. studies.
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CHAPTER 1
INTRODUCTION

1.1 Introduction
Since the invention of metal-oxide-semiconductor field-effect-transistor (MOSFET) in the 1960s [1], the pace of progress for MOS technology in both the R&D and industrial manufacturing sectors has exceeded most of projections that were made. The key to the significant advancement of high performance integrated circuits is the ability to reduce the active dimensions of the MOS transistors; a practice termed as “scaling” by the semiconductor industry. The advantage of scaling is an increase in both the packing density of components and speed of circuits, while reducing power dissipation [2]. This phenomenon which is broadly known as Moore’s Law was predicted by Gordon Moore, co-founder of Intel in 1965, four years after the first integrated circuit was invented [3, 4]. Although Moore’s Law is not a real physics law, it is an important standard or expectation which has been followed by the semiconductor industry for the past four decades. It says that the numbers of transistors that can be placed on an integrated circuit chip will double every two years. However, the continuous and aggressive scaling practice requires the device and materials processes to be constantly pushed to the limits. Thus, innovative device ideas and alternative process techniques are constantly needed to keep up with the projections made by the International Technology Roadmap for Semiconductors (ITRS)[5, 6].

1.2 Issues for SiO2 scaling
The success of the Microelectronic or Nanoelectronic Industry can be attributed to the existence of a stable thermal oxide of silicon, i.e., silicon dioxide (SiO2). The thin SiO2 layer that forms the gate dielectric of transistors in modern very-large-scale integrated (VLSI) circuits serves two essential purposes: Its ability to

1) Insulate the gate from the channel electrically in order for the gate electrode to induce carriers in the channel to conduct current.
2) Separate the gate from the channel physically so that the elements in the gate, such as Boron in P+ polysilicon gate will not diffuse into the channel and change its electrical properties.

In addition, the ability of silicon to form SiO₂ at a relatively low cost has enabled silicon to dominate the semiconductor industry among many other semiconductor materials such as Ge, GaAs, InP etc. As shown in Table 1.1[7], silicon dioxide (SiO₂) also uniquely possesses outstanding properties such as high resistivity, excellent dielectric strength, high melting point, a large band gap, and low defect density at the Si/SiO₂ interface. These outstanding properties present significant advantages over any other alternative gate dielectric candidates.

The performance of logic devices (MOSFETS) are associated with their drive current. The drive current (drain current) using gradual channel approximation can be written as [8]:

\[
I_{D,\text{sat}} = \frac{W}{L} \mu C_{ox} \left( V_G - V_T \right)^2 \frac{V_{CL}}{2}
\]

Thus, a reduction in the channel length or an increase in the gate dielectric capacitance would result in an increase the drive current, \( I_{D,\text{sat}} \). Since the gate dielectric capacitance could be modeled as a parallel plate capacitor, the reduction of the gate dielectric thickness would conversely increase the drive current of a MOS transistor. Ignoring quantum mechanical and depletion effects in the Si substrate and gate, the oxide capacitance can be expressed by:

\[
C_{ox} = \frac{k \varepsilon_0 A}{t_{ox}}
\]

where \( k, \varepsilon_0, t_{ox}, \) and \( A \) are relative dielectric constant (3.9 for SiO₂), vacuum dielectric constant (8.854×10⁻¹⁴ F/cm), oxide thickness, and area of the capacitor respectively.
Thinning the oxide dielectric used to be a simple and effective way to obtain high capacitance values, as SiO$_2$ is highly stable on Si as mentioned earlier. However, there is a physical and practical limit to how thin the oxide film can be made. In the past four decades, SiO$_2$ has decreased in thickness from hundreds of nanometers to less than 1.2 nm used currently. This leads to several limitations and issues for ultra thin SiO$_2$ such as high gate leakage current, reduced drive current, reliability degradation, and enhanced Boron penetration.

The most significant issue of ultra thin SiO$_2$ is the gate leakage current, which causes an increase in power consumption and will subsequently lead to device malfunction. The leakage current through oxide is due to quantum-mechanical tunneling, either Fowler-Nordheim (FN) tunneling [9], or direct tunneling for an oxide thickness less than 3 nm. Fowler-Nordheim tunneling can be approximated as electron tunneling through triangular energy barrier, whereas direct tunneling current can be approximated as electron tunneling through a trapezoidal barrier. The dominant leakage current for ultra thin oxide (< 3 nm), however is the direct tunneling current. Figure 1.1 shows the schematic band diagram explaining the direct tunneling mechanism. In the case of thick oxides, the oxide acts as an insulator, functioning as a barrier for carriers. Thus, leakage current remains low. In case of thin insulator, however, the quantum effect can not be neglected and carriers can pass through the insulator directly. As shown in Figure 1.2 based on the simulation modeled by Lo et al. [10], the gate leakage current increases by one order of magnitude for each 0.2 nm decrease of the oxide thickness.

It is also interesting to note that the drive current decreases below a certain thickness of SiO$_2$, as reported by Timp et al. [11]. As shown in Figure 1.3, at oxide thickness below 13Å, the drain current decreases, resulting in no advantages in performance (drive current) [12]. Theoretical simulation by Fischetti et al. [13] using Monte Carlo-Poisson and quantum mechanical models (based on electron scattering from gate-oxide interface plasmons) demonstrated that excitation and adsorption of plasma modes in the gate region result in net loss of momentum for carries in the channel. The enhanced scattering of electrons lowered the mobility in the inversion layer of the ultra-thin oxide because of
extreme carrier confinement. This leads to a decrease of electron velocity, which subsequently reduced the drain current/device performance.

1.3 High-k gate dielectric

The basis for functioning of MOS transistors is the ability of the gate to modulate the current in the channel by electric field through the dielectric (SiO₂) to act as a switch. However, the continuous scaling required for improving performance of transistors has reduced the thickness of the gate dielectric to a point where SiO₂ is no longer able to work effectively as an insulator, i.e., leakage current through the SiO₂ due to quantum tunneling effects. In the semiconductor industry one solution is to identify a replacement material where the gate insulator would be thick enough to keep electrons from tunneling through it while allowing the gate’s dielectric field into the channel to modulate the conduction of current. Thus, the material has to be physically thick but electrically thin. High permittivity (high-k) dielectric material satisfies the above requirement. The phrase “Equivalent Oxide Thickness” (EOT) refers then to the ratio of the dielectric constant (εₖ) of an alternative (or high-k) material over that of SiO₂ as shown in equation (1.3):

\[
EOT = \frac{\varepsilon_{\text{oxide}}}{\varepsilon_k} t_k
\]

where \(EOT\), \(t_k\), \(\varepsilon_{\text{oxide}}\), and \(\varepsilon_k\) are equivalent oxide thickness, physical thickness of alternative gate material, dielectric constant of oxide (3.9), and dielectric constant of alternative gate material respectively.

The term “high-k” refers to a material with a higher dielectric constant as compared to SiO₂. A higher dielectric constant means that the insulator can provide an increase of capacitance for the same thickness of an insulator with a lower k value. The k value relates to the ability of materials to polarize. As shown in Figure 1.4, an insulator with a higher k value provides the same charge despite being thicker physically. There are a wide variety of films with higher k values than SiO₂, ranging from Si₃N₄ with a k value of 7, up to Pb-La-Ti (PLT) with a k value of 1,400. It is, however, not simple to replace SiO₂ with a high-k material, because a high-k dielectric must satisfy several conditions which deter-
mine the electrical properties of MOSFET.

A systematic consideration of the required properties of gate dielectrics stresses the following guidelines for selecting an alternative gate dielectric [14].

1) **Permittivity, band gap, and band alignment to silicon**

As mentioned earlier, higher dielectric constant enables the gate insulator to be made physically thicker for the same capacitance value. However, the band gap which determines the barrier height (against electron and hole tunneling) is roughly inversely proportional to the dielectric constant. It is therefore necessary to have a high-k dielectric with a reasonable band gap in order to suppress the leakage currents due to Schottky emission and quantum tunneling.

2) **Thermodynamic stability on silicon**

High temperature wafer processing, such as thermal activation of dopant impurities, is part of the process flow of VLSI fabrication. In such a thermal process, a dielectric material such as SiO₂ or a high-k dielectric material, must be thermodynamically stable on silicon. In addition, silicide formation, MₓSiₙ should not occur during these high temperature processes. A conductive path across the channel, which essentially creates a short between source and drain would occur, if silicides were formed. These interfacial oxide layers which form series capacitances with the gate dielectric decrease the total capacitance of the gate dielectric material. As shown in equation (1.4), the equivalent oxide thickness (EOT) of the gate-stack dielectric would never be less than the value of the lower-k material (SiO₂). Therefore, much of the expected increase in the gate capacitance associated with high-k dielectric material is compromised.

\[
EOT = t_{SiO_2} + \left( \frac{k_{SiO_2}}{k_{highk}} \right) * t_{highk}
\]  

(1.4)

Furthermore, micro-crystal growth in the films may also occur during the thermal process and must be prevented because the micro-crystals act as a conduction path, which increases the gate leakage current tremendously.
3) Low density of interface traps (interface quality)

Mobility is one of the most important factors in properties of MOSFET because it directly affects the drain current (drive performance). The key to obtain high mobility is the quality of the gate insulator. It is considered that carrier mobility is degraded by the carrier scattering effect caused by defects in the gate insulator such as fixed charges and interface trap density. The fixed charges cause a shift in the flat-band voltage ($V_{FB}$), and higher density of interface traps induces Coulomb scattering.

In addition to the requirements mentioned earlier, high-k materials must also be compatible with current materials and processes used in CMOS device processing, as well as having excellent electrical reliability characteristics. These strict and stringent requirements impose critical challenges to enable implementation of a high-k material as gate dielectric. In addition, the use of high-k dielectric requires the need for metal gates and will be discussed in the next section.

1.4 Metal Gate Electrodes

The need for metal gate electrodes arises from the limitations of present polysilicon (poly-Si) gate technology. Some of the limitations of the poly-Si gates are high sheet resistance, dopant penetration, and poly-Si depletion. Sheet resistance of poly-Si is much higher than of metals. Low contact resistance is required for state-of-the-art high speed CMOS operation, in which case metal gates are required. In addition, poly-Si has to be externally doped with impurities (dopants) to define the source and drain regions. During the doping thermal cycle, it is difficult to avoid penetration of dopants, especially boron in the pMOS transistor, through the thin gate dielectric. The dopant penetration leads to adverse effects on the device's threshold voltage. Modern CMOS processing require the use of n+ poly-Si gates for NMOS and p+ poly-Si gates for PMOS, and this is normally accomplished by ion implantation and subsequent annealing. However, ultra shallow junctions are required for deep sub-micron devices. Thus, the energy of implantation and the dopant activation temperature have been reduced substantially for ultra shallow junctions. This results in lower doping of the poly-Si gate, especially at the oxide-Poly Si interface. The reduction in dopants at the interface of oxide and poly-Si leads to a depletion
layer in the gate and an increase of the effective oxide thickness (EOT), which would consequently increase the threshold voltage and decrease the transconductance [15]. These disadvantages of poly-Si as gate electrodes directly translate into a decrease in the drive current, which is why metal gate electrodes are required for advanced MOS transistor structures. In addition, poly-Si depletion becomes more severe as the effective dielectric thickness is scaled down.

Replacing polysilicon gate electrodes with metal gate electrodes however, imposes serious manufacturing and reliability challenges. Thermal/chemical stability and process compatibility with high-k dielectrics as well as compatibility with the current CMOS processing is required. Dual metal gate electrodes should have appropriate metal work functions for NMOS and for PMOS. For conventional device operation, the optimum work functions should be made within 0.2 eV of the conduction and valance band edges of Si [16].

1.5 Motivations and Research Objectives

1.5.1 Background

Despite the challenges required for replacing SiO₂ with an alternative gate dielectric material, and the need to use metal gates as the gate electrodes, the semiconductor industry has shown the adversity and the resilience to overcome these obstacles to keep up with the ITRS projections. The change to alternative gate dielectric from SiO₂ began with the implementation of lightly nitrided oxides for logic devices as the gate thickness scaled below 2.2 nm at the 180 nm node. The addition of nitrogen to SiO₂ greatly reduces boron diffusion from the p+ poly layer through the silicon oxynitride (SiON) dielectric layer. Thus, the Boron penetration issues (which causes threshold voltage shift and degrade reliability in ultra-thin SiO₂ layer) are essentially eliminated by using SiON dielectric [17-19]. As shown in Figure 1.5, heavy doping with nitrogen increases the k value toward Si₃N₄ (k = 7.8) and thus reduces gate leakage current [20]. Heavily nitrogen-doped oxynitrdes (SiON) were later used through the 90nm node formed by either thermal nitridation (TN-O) or plasma nitridation (PN-O) of the SiO₂ oxide layer with nitrogen compositional
engineering up to a few percent [21-26]. The use of SiON however, suffers from the fact that the highest permittivity, or $k$ value obtainable is only twice the value ($k = 7.8$) of pure SiO$_2$. According to the ITRS projection in 2005 [5], the use of high-$k$ dielectric material is required beyond 2008, as shown in Figure 1.6. At the cross over the simulated leakage current density ($J_{g\text{ sim}}$) and leakage current density limit ($J_{g\text{ limit}}$), SiON gate dielectric is incapable of meeting the gate leakage current limit beyond 2008.

Numerous research work toward implementing high-$k$ materials was conducted in the late 1990’s when people realized that SiO$_2$ would be incapable of meeting the post 2008 requirement of oxide scaling. Various research work was then pursued aggressively on high-$k$ dielectric candidates such as aluminum oxide (Al$_2$O$_3$), titanium dioxide (TiO$_2$), hafnium dioxide (HfO$_2$), zirconium oxide (ZrO$_2$), zirconium silicate (ZrSiO$_4$), and lanthanum oxide (La$_2$O$_3$). A comprehensive review paper on the high-$k$ materials can be found from G.D Wilk et al. [14] and J-P. Locquet et al.[27].

The schematic diagram shown in Figure 1.7 reviews the common high-$k$ dielectric candidates. Based on this diagram, it can be seen that Hf and Zr based dielectrics are the most likely and promising candidates for high-$k$ dielectric material as these materials showed more stable electrical characteristics. However, Hf-based dielectric was chosen by most researchers as the likely candidate due to its higher $k$ value compared to Zr-based dielectrics. The complete change of the gate dielectric material to high-$k$ (Hf-based dielectric) and metal gate electrodes (different metal gates for NMOS and PMOS) was demonstrated and implemented successfully at the 45nm process node by Intel [28].

The implementation of high-$k$ plus metal gate transistors was an important breakthrough in the logic technology as this was one of the biggest change to the process flow of integrated circuit fabrication. However, it has not been demonstrated that the high-$k$ plus metal gate device could be scaled beyond the 32 nm process node. In addition, there are several questions and problems that remained to be solved.
1.5.2 Motivation

Precise thickness control and good surface morphology is required in the deposition of high-k materials. Previously, reactive sputtering and metal organic chemical vapor deposition (MOCVD) were used to make the dielectric layer. However, the dielectric layer that was produced contains gaps that could trap charges in the high-k layer. This problem could be solved using atomic layer deposition (ALD), in which the dielectric is build up one layer at a time. In spite of that, good starting surface chemistry is significant for both the thickness of the lower interface and the quality of the starting materials for deposition of ultra thin high-k films [29]. It has been reported that ALD of HfO$_2$ showed unacceptable defects below ~3.0nm physical thickness due to the growth behavior during the ALD process [30]. Chemical oxides have proven to be a able to provide a robust starting surface for high-k materials as well as providing low interface traps down to 0.4nm [31]. In addition, an interfacial layer of SiO$_2$ has also proven to reduce mobility degradation of high-k due to coupling of low energy Surface Optical (SO) phonon modes. The SO phonon modes arise from the polarization of the high-k material to the inversion channel charge carriers [13]. Thus, an interfacial layer of SiO$_2$ is beneficial to enable a high drive performance of CMOS transistors and is desirable as a good starting surface for ALD deposition of the high-k material.

It has been reported that diffusion of oxygen through HfO$_2$ is a fast and reactive process [32]. Oxygen which diffuses through HfO$_2$ will react with Si at the interface and forms an interfacial layer. Even under optimized processing conditions, it was reported that the contribution from the interfacial layer is around 5Å [33, 34]. Thus, the interfacial oxide layer, which is not only unavoidable during growth/deposition/annealing of the high-k material but is also required, will increase the EOT of the dielectric material as described in Equation (1.5) below:

$$EOT = T_{\text{interfacial oxide}} + T_{\text{high k}} \frac{3.9 \varepsilon_{\text{high k}}}{\varepsilon_{\text{high k}}}$$

(1.5)

This interfacial oxide layer can dominate gate-leakage degradation as EOT is scaled below 1.2nm for these Hf-based oxides. For an EOT of 1.0 nm (which is required for process node beyond 32 nm), and with an interfacial oxide of 0.6 nm, the physical thick-
ness of the high-k layer assuming a $k$ value of 26 (pure HfO$_2$), is only 2.6 nm. The assumption of using pure HfO$_2$ is an overestimate since pure HfO$_2$ is not thermodynamically stable at high processing temperature and tends to crystallize at processing temperatures above 700 ºC [35, 36]. Thus, if we were to assume a reasonable $k$ value of around 10 (HfSiON), the physical thickness of the high-k layer is only 1 nm. This will require extremely thin high $k$ films with excellent composition control.

Implementing Hf-based material requires the changing of the conventional process flow of transistor fabrication from the *gate-first* approach, (where the dielectric material is deposited first) to *gate-last* approach (where the dielectric material is deposited in the last steps) in order to circumvent the thermal annealing requirements after the source and drain are formed. The change of the process flow is challenging and increases the production cost. Although Intel has demonstrated the implementation of *gate-last* approach, not many semiconductor companies are quickly adopting this new approach due to cost issues.

In view of these constraints imposed on implementing high-k dielectric material to the process flow of transistor fabrication, this work will focus on a novel method to reduce the gate leakage current in order to continue to extend the use of SiO$_2$/SiON as the dielectric material for transistor fabrication. The main thrust of this work is to investigate and understand the principles behind a phenomenon dubbed “Phonon-Energy-Coupling-Enhancement” effect, in which reduction of tunneling current on SiO$_2$/SiON by several orders of magnitude was observed [37, 38]. Even if high-k dielectric materials were to be used on all transistor fabrication, the interfacial oxide (~0.5 nm), which is required for high-k materials, can be improved using the PECE effect to further reduce the leakage current of the dielectric stack. As shown in Figure 1.8, the leakage current reduction of the state-of-the art high-$k$ plus metal gate structure developed by Intel [28] showed a reduction of only 25x for NMOS and 1000x for PMOS as compared to conventional SiON/Poly-Gate structure of a 65 nm transistor with the same EOT [39]. The PECE effect work performed on SiO$_2$/SiON devices was shown to reliably obtain leakage current reduction up to 5 orders of magnitude. Thus, the high-$k$ plus metal gate approach may
not be needed because a conventional SiO₂ dielectric material with the PECE effect can achieve similar or even better leakage current reduction than high-k materials. The huge benefit of using conventional SiO₂ with the PECE-induced leakage reduction is its low cost for implementation in CMOS processing. Another advantage is that the PECE effect may help scaling SiO₂ down to below 0.5 nm, which can not be achieved by high-k materials because of the 0.5 nm interfacial oxide. It should also be noted that research-based transistors with 0.8 nm (physical thickness) of SiO₂ have been demonstrated to work [40].

1.6 Overview of Dissertation

This dissertation will focus on understanding the principles of the PECE effect as well as its applications on semiconductor devices, particularly on reducing the gate tunneling current of ultra thin SiO₂ and SiON.

Chapter 1 provides the basic introduction of the issues related to scaling on CMOS devices, as well as the implication of scaling on conventional SiO₂ dielectric layer, and the need for alternative gate dielectrics, and its requirements. The motivation and research objectives for this work are also discussed.

Chapter 2 provides the introduction of the experimental work conducted that led to the discovery of PECE effect. Leakage current reduction due to RTP-induced PECE effects on SiON dielectric MOS capacitors are also characterized.

Chapter 3 provides experimental setup, RCA clean, oxidation, thickness measurement via Capacitance-Voltage, RTP setup for trace O₂ and trace moisture experiments as well as temperature measurement for the RTP chamber.

Chapter 4 provides the FT-IR studies of the process parameters needed to generate PECE effects by characterizing the absorption intensity of the Si-O rocking modes.

Chapter 5 provides the processes, materials consideration, and fabrication procedures to
observe the PECE effect reliably on MOS capacitors.

Chapter 6 discusses the PECE effect on Si-Si bonds and the implication of breakdown voltage on PN junction diodes.

Chapter 7 discusses the PECE work performed on ultra thin SiO$_2$/SiON on gate leakage reduction. Varying RTP annealing conditions were investigated such as pure N$_2$ ambient, low-level moisture ambient, and trace O$_2$ ambient.

Chapter 8 concludes the research work with focus on future directions of the research on PECE effects.
Table 1.1: Properties of SiO$_2$ [7]

<table>
<thead>
<tr>
<th>Properties</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dielectric strength</td>
<td>$\sim$10 MV/cm</td>
</tr>
<tr>
<td>Dielectric constant</td>
<td>$\sim$3.9</td>
</tr>
<tr>
<td>Interfacial defect density</td>
<td>$\sim$10$^{10}$ eV$^{-1}$cm$^{-2}$</td>
</tr>
<tr>
<td>Melting point</td>
<td>1713 °C</td>
</tr>
<tr>
<td>Energy gap</td>
<td>$\sim$9 eV</td>
</tr>
<tr>
<td>Resistivity</td>
<td>$\sim$10$^{15}$ Ω-cm</td>
</tr>
<tr>
<td>Density</td>
<td>2.27 g/cm$^3$</td>
</tr>
<tr>
<td>Bulk Refractive Index</td>
<td>1.46</td>
</tr>
</tbody>
</table>
Figure 1.1  Direct Tunneling Mechanism of Ultra thin SiO$_2$
Figure 1.2 Measured and simulated $J_G$-$V_G$ tunneling currents for silicon oxide thicknesses ranging from 3.6 to 1.0 nm [10]
Figure 1.3  Drive current vs. gate leakage for a) $L_g = 140$ nm, and b) $L_g = 70$ nm. The drive current measurements were obtained at $V_D = V_G = 1.5$ V, whereas the leakage current measurement was measured at $V_G = 1.5$ V and $V_D = 0$ V [12]
Figure 1.4  Schematic illustration of the concept of different values of k (dielectric constant). A higher k value as shown in the figure on the right enables the material to provide the same charge with a thicker material.
Figure 1.5 Influence of Nitrogen on leakage current of dielectric film [20]
Figure 1.6  Simulated Gate Leakage ($J_{g_{\text{sim}}}$) versus Gate Leakage Current Density ($J_{g_{\text{limit}}}$) due to direct tunneling for high-performance logic [5]
Figure 1.7 Review of High-k dielectric candidates. ZrO$_2$ and HfO$_2$ exhibit the most promising candidates for alternative high-k dielectric [27].
Figure 1.8 Comparison of leakage current reduction of Intel’s High-k + Metal Gate transistor [28]. The leakage current reduction of 25 X for NMOS and 1000 X for PMOS is observed as compared to SiON/Poly transistor of 65 nm process node [39]
CHAPTER 2
PHONON-ENERGY COUPLING ENHANCEMENT EFFECT

2.1 Introduction
Chapter 2 presents the experimental work that led to the discovery of the Phonon-Energy-Coupling-Enhancement (PECE) Effect. Discovery of the PECE Effect was the subsequent consequence of studying the mechanism behind the hot carrier-induced degradation in metal oxide semiconductor (MOS) transistors, specifically the hydrogen/deuterium (H/D) isotope effect. Fourier-Transform-Infrared (FTIR) spectroscopy (based on infrared spectroscopy) is a useful analytical tool to study the vibrational modes of SiO₂/Si interfaces. The FT-IR experiments were conducted to prove Van de Walle’s theory on H/D isotope effect (based on bond energy de-excitation) provided the groundwork on PECE effect studies as described in detail in section 2.4 [41].

2.2 Theoretical Background: Hydrogen/Deuterium Isotope Effect
Hot electron induced device degradation has been one of the most researched topics in semiconductor reliability for the past 30 years [42]. As device dimensions are scaled down to achieve higher performance, unwanted side effects (short channel effects) arise due to the higher electric field in the channel. The drain current in the channel ionizes the carriers, which attain a larger energy level than the thermal energy in equilibrium. These carriers, which are termed as hot carriers, are energetic charge carriers that achieve ballistic transport in the channel and acquire an exceedingly high velocity. Even though these carriers could increase the speed of MOS transistors, the hot carriers could also have adverse effects on the reliability of transistors specifically on the increase of dangling bonds at the silicon/silicon oxide interface. Increase in dangling bonds, which are also referred to as surface states or interfacial traps, degrades MOS transistors during transistor operation. Interfacial traps arise from unsatisfied chemical bonds that occur at the Si/SiO₂ interface and could traps charge, thus the name interfacial traps. In order to minimize interfacial traps, hydrogen passivation through Post-Metal-Annealing (PMA) in hydrogen ambient is a common technique to minimize the presence of dangling bonds
present at the Si/SiO₂ interface. However, these Si-H bonds are not stable, and can be broken by energetic hot carriers in the channel as mentioned earlier.

An alternative annealing process of using deuterium instead of hydrogen was proposed by Lyding et al. [43] to passivate the dangling bonds at the Si/SiO₂ interface. This was inspired partly by Lyding’s previous works on the hydrogen passivation of the dangling bonds on Si (100):2x1 surfaces under ultra high vacuum conditions. It was demonstrated that desorption of hydrogen from the Si surface can be achieved by irradiation with electrons emitted from a scanning tunneling microscope (STM) tip [44, 45]. Avouris et al. [46] also studied the STM-induced desorption from Si (100):2x1 experiments with deuterium, where the isotope effect was observed. It was found that deuterium was harder to be removed in comparison with hydrogen (up to two orders of magnitude). Based on these STM experiments, Lyding et al. studied the isotope effect of hot-electron degradation in MOS transistors to compare the degradation effect after hydrogen annealing and deuterium annealing. Results similar to the STM desorption experiments were also achieved in these hot-electron degradation experiments, where Si-D bonds showed more resistance to hot electron degradation compared to Si-H bonds. The lifetime of transistors annealed in deuterium was also found to be 10-50 times longer compared to transistors annealed in hydrogen [43]. The theoretical explanation provided was that the isotope effect was due to the larger mass of deuterium as compared to that of hydrogen. Thus, more energy is required to remove/disassociate deuterium from the Si/SiO₂ interface. This led to enthusiasm among researchers to investigate further the use of deuterium instead of hydrogen as surface passivation and the implementation in the process flow of integrated circuit manufacturing [47-51]

Van de Walle et al. however, disagreed with the mass theory and proposed an alternative theory for the H/D isotope effect, which states that the isotope effect is caused by two competing processes [52]:

1) The vibrational energy of bonds is accumulated through multiple vibrational excitation by energetic hot electrons in the low voltage regime [53]. The electrons excite Si-H/D bonds so that vibrational energy of the bonds is increased to a point where the
bonds are broken.

2) There is a de-excitation (quenching) process, where the vibrational energy of the Si-D bond is reduced by energy coupling from the Si-D bonds to substrate phonons (Si-Si TO phonon mode).

The de-excitation process is the reason why Si-D bonds are stronger and harder to dissociate compared to Si-H bonds. This is because the vibrational frequency of the Si-H bond (Si-H bending mode at 650 cm\(^{-1}\)) is far away from the Si-Si TO phonon mode (463 cm\(^{-1}\)) as compared to Si-D vibrational frequency (Si-D bending mode at 460 cm\(^{-1}\)). The extent to which the vibrational energy stored in Si-H/Si-D bonds excited by electrons depends upon the vibrational lifetime, which is the rate at which energy is lost by coupling to phonons. Thus, bonds with larger vibrational lifetimes are more susceptible to bond breakage due to efficient vibrational excitation. Since there is no energy coupling between Si-H bonds and the Si substrate phonons, this makes the Si-H bonds more vulnerable to hot electron excitation compared to Si-D bonds. Experimental works by Avouris et al. [46] showed that vibrational lifetime of Si-H was indeed larger than that of Si-D, which is apparently caused by energy coupling. This leads to a more robust Si-D bonds compared to Si-H bonds.

2.3 Evidence for energy coupling from the Si-D vibration mode to the Si-Si and Si-O vibration modes at the SiO\(_2\)-Si interface [54]

Van de Walle’s theory of vibrational energy de-excitation by energy coupling from Si-D bonds to Si-Si bulk phonons were based on theoretical calculations. The experimental data of vibrational frequencies of Si-H and Si-D bending modes were obtained from amorphous Si (\(\alpha\)-Si) films [55, 56]. This was also confirmed by Wei et al. [57] in their work on light-induced photoconductivity degradation of deuterated and hydrogenated \(\alpha\)-Si, where it was found that deuterated \(\alpha\)-Si was more stable under light exposure. However, the chemical environment of Si-H/D bonds in \(\alpha\)-Si is very different from that in the SiO\(_2\) film on a single crystal silicon substrate. In order to verify Van de Walle’s theory, measurements of the vibrational frequency of the Si-D/Si-H bonds in a conventional MOS structure based on SiO\(_2\) film on a single crystal silicon substrate would be needed.
This would provide a clear understanding of the fundamental mechanism of isotope effects on hot electron degradation in MOS transistors. Vibrational frequencies of Si-H/D and Si-Si bonds were measured using Fourier-Transform-Infrared (FT-IR) spectrometer.

The samples used in the FT-IR experiments were 2 inch, N(100) orientation silicon wafers. High doping density wafer (ρ = 0.001 Ω-cm, N_d ~ 10^{19} cm^{-3}) were used in order to mimic the high density of electrons that are present in the channel of MOS transistor at the Si/SiO_2 interface. The thermal oxide of 32nm as measured using ellipsometry was grown at 1050 °C in dry oxygen ambient. The wafer was cut into four pieces where two pieces were used as the annealed sample (in hydrogen or deuterium), and the other two pieces were used as the control samples for comparison. The annealing process was performed at 450 °C in the respective ambient (hydrogen, or deuterium) for 60 minutes. The infrared absorbance spectrum was measured using Themo Nicolet Nexus 470 FT-IR spectrometer with a variable angle specular reflectance accessory (Pike VeeMax II). The specular reflectance method was chosen because of the ease of obtaining the infrared spectrum since no additional sample preparation would be needed. The samples would only need to be placed on the specular reflectance accessory to obtain the infrared spectrum as shown in Figure 2.1. The spectral range was selected from 400 to 900 cm^{-1} with a resolution of 8 cm^{-1}.

Figure 2.2 shows the FTIR spectra of the H_2 annealed sample and the control oxide sample (without H_2 annealing), which shows a nearly identical absorbance intensity at the 400 to 520 cm^{-1} region. The absorption peaks in this region corresponds to the Si-Si TO and Si-O rocking phonon modes. It is also clear that Si-H bending mode at 592 cm^{-1} can be uniquely observed only in the hydrogen annealed sample, which confirms that the annealing process was sufficient for H atoms to diffuse through the oxide and form Si-H bonds at the Si/SiO_2 interface. Even though the calculated value for Si-H bending mode is around 650 cm^{-1}, we can safely assume that this absorbance peak can be attributed to Si-H bending mode since it is unique to the hydrogenated sample. It should be noted that the thermal oxide of approximately 32 nm was grown in order to observe the absorbance peaks due to the low sensitivity of specular reflectance measurements.
The absorbance spectrum for deuterated sample is shown in Figure 2.3. As described for the hydrogenated sample as shown in Figure 2.2, we can ascribe the main absorbance peaks at around 400 to 520 cm\(^{-1}\) to Si-Si TO and Si-O rocking mode. However, we can clearly distinguish the control sample (unannealed) and the deuterated sample from the difference in the absorbance intensity. In addition, there also exists a peak at 490 cm\(^{-1}\) in the D\(_2\) annealed sample, which can be attributed to the Si-D bending mode based on the relation between force constant, reduced mass and absorption frequency equation [58].

\[
\nu = \frac{1}{2\pi} \sqrt{\frac{k}{\mu}}
\]  

(2.1)

where \(\nu\), \(k\), and \(\mu\) are absorption frequency, force constant and reduced mass respectively. Since Si-H bending mode is known to be at 650 cm\(^{-1}\), we can calculate the Si-D bending mode value based on the ratio of the reduced masses between Si-H and Si-D. In addition, we can modify the vibrational frequency relation in equation (2.1) to obtain the wavenumber values for bond vibrational frequencies as shown in equation (2.2).

\[
\bar{\nu} = \frac{1}{2\pi c} \sqrt{\frac{k}{\mu}}
\]  

(2.2)

Since the wavenumber values are inversely proportional to the reduced mass, we can obtain the ratio of the square root of reduced mass of Si-H and Si-D bonds which is 0.72. The reduced mass equation can be described as shown in equation (2.3) below [59]:

\[
\mu = \frac{m_1 m_2}{m_1 + m_2}
\]  

(2.3)

where \(m_1\) and \(m_2\) are the atomic mass of Si (28) and that of either H (1) or D (2).

For Si-H:

\[
\mu = \frac{28 \times 1}{28 + 1} = 0.966
\]
For Si-D:

\[ \mu = \frac{28 \times 2}{28 + 2} = 1.897 \]

\[ \nu_D = \sqrt{\frac{\mu_H}{\mu_D}} = 0.72 \]

Thus, we can calculate the wavenumber of Si-D bending mode to be 468 cm\(^{-1}\), which is close to the observed absorption peak of 490 cm\(^{-1}\) in the deuterated sample.

The enhanced IR absorption of the Si-Si TO and Si-O rocking mode confirms that the energy of the Si-D bending mode is indeed coupled to the above mentioned bonds. Thus, this FT-IR experiments confirmed Van de Walle’s theory for the STM desorption experiments [46]. However, in the case of MOS transistor structure, the de-excitation process might also involve energy coupling to the Si-O rocking mode as well as shown schematically in Figure 2.4. Therefore, the oxide structure may also play a role in energy dissipation of the Si–D bond in MOS devices.

**2.4 Discovery of Phonon-Energy-Coupling-Enhancement Effect**

As mentioned in the previous section, Van de Walle’s theory of de-excitation process on MOS based structure involved energy coupling between Si-D bending mode and Si-Si TO mode as well as Si-O rocking mode. Dr. Zhi Chen proposed that the mismatch between Si-D bending mode and Si-Si TO mode might result in an inefficient coupling between the energy bonds. Thus, the H/D isotope effect might be enhanced if the Si-D bending mode could be shifted to match the Si-Si TO mode, which might result in an increase in the IR absorption intensity. It was suggested that a thermal stress might be able to achieve the abovementioned idea. RTP (Rapid Thermal Processer) a widely used tool in the semiconductor industry based on a rapid heating and cooling cycles, was chosen to perform the thermal stress.

The samples and experiment setups used for the RTP experiments were as described in Section 2.3, except that the oxide grown was approximately 23 nm. RTP was performed
in N₂ environment at University of Louisville’s RTA equipment (Modular Process Technology model RTP-600S) at 1050 ºC at a hold time of 4 minutes. The grown oxide sample was cut into three pieces; Sample 1 was used as a control (no further processing); sample 2 underwent RTP annealing (as mentioned above), and sample 3 was processed in RTP and annealed at 450ºC in D₂ ambient for 30 minutes. Figure 2.5 shows the absorbance spectrum from the FT-IR measurements (spectral range from 400 to 900 cm⁻¹ with a resolution of 8 cm⁻¹ [60]). The IR spectra ranging from 400 cm⁻¹ to 520 cm⁻¹ (Si-Si TO and Si-O rocking mode) showed a significant increase in the absorption intensity for samples processed in RTP (curve 2). The enhanced absorption intensity was shown to be larger (~50 %) than that of the samples annealed only in D₂ (~25%, shown in Figure 2.3). Although, the measurements are not based on quantitative measurements, the enhanced absorption intensity provides a qualitative comparison between the samples. The Si-Si TO and Si-O rocking modes, however, were not shifted as suggested earlier. This also led to an idea that RTP processing might have a beneficial effect on the quality of SiO₂ film.

MOS capacitors made of thick oxide (~10.2 nm SiO₂ thickness) subjected to RTP annealing (T=1050 ºC for 4 min.) was fabricated to understand the correlation between the enhanced Si-O absorbance intensity and the quality of the SiO₂ film. The front gate electrode of aluminum was defined using shadow mask. Post metal annealing (PMA) in deuterium at 450 ºC for 30 minutes was performed in both samples. As shown in Figure 2.6, there exists a two orders of magnitude of reduction of leakage current after RTP annealing, comparing to the control sample [60]. In addition, time-zero-dielectric-breakdown (TZDB) measurements showed that RTP annealed sample also exhibit larger breakdown voltage as shown in Figure 2.7 [61].

One major issue for MOS transistors is the large gate leakage current of ultra thin oxide due to quantum mechanical direct tunneling as described in the previous chapter. However, leakage current measurements on ultra thin oxide (~22 Å) fabricated using the RTP process (RTP @ 1050 ºC for 60 seconds) showed a reduction in the gate tunnel current as well. As shown in Figure 2.8 [60], the leakage current was reduced by five orders of magnitude, which is surprising, because it was unknown that the strengthened Si-O bonds
might have an effect on the direct tunneling current.

These results suggest that the quality of the SiO\textsubscript{2} film is improved and its IR absorbance is enhanced accordingly after RTP. This led to the naming of this process as “Phonon-Energy-Coupling-Enhancement.” Because only a small number of Si-D bonds exist at the SiO\textsubscript{2}/Si interface, majority of energy coupling mainly occurs from Si-O bonds to Si-Si bonds, which are caused by proper RTP processing.

2.5 Initial Study of RTP-Induced PECE Effect on Ultrathin SiO\textsubscript{x}N\textsubscript{y} [62]

The previous sections described the experimental study of PECE effect performed on SiO\textsubscript{2} films. However, the gate dielectrics used mostly in the semiconductor industry is a nitrided oxide film. The major benefit of using silicon oxynitride (SiO\textsubscript{x}N\textsubscript{y}) instead of SiO\textsubscript{2} is suppression of boron penetration from the poly-Si gate. In addition, the growth process of oxynitride is similar to that of SiO\textsubscript{2}. Thus, it would be beneficial if the PECE effects that were observed in the SiO\textsubscript{2} film exist in SiO\textsubscript{x}N\textsubscript{y} film as well. Since majority of chemical bonds in SiO\textsubscript{x}N\textsubscript{y} (~5-10% N) are Si-O bonds, it is expected that the PECE effect might still exist in SiO\textsubscript{x}N\textsubscript{y}.

Incorporation of N into SiO\textsubscript{2} can be performed either by thermal oxynitridation (via nitridation in N\textsubscript{2}O, NO, NH\textsubscript{3}, or in rapid thermal annealing in N\textsubscript{2}) or by chemical and physical deposition methods (e.g. CVD, ALD, JVD, plasma, or ion implantation) [63]. In order to mimic the growth processing or SiO\textsubscript{2} in a furnace, thermal oxynitridation in NO gas was used in this study. In addition, NO is believed to be responsible for the incorporation of N in SiO\textsubscript{x}N\textsubscript{y} by thermal oxynitridation of Si, or annealing in N\textsubscript{2} [64]. It is also worth noting that the self-limiting growth of SiO\textsubscript{x}N\textsubscript{y} behavior facilitates good thickness control in the ultra-thin regime (< 3nm), which was an important criteria in this study.

MOS capacitors were fabricated on 2 inch 1-10 Ω-cm p-type wafers. The wafers were initially cleaned using conventional RCA cleaning and etched in dilute HF (1:30) to remove any native oxide. The samples were then immediately loaded into Lindberg/Blue furnace at 800 °C with only N\textsubscript{2} gas flowing in the chamber to minimize/eliminate native
oxide growth. The furnace was ramped to 900 °C at a ramp rate of 15 °C/min to reduce thermal strain/stress on the wafers. The films were grown at about 1 atm in pure NO with 0.3 standard liters per minute (SLM) flow rate. Post oxidation annealing in N₂ environment was performed at the oxynitridation temperature of 900 °C for 15 minutes. The film thickness was measured using M-44 spectroscopic ellipsometer (J. A. Woollam Co., Inc).

The wafer was then cut into four pieces; samples 1 and 2 are control samples (no RTP treatment), sample 3 received RTP (Modular Process Technology Co. RTP-600S) treatment in nitrogen at 1050 °C for 30 seconds, and sample 4 received RTP treatment in nitrogen at 1050 °C for 60 seconds. Sample 2 (no RTP treatment) was used for XPS measurements. Aluminum film (thickness of 100 nm) was evaporated onto the rest of the samples (sample 1, 3, and 4) using thermal evaporator at base pressure of 2×10⁻⁶ torr. Circular electrodes (Area = 78.5 x 10⁻⁹ m²) were defined using photolithography (organic negative resist, SU8-2001) and lift-off process. The back contact was made following the steps described by Nicollian [65]; Native oxides were etched in buffered HF (6:1) for 2 minutes. Then, emery cloth was used to create a damaged region in the back surface of the silicon wafer. Post-metal annealing in deuterium at 420 °C for 10 minutes was performed on the devices. The thickness of the oxynitride layers on all the samples was measured using M-44 spectroscopic ellipsometer (J.A. Woollam Co., Inc). The current-voltage curves were measured using Agilent 4155B semiconductor parameter analyzer. High-Frequency Capacitance-Voltage (C-V) curves of MOS capacitors were measured using Keithley 590 CV Analyzer at 1 MHz.

XPS measurements were also performed on one of the control samples to identify the chemical composition of the as-grown oxynitride film. In this study, an XPS system (base pressure of 10⁻¹⁰ torr) with an Mg K α (1253.6 eV) x-ray source with a take-off angle of 57° was used. The sample was calibrated to center the C 1s peak at 285.0 eV.

Deconvolution of Si 2p and N 1s spectra obtained from XPS was performed since the binding energies of Si 2p in pure silicon (99.3 eV) and N 1s (400.1 eV) in atomic nitrogen are known [66]. Figure 2.9 shows the N 1s spectrum which was decomposed using
four Gaussian curve fitting. Four peaks were observed in the N 1s spectra with binding energies at 397.9, 400.6, 401.9, and 403.6 eV corresponding to the results of Chang et al. [67]. The peaks are attributed to NSi$_3$, NSi$_2$O, NSiO$_2$, and NO$_3$ bonding configuration respectively. This assignments are based upon the density functional theory (DFT) calculations by Rignanese et al. [68], where the approximately even spacing between peaks (~1.8 eV) matches the spacing for NSi$_3$, NSi$_2$O, NSiO$_2$, and NO$_3$ respectively. Figure 2.10(a) shows the O 1s spectrum with a distinct peak at 531.6 eV. The O 1s intensity is 25 times greater than the N 1s peaks, which is expected since thermal nitridation is dominated by formation of Si-O bonds. Figure 2.10(b) shows the Si 2p photoemission spectra decomposed into three major components using Gaussian curve fittings: Si, Si-N, and Si-O. The binding energies are at 99.4, 102.85, and 103.95 eV respectively. The SiO$_x$N$_y$ peak is expected to be between 102 eV (Si 2p of Si$_3$N$_4$) and 103.3 eV (Si 2p of SiO$_2$) and is located at 102.85 eV for our sample, which is consistent with the results reported by Yao et al. [69].

N concentration as well as Si and O in the oxynitride film were obtained using the approximation of atomic composition as shown in equation (2.4):

\[
\%C = \frac{A_i/S_i}{\sum A_i/S_i}
\]

(2.4)

Where C is the atomic composition of the element, $A_i$ is the area under the compound peak at half width, and $S_i$ is the sensitivity factor of the material.

The calculated concentration of N, O, and Si are 4.7 %, 66.9 %, 28.4 % respectively in the grown oxynitride film. The relationship between dielectric constant, $k$ and N concentration of oxynitride film has been studied extensively by Guo et al. [70], where one can obtain $k$ from the plot of $k$ vs. N (shown in Figure 1.5, Chapter 1) [70]. Thus, the dielectric constant of the grown oxynitride film is approximately 4.5 (compared to $k$ value of SiO$_2$ of 3.9 and Si$_3$N$_4$ of 7.8). The Equivalent Oxide Thickness (EOT) of the grown Si-O$_x$N$_y$ film is measured to be around 21 Å (measured from ellipsometer measurements using dielectric constant of 4.5).
The RTP-induced PECE effect can be observed on the leakage current measurements (tunneling current density, \( J_G \), versus gate voltage, \( V_G \)) of the MOS capacitor as shown in Figure 2.11. We observed leakage current reduction of 4 orders of magnitude after RTP processing plus deuterium anneal. The reduction of direct tunneling current might be due to the change of the energy band structure and the electron effective mass in the oxide/oxynitride. This, however still needs to be verified. Figure 2.12 shows the high-frequency C-V measurements of the p-type Al-gate MOS capacitors C-V curve. The measured flatband voltages, \( V_{FB} \) of \(-0.9\) V for both the control and RTP-treated samples is close to the ideal Al/oxide/p-Si MOS capacitor structure. This indicates that there is no significant amount of fixed charges in our oxynitride samples. However, there is a slight discrepancy in the accumulated capacitance value, which indicates either a change in thickness or a change in the dielectric constant. However, taking the increased thickness of the RTP-induced PECE effect into consideration (approximately 1 to 2 Å), the reduction of the tunnel current is still significant.

### 2.6 Conclusion

The basis for the study on PECE effect was to see an increase of the quality of the SiO\(_2\) due to RTP processing. However, RTP has been used in the semiconductor industry for quite some time. In the past, RTP was mainly used to activate dopant following ion implantation. Thus, the semiconductor industry should have observed the reduction of the leakage current. However, absorbance intensity of the Si-O bonds on thick oxide (FT-IR measurements on oxide sample thicker than 800 Å) was not observed as shown in Figure 2.13. This suggests that the PECE effect may not exists for the polysilicon/SiO\(_2\) gate structure due to the larger tolerance for thermal shock on thick gate oxides. In a conventional CMOS process flow in the semiconductor industry, the gate oxide is grown first, followed by polysilicon gate deposition. Thus, even if RTP was performed following dopant activation, the PECE effect will not be observed due to the presence of the polysilicon structure. In addition, the RTP process performed was not in the presence of pure N\(_2\) as was claimed in Reference [60] and [62]. This is due to the fact that an increase in the thickness SiO\(_2\) film following RTP processing at University of Louisville was observed. The process involved in replicating the PECE effect is not a simple RTP annealing step,
but involved other factors as well. In addition, the accumulation capacitance corresponding to oxide thickness could not be obtained in the results shown in Reference [60]. The procedure involved in obtaining correct C-V measurements that correlate to the thickness of the oxide as well as the procedures to accurately observing the PECE effects will be discussed in detail in the next few chapters.
Figure 2.1  Variable angle specular reflectance accessory (Pike VeeMax II)
Figure 2.2  Comparison of FTIR spectra between control (unannealed) and H$_2$ annealed SiO$_2$/Si sample (Thickness of SiO$_2$ is ~32 nm). The intensity of the Si-O and Si-Si TO are equivalent [54].
Figure 2.3 Comparison of FTIR spectra between control (unannealed) and D$_2$ annealed SiO$_2$/Si sample (Thickness of SiO$_2$ is ~32 nm). The intensity of the Si-O and Si-Si TO are enhanced with D$_2$ annealed sample due to the coupling between Si-D bending mode and the Si-Si TO mode [54].
Figure 2.4  Schematic representation of energy coupling process between Si-D and Si-Si TO and Si-O rocking mode.
Figure 2.5 Phonon-energy coupling enhancement (PECE) between Si-O rocking mode and Si-Si TO mode after RTP processing (T = 1050 ºC for 4 minutes hold time) of SiO₂/Si (Tox=230Å). The absorbance is enhanced with deuterium annealing (450 ºC for 30 mins) [60].
Figure 2.6  Comparison of leakage current measurements of sample with D$_2$ anneal and RTP (T = 1050 °C for 4 mins) plus D$_2$ anneal. The oxide thickness of the sample is 10.2 nm as measured using ellipsometer [60].
Figure 2.7  Comparison of Time-Zero-Dielectric-Breakdown (TZDB) measurements of sample with D$_2$ anneal and RTP (T = 1050 °C for 4 mins) plus D$_2$ anneal. The oxide thickness of the sample is 10.2 nm as measured using ellipsometer. Average values: 18 V for D$_2$ annealed devices and 26 V for RTP plus D$_2$ annealed devices [61]
Figure 2.8  Comparison of Gate Leakage Density of MOS capacitor ($T_{\text{oxide}} = 2.2 \text{ nm on N+ wafer, } N_d = 1 \times 10^{19} \text{ cm}^{-3}$) between control sample and RTP (60 secs at 1050 °C) [60].
Figure 2.9  Deconvolution of N(1s) spectra of NO oxynitride control sample
Figure 2.10 (a): O(1s) XPS spectra of NO oxynitride control sample; (b) De-convolution of Si(2p) XPS spectra of NO oxynitride control sample
Figure 2.11 Comparison of tunneling current density of RTP-induced PECE effect oxynitride film and control sample
Figure 2.12 Comparison of High-frequency (1 MHz) C-V measurements of RTP-induced PECE effect devices (RTP @ 1050 °C for 30 and 60 secs) and control sample.
Figure 2.13 Comparison of FTIR spectra for thick oxide (800Å) between control and RTP-annealed sample at 1050 °C. No change in absorbance intensity observed.
3.1 Introduction
This Chapter describes the experimental setups and materials used in the fabrication of devices in the Phonon-Energy-Coupling-Enhancement (PECE) effect experiments. The primary focus for this Chapter is to describe the RTP setup to conduct the PECE effect experiments.

3.2 Growth of Ultra thin SiO₂
The MOS capacitor is one of the simplest structure used to characterize the quality of the insulator and its electrical properties such as thickness of the dielectric, oxide charges, leakage current density, breakdown voltage, substrate dopant density and flatband voltage. The structure consists of a dielectric layer sandwiched between the metal gate electrodes at the top and silicon substrate on the bottom. The electrical connection to the silicon substrate is usually formed by deposition of highly conductive metals such as Aluminum. Fabrication of MOS capacitors starts with forming the oxide layer as the gate dielectric in a thermal furnace. The Si substrate however, has to be cleaned prior to growing the oxide layer as any contaminants present on the substrate will affect the quality of the oxide grown. The wafer cleaning process entails the RCA clean procedure developed by Dr Werner Kern [71]. Prior to loading the wafer into the thermal furnace at 900 °C, the Si wafer was etched in dilute HF solution to remove chemical oxide grown during the RCA cleaning process. In order to minimize the growth of oxide in ambient air, the Si wafer loaded into the thermal furnace quickly in N₂ ambient. The thin SiO₂ layer was grown at 900 °C in dilute O₂ ambient (5% O₂:N₂). Post-Oxidation-Annealing (POA) in N₂ ambient was performed after the short oxidation time (~ 20 seconds) for 30 minutes. The POA step is necessary to reduce fixed oxide charges. The thickness of the oxide ranging from 20 to 25 Å as measured using an ellipsometer. The next step consists of subjecting the samples to RTP processing according to the experimental plan described in the next section. The complete process flow for the MOS capacitor fabrication is de-
scribed in detail in Chapter 6.

3.3 Rapid Thermal Annealing

Rapid Thermal Annealing (RTA) is a process used in semiconductor industry for a number of process steps such as dopant activation, silicidation, and also growth of ultra thin thermal oxide (Rapid Thermal Oxidation, RTO). RTA was developed to minimize the thermal budget of a process by rapidly heating and cooling samples at rates that are unattainable in conventional process. The equipment used in this RTA process is a Modular Process model RTP-600S. The RTP chamber is shown in Figure 3.1(a) from the front view and Figure 3.1(b) from the back view. High volume purge gas (He or N₂) is connected to GAS 1 line, while process gases (pure He, pure N₂, trace O₂:He, trace O₂:N₂, and trace H₂O:He/N₂) is connected to GAS 2 line. The gas flow rates are controlled by a built-in MFC (Mass-Flow-Controller).

3.3.1 Temperature Measurements

Temperature control of the RTP equipment used in this study is based on a closed-loop pyrometer control. Pyrometers operate by measuring the radiant energy received and converting the power to the source temperature. The actual temperature however needs to be calibrated using thermocouple (TC- type K), which measures the temperature on the Si substrate holder directly, as shown in Figure 3.2. The thermocouple was placed on the wafer holder (4 inch) only during the recipe calibration run. Subsequent processing for RTP experiments was performed without the TC in order to minimize contaminations from the chemical reactions with the Si substrate holder. A typical RTP run is shown in Figure 3.3. The ramp rate is usually set at 10 °C/secs up to the desired temperature. The lamp intensity in the RTP chamber increases during the ramp up procedure and reaches a peak value at the beginning of the hold cycle. During the hold cycle, the lamp intensity decreases gradually to maintain the temperature at the hold cycle. Thus, we can approximate the temperature at the RTP chamber at the hold cycle by monitoring the pyrometer peak intensity. The peak lamp intensity corresponding to the temperature in the RTP chamber is shown in Figure 3.4. At the end of the hold cycle, the radiation from the
RTP chamber (lamp intensity) is turned off completely. In order to cool down the temperature rapidly, high volume (~20 Standard-Liter-Per-Minute, SLM) purge gas (Helium) is flowed through the quartz chamber across the wafer. In addition, compress air and chilled water is flowing around the RTP quartz chamber to aid in the cooling process. The cooling rate is determined to be around 80 to 100 °C/sec.

3.3.2 Trace moisture ambient in RTP process setup

The experimental setup for the trace moisture RTP process is shown in Figure 3.5. The moisture content is controlled by the mixture of dry gas (Flowmeter 1) and wet gas (Flowmeter 2). High purity N\textsubscript{2} is used as the carrier gas. In order to minimize excess moisture concentration into the RTP chamber, a set of pressure control valves are placed systematically following these particular process steps:

1) Close all valves prior to any experimental runs.

2) The moisture level in the bubbler is saturated initially. Valve #1 and #3 are turned on, where dry gas (He or N\textsubscript{2} from flowmeter #2) are flowed through the bubbler and out to air ambient to reduce the saturated moisture content in the bubbler. This step is necessary to ensure that high moisture levels are not present in the gas line through the RTP chamber.

3) Valve 4 controls the mixture of dry and wet gases into the RTP chamber. Valves #2 and #4 are turned on 10 minutes after performing step #2. Valve #3 is then turned off to allow the mixture of dry and wet gases flow into the RTP chamber. The moisture content is monitored by the inline Dew Point Meter (JLC International Shaw Inline Dew Point Meter), where the amount of moisture content (ppm) is controlled by the ratio of flowmeter 1 and flowmeter 2.

The dew point meter provides an accurate representation of moisture concentration in the gas line. Flowmeter #2, which controls the dry gas flow rate is set at 2 SLM (Standard-Liter-per-Minute), while the wet gas flow rate is adjusted according to process needs (moisture content). The relation between moisture concentration (measured at parts-per-million, ppm) and the gas flow through the bubbler (wet gas) is shown in Figure 3.6.
3.3.3 Trace O₂ RTP process setup

Figure 3.7 shows the experimental setup for trace O₂: He RTP experiments. The process gas (mixture of He:O₂) of the oxygen concentration (monitored in parts-per-million, ppm) is monitored using an inline trace O₂ analyzer (Alpha Omega Series 3000). The concentration of O₂ is controlled by varying the oxygen flow (Flowmeter #1), while the carrier gas, He (Flowmeter #2) is set at a fixed flow rate of 2 SLM.

3.4 Oxide Thickness Determination from C-V Measurements

3.4.1 Introduction

The need for accurate and precise thickness measurements of ultra thin SiO₂ is vital in the study of RTP-induced PECE effect experiments. The thickness of the SiO₂ film was determined by ellipsometer measurements due to its simplicity, fast, precise, and nondestructive nature in our previous RTP-induced PECE effects works [37, 72, 73]. In addition to ellipsometry measurements, thickness of oxide films can be determined using HRTEM (High-Resolution-Transmission-Electron-Microscopy) and also from the accumulation region of MOS capacitors in Capacitance-Voltage (C-V) measurements. HRTEM, which provides a measure of thickness of the dielectric through direct imaging the cross section of the silicon substrate, was not performed in our study. This is due to the significant amount of time needed to prepare samples for the imaging purpose. In addition, the principal limitation of HRTEM image analysis is the uncertainty in locating the exact position of the interface that defines the oxide layer. The HRTEM image obtained yields only a small portion of the film and may not be an accurate representation of the film as a whole as opposed to ellipsometry and C-V measurements.

3.4.2 Oxide Thickness extraction from C-V measurements

In our previous work [37, 72, 73], the thickness of the oxide film could not be accurately obtained from C-V measurements. Traditionally, oxide thickness (dielectric) can be extracted from a MOS capacitor using a parallel capacitance model \( t_{ox} = \frac{\varepsilon A}{C_{ox}} \) as described in equation (1.2). However, this simple model does not hold for thin oxides as the
accumulation region does not saturate as in thick oxide films, but rather increases with increasing gate voltage. This is caused by quantum mechanical (QM) confinement effects near the SiO$_2$-Si interface, and finite voltage drop across polysilicon gates (poly-Si depletion) [74]. The QM confinement effects [75] causes additional band bending under the gate oxide creating a quantum well that splits carrier energy band into subbands. The band bending occurs because the surface carriers (holes or electrons) are located in localized energy levels above the conduction band edge. In addition, the charge centroids are shifted further from the surface, where the maximum carrier concentration is located ~1 nm under the gate oxide as shown in Figure 3.8. The QM effect results in an additional capacitance in series with the gate oxide capacitance ($C_{ox}$), which reduces the effective oxide capacitance (thicker EOT) as illustrated in Figure 3.9. The classical C-V without QM effect or poly-Si depletion effect is simulated using the MATLAB program in the Appendix section, while the C-V curve accounting for QM effect is simulated using Berkeley QM C-V simulator. The simulated parameters are $t_{ox} = 25$ Å, $N_d = 5 \times 10^{16}$ cm$^{-3}$, and $V_{fb} = 0.006$ V. As shown in the figure, the classical C-V curve overestimated the oxide layer by 3 Å. Optical measurements using ellipsometer technique were conducted to verify this extraction scheme. Figure 3.10 shows that the oxide thicknesses as extracted from the Berkeley QM C-V simulator are measured to within 1 Å of those measured by ellipsometry with multiple measurement angles (index of refraction, $\eta = 1.45$).

In addition to QM effects, oxide capacitance could also be affected by the quality of the metal electrode, where an additional series resistance from metal contacts could significantly reduce the accumulation capacitance values due to the sensitivity nature of C-V measurements. The reduction in accumulation region of MOS capacitor occurs also in samples that were not subjected to Post-Metallization-Annealing, where an additional air gap layer could be formed. This is described in detail in Chapter 6. Leakage current density, $J_G$ however, was not affected by the series resistance. This is due to the high current/low resistance path in the ultra thin insulator layer, which is significantly higher than series resistance from the metal contact.

Figure 3.11(a) shows the leakage current density measurements and C-V measurements
of MOS capacitors fabricated using two SiO$_2$ film thickness (~25 and 26 Å) as measured using a spectroscopic ellipsometer. One of the samples was fabricated using conventional MOS capacitor process flow, where the top gate electrode, Aluminum was defined via lift-off process. Post-Metallization Annealing (PMA) however, was not performed on this sample due to the probability that Aluminum will diffuse through the thin oxide layer causing an electrical shorting path. The other sample was fabricated using Nickel as the top gate electrode and annealed at 450 °C in forming gas ambient (10% H$_2$:N$_2$). As shown in Figure 3.11(b), the accumulation capacitance for the Aluminum gate sample without PMA showed a much lower value as compared to the Nickel gate electrode sample with PMA. The thickness of the oxide layer was extracted via UC Berkeley Quantum-Mechanical Simulator (taking quantum correction into consideration) and listed in Table 3.1. The leakage current density, J$_G$ for both samples however, are almost similar except for voltages < 1 V. It should be noted that the flatband voltage, V$_{FB}$ is different for both samples due to the difference in work function between the metals. The leakage current measured for the sample without PMA display a lower value due to the series resistance/air gap within the structure. However, the reduction in J$_G$ is not significant as compared to the reduction in capacitance. In addition, it worth noting that the J$_G$ value measured at (V$_{FB}$-1V) for both samples are almost similar and is comparable for standard oxide thickness in the 25 to 26 Å range (1 x 10$^{-3}$ A/cm$^2$) [76].

3.5 Conclusion
The experimental setup concerning the process gases used (trace moisture and trace O$_2$) was described in detail. In addition, we explained that thickness of SiO$_2$ film extracted via ellipsometry and C-V measurements are accurate representations. It was found that leakage current measurements are not significantly affected by series resistance/air gap from MOS structure as compared to C-V measurements.
Table 3.1: Thickness comparison of MOS capacitors fabricated with and without PMA extracted via ellipsometer and C-V measurements.

<table>
<thead>
<tr>
<th>Sample</th>
<th>EOT (Å)</th>
<th>Ellipsometer</th>
<th>C-V Simulated</th>
</tr>
</thead>
<tbody>
<tr>
<td>No PMA Al</td>
<td>25</td>
<td></td>
<td>36.2</td>
</tr>
<tr>
<td>PMA Nickel</td>
<td>26</td>
<td></td>
<td>25.5</td>
</tr>
</tbody>
</table>
Figure 3.1  Schematic illustration of RTP equipment used in this dissertation study (Modular Process RTP-600S) viewed from: (a) front and (b) back.
Figure 3.2  Temperature measurement of RTP process via thermocouple.
Figure 3.3 Temperature and Intensity Profile of a typical RTP process run
Figure 3.4 Relationship between temperature at hold cycle during RTP process and the peak intensity measured by pyrometer

\[
y = 650.52 + 7.8353x \quad R = 0.99741
\]
Figure 3.5  Schematic illustration of trace moisture as process gas in RTP experiments
Figure 3.6 Moisture concentration (parts-per-million, ppm) dependent on flow rate (standard-cubic-centimeter-per-minute, sccm) of carrier gas in trace moisture RTP process step. Note that the flow rate of N$_2$ corresponds to flowmeter #1 in Figure 3.4, while flowmeter #2 (dry gas) is fixed at 2 SLM (Standard-Liter-per-Minute)
Figure 3.7  Schematic illustration experimental setup for RTP experiment using trace O₂ as process gas
Figure 3.8  Quantum mechanical effect on charge densities depicting electron distribution calculated from Classical models (Maxwell-Boltzman, MB and Fermi-Dirac (FD) statistics) [77]
Figure 3.9  Comparison of simulated C-V curves between classical and quantum-mechanical model (Berkeley Quantum-Mechanical Simulator). Simulated parameters are $t_{ox} = 25$ Å, $N_D = 5 \times 10^{16}$ cm$^{-3}$, and $V_{fb} = 0.006$ V.
Figure 3.10 Comparison between thickness of oxide extracted from ellipsometer and C-V measurements. The oxide thickness obtained from C-V measurements (extracted from Berkeley QM simulator) represents the average of 20 devices. The ellipsometer thickness measurements represent the average of 5 data points from different location of the sample.
Figure 3.11 Comparison of electrical characterization of MOS capacitors using SiO$_2$ fabricated utilizing Al and Nickel as gate electrode: (a) Leakage current measurement (b) C-V measurement. PMA was not performed for the Al gate sample.
4.1 Introduction

4.1.1 Introduction to FT-IR Spectroscopy

The background for the Phonon-Energy-Coupling-Enhancement Effect (PECE) was established and described in detail in Chapter 2. The FT-IR experiments that were conducted were only explained briefly. The experimental setups and considerations required as well as extension works on infrared spectroscopy measurements will be described in detail in this Chapter.

Infrared spectroscopy is a characterization technique that is based on (change in dipole moments) vibrations of atoms of a molecule. The infrared spectrum can be obtained by passing infrared radiation through a sample of interest and determining the fractions of the incident radiation that is absorbed at a particular energy. The frequency of the vibration of a sample is correlated to the peaks in the absorption spectrum. In addition, the energy of most molecular vibrational modes correspond to the infrared region (usually characterized as the mid infrared region) of the electromagnetic spectrum, between $400 \text{ cm}^{-1}$ to $4000 \text{ cm}^{-1}$, which is also the operational region of most FT-IR (Fourier-Transform Infrared) instruments [78]. This chapter is devoted to the application of infrared spectroscopy to understand the mechanism of the Phonon-Energy-Coupling-Enhancement (PECE) effect on oxidized semiconductor substrates.

4.1.2 Reflectance Sampling Technique

Choosing the right sampling technique is one of the most important considerations involved in performing FT-IR measurements. The three most common sampling techniques are transmission, reflectance and photoacoustic spectroscopy (PAS). Reflectance sampling technique or more specifically specular reflectance was used in the study of the mechanism of the PECE effect. FT-IR measurements were performed using a variable angle
(30° to 85°) specular reflectance accessory (Pike VeeMax, manufactured by Pike Technologies) to obtain absorbance properties of the thin SiO₂ layer on silicon substrate. This section will explain the reasoning behind the use of reflectance sampling technique instead of transmission sampling technique.

In the reflectance sampling technique, the surface contributes most strongly to the infrared spectrum. In contrast to transmission sampling technique, the bulk of a sample rather than surface contributes strongly to spectrum. Thus, the fact that reflectance techniques obtain the spectrum of the surface of a sample is good since the surface of the sample is of interest (SiO₂ film on Silicon substrate). In addition, as compared to transmission experiments, the thickness of the sample is not a concern. Thus, sample preparation is simple and faster. Grinding or polishing of the silicon substrate to obtain a thin layer as well as the need for double sided polished silicon wafers are not required for transmission measurements. This is due to the fact that the rough side of a single sided polished wafer can scatter infrared light significantly.

However, there are some disadvantages for this technique. For example, it is difficult to accurately determine the depth of penetration and the pathlength. The depth of penetration depends upon the properties of the surface and the angle of incidence. In addition, pathlength is a quantity of absorbance based on Beer-Lamberts’s law. Thus, quantitative measurements are difficult to obtain. This however, is not a concern for our measurements since we only compare the absorbance values in a relative manner.

Beer-Lambert’s law, which is the basis of all quantitative measurement, can be described in the equation below [78]:

\[ A = \varepsilon \cdot c \cdot l \]  

(4.1)

where \( \varepsilon \), \( c \), and \( l \) are molar absorptivity, concentration, and pathlength respectively. It should be noted that absorbance is a unitless quantity since the units of \( \varepsilon \) are usually given in the inverse of the product of concentration and pathlength, which cancels out the other two variables in Beer's Law.
4.1.3 Specular Reflectance

The use of the specular reflectance technique provides a non-destructive means for sample analysis with no sample preparation. The basis for specular reflectance is that the reflected angle of incidence equals the angle of reflectance, as shown in Figure 4.1. The amount of light that is reflected back depends upon the angle of incidence, refractive index, surface roughness and the absorption properties of the sample. In the case of thin SiO$_2$ film on Si substrate, specular reflections are assumed to occur at the ambient-film (SiO$_2$) and film (SiO$_2$)-substrate (Si) interfaces. The infrared beam passes through the SiO$_2$ layer, reflects through the smooth Si surface and passes through the SiO$_2$ film a second time as shown in Figure 4.2(a). The silicon substrate is treated as infinitely thick, thereby a negligible amount of backside scattered light is assumed to be present in the reflected beam. In addition, the roughed backside of a single polished wafer actually simplifies the measurement by reducing multiple reflections within the wafer.

The incident FTIR beam $I_0$ is illuminated at an angle of incidence $\theta_1$. Part of the beam is reflected from the sample surface, $I_R$ and the other is transmitted into the sample, $I_T$ at an angle of $\theta_2$ based on Snell’s Law as shown in equation (4.2).

$$n_1 \sin \theta_1 = n_2 \sin \theta_2$$

(4.2)

The beam reflects back to the surface of the thin film (SiO$_2$) at the reflective surface (Si substrate). The spectra obtained from reflectance-absorption technique are typically of high quality and similar to spectra obtained from transmission measurements. In addition, for high angles of incidence (between 60 to 85 degrees), only the electromagnetic field in the plane of incident and reflected beam is enhanced as shown in Figure 4.2(b). This is caused by the surface selection rule, where the vibration with component dynamic dipole moment is aligned perpendicular to the surface interacts with the $p$-polarized incident light [78]. Thus, strong absorbance spectrum comparable to transmission sampling technique can be easily achieved.
4.2 FT-IR measurements setup and considerations

The FT-IR measurements that were performed in this study involved qualitative and quantitative analysis. The qualitative analysis involved determining the peak positions of the vibrational modes of interest. Quantitative analyses however, are not as straightforward as qualitative analysis as described previously due to Beer-Lamberts law.

In FT-IR measurements, absorbance is defined as:

\[
A = \log\left(\frac{I_0}{I}\right) = \log_{10}\left(\frac{1}{T}\right)
\]

(4.3)

Where \(I_0\), \(I\), and \(T\) are intensity of incident radiant flux, transmitted radiant flux, and transmittance of the sample respectively.

The FT-IR instrument that was used (Thermo Nicolet model Nexus 470) is a single-beam instrument, in which the absorbance spectra are not obtained in real time. The single beam spectrum is a plot of raw detector versus wavenumber. In order to obtain the absorbance bands from the sample, a background spectrum is obtained once prior to collecting the infrared spectrum of the sample of interest. The background spectrum consists of contribution from any ambient water, and carbon dioxide present in the optical bench. Ideally, the final spectrum should be free of all instrumental and environmental contributions, and should only contain features from the sample. Thus, the optical FT-IR bench needs to be purged with nitrogen gas and be equipped with a dessicator in order to reduce CO\(_2\) level and ambient water respectively. In addition, the background spectrum that was used has to be obtained from a Si substrate similar to the sample of interest. The Si substrate used for the background spectrum is etched with dilute HF to remove its native SiO\(_2\) layer. This helps match the reflective properties of the sample and background and produces a better spectrum.

Figure 4.3 shows the background spectrum of Silicon wafer (N-type, (100) orientation, dopant density of 1x10\(^{19}\) cm\(^{-3}\)) with an angle of incidence varying from 65 to 75 degrees. As shown in the figure, a higher angle of incidence results in higher spectrum intensity. If
the reflective properties of the background and the sample are significantly different, the contribution from the sample of interest will be hard to observe because the spectrum is a ratio of the background and the measured sample. Thus, the background spectrum has to be measured again if a different angle of incidence is used. The contribution from carbon dioxide (CO₂) and moisture (H₂O) can also be easily seen from the background spectra. The CO₂ peaks are shown at 2360 cm⁻¹ and also at 667 cm⁻¹, while H₂O peaks are shown as an irregular group of lines at 3600 cm⁻¹ and at about 1600 cm⁻¹. The FT-IR instrument is usually purged with dry N₂ gas overnight prior to performing FT-IR measurements until the CO₂ absorption peak at 2350 cm⁻¹ became undetectable and H₂O level in the background spectrum is of minimal level as shown in Figure 4.4.

The analysis of the infrared spectrum that was obtained requires the use of proper spectral manipulation to label and relate the peaks of interest. The method that was used in the quantitative analysis is the Baseline method, where a line is drawn to connect adjacent known baseline value. This method however requires initial estimate of the known peaks and is subject to errors if not performed correctly. Thus, measurements of a given sample are usually performed at least 10 times to obtain the average of the infrared spectrums and correct the baseline as necessary. In addition, to improve the signal to noise ratio 256 scans were used with 8 cm⁻¹ resolution. The FT-IR setups and considerations described in this section will be used to obtain spectra and analyze samples in the study of the PECE effect in the next few sections.

4.3 Optimizing Angle of Incidence of Specular Reflectance FT-IR Measurements

4.3.1 Introduction

Infrared spectroscopy (IR) is one of the most suitable techniques used to study the chemical composition and structures of SiO₂ films. Infrared spectroscopy of SiO₂ films could provide information on oxygen stoichiometry, thickness, density, and local atomic structure of oxide films formed on Si. Sensitivity however, is a limiting factor in spectroscopic detection of thin films. Quantitative determination of bond concentration is hard to de-
termine due to insufficient instrument sensitivity for thin films. In addition, the noise level in thin films is comparable to the absorption intensity of the measured sample. Thus, we have to work on SiO$_2$ films that are thicker than 100 Å in order to be able to quantitify the absorption peaks.

There exist three infrared vibrational modes in the infrared absorption spectrum of a amorphous or crystalline SiO$_x$ in the mid-infrared region of 400–4000 cm$^{-1}$ [79]. The vibrational modes are shown in Figure 4.5, and can be classified as Si-O rocking, bending, and stretching modes. The Si-O rocking mode is located at the lowest vibrational frequency at $\sim 450$ cm$^{-1}$, where the rocking motion of the bridging oxygen atoms are perpendicular to the Si-O-Si bonding plane. The intermediate vibrational frequency (Si-O bending mode) which also exhibit the weakest absorption is located at $\sim 810$ cm$^{-1}$, where the bending motion of the oxygen atoms is located along the bisector of the Si-O-Si bond angle at $\sim 150^\circ$. The strongest absorption vibrational mode, Si-O stretching mode is located at $\sim 1075$ cm$^{-1}$, where the oxygen atom is in the Si-O-Si bonding plane in the direction parallel to a line joining the two Si atoms. The Si-O infrared vibrational modes provide information about the growth mechanism and the structural feature of SiO$_2$ films.

Reflectance measurements on thin films are usually performed at a large angle of incidence to obtain the maximum sensitivity. In the case of infrared spectrum on SiO$_2$, most characterization work on the quality of the oxide focused on the Si-O stretching mode, (located at $\sim 1000$ to 1100 cm$^{-1}$) which is also the most intense absorption peak [80-82]. Information of the SiO$_2$ film such as chemical bonding character, strain relief of the bond, stoichiometry of the film, porosity and density change, can be obtained from the Si-O stretching vibrational mode [83]. The basis of the Phonon-Energy-Coupling-Enhancement (PECE) effect as described in Chapter 2, is an enhanced intensity of the Si-O and Si-Si bonds due to the energy coupling between Si-O rocking mode and Si-Si bonds located in the 400-500 cm$^{-1}$ wavenumber region. Thus, it is critical that the optimum angle of incidence is chosen to obtain the maximum intensity of infrared absorption in the Si-O rocking mode.
4.3.2 Results and Discussion

Figure 4.6 shows the FT-IR absorption spectra measurements of a 230Å SiO₂ film which was grown thermally by dry oxidation condition on a N(100) Silicon substrate (dopant density of 1×10¹⁹ cm⁻³). The SiO₂ thickness was measured using spectroscopic ellipsometry with a fixed refractive index of 1.455. Specular reflectance of the FT-IR absorption spectra was performed with varying angle of incidence from 30° to 80°.

As shown in Figure 4.6, Si-O stretching mode is observed to split into two distinct absorption peaks at 1084 cm⁻¹ and 1257 cm⁻¹. The peaks were attributed to transverse-optical (TO) and longitudinal optic (LO) phonons respectively [84, 85]. The absorption intensity of the Si-O vibrational modes (Si-O stretching TO and LO, and Si-O rocking mode) with respect to the angle of incidence is shown in Table 4.1. It is worth noting that the peak position of LO and TO mode are independent of incident angle and the Si-O bending mode can only be observed at the lowest angle of incidence (30°), close to the normal plane since it is the weakest absorption mode. The highest absorption intensity for each of the respective Si-O vibrational modes is shown in bold.

As shown in Table 4.1, the highest absorption intensity for Si-O rocking mode is obtained at an angle of incidence of 65° while the highest absorption intensity for both the Si-O stretching mode is obtained at 30°. Figure 4.7 shows the dependence of the angle of incidence to the absorption intensity at the Si-O rocking mode only. It can be clearly observed that the maximum sensitivity for the Si-O rocking mode is at 65° angle of incidence. Thus, since the study of the PECE effect is focused on the Si-O rocking mode, the choice of the angle of incidence of 65° will be used. It should be noted that the Si-Si bond is not shown because the signals from the Si substrate were subtracted from the spectra. Thus, signal from Si-Si bonding was totally screened out by the strong signal from the Si substrate in the IR spectra of the sample and hence hard to illustrate. The Si-Si absorption mode though weak, was however observed by Wei et al. [86] at 495 cm⁻¹ for a normal mode transmission infrared spectra.
Table 4.1: Absorption intensity for Si-O rocking, Si-O stretching TO, and Si-O stretching LO with respect to angle of incidence.

<table>
<thead>
<tr>
<th>Angle</th>
<th>Si-O rocking (466 cm⁻¹)</th>
<th>Si-O stretching TO (1084 cm⁻¹)</th>
<th>Si-O stretching LO (1257 cm⁻¹)</th>
</tr>
</thead>
<tbody>
<tr>
<td>30°</td>
<td>0.0051</td>
<td>0.0174</td>
<td>0.00697</td>
</tr>
<tr>
<td>65°</td>
<td><strong>0.00584</strong></td>
<td>0.012</td>
<td>0.002</td>
</tr>
<tr>
<td>73°</td>
<td>0.00426</td>
<td>0.0095</td>
<td>0.00436</td>
</tr>
<tr>
<td>75°</td>
<td>0.0041</td>
<td>0.0088</td>
<td>0.004922</td>
</tr>
<tr>
<td>80°</td>
<td>0.00296</td>
<td>0.00673</td>
<td>0.00566</td>
</tr>
</tbody>
</table>

The appearance of the Si-O stretching LO mode is odd since electromagnetic (EM) waves in theory are only capable of interaction with TO modes because light propagates as a transverse wave and do not interact with the LO phonons in an infinite network [87]. However, since the infinite boundary conditions are not met for thin films, the LO can be detected as long as two requirements as met [88]:

a) The film thickness condition of:

\[
\frac{2*\pi*d}{\lambda} \ll 1
\]

(4.4)

Where d is the film thickness and \(\lambda\) is the wavelength of incident light. The thickness of the grown SiO₂ sample is 230Å while the LO mode is observed around 1257 cm⁻¹. Using equation (4.4), it can be shown that the thickness of 230Å satisfy the required condition.

\[
\lambda = \frac{1}{\nu} = 7.95 \times 10^{-4} \text{ cm}
\]

\[
\frac{2*\pi*d}{\lambda} = \frac{2*\pi*(230 \times 10^{-8} \text{ cm})}{7.95 \times 10^{-4}} = 0.0182 \ll 1
\]

b) The incident beam must be oblique and \(p\)-polarized

This phenomenon is due to the Berreman effect [88], where \(p\)-polarized light having an electric-field vector in the plane of incidence under an oblique incidence is able to excite LO mode and TO phonon modes in a thin film material. However, the LO phonon mode
of unpolarized spectra at oblique incidence reflectance has been reported, similar to our
FT-IR experiment [83, 89, 90].

The appearance of the LO mode was postulated to exist due to optical properties [91].
This is due to the fact that the SiO2 film is thinner than the infrared wavelength. The optical
properties can be determined by observing the spectral dependence of the material’s complex optical constant, which consists of the refractive index (n) and the extinction
coefficient (k). Figure 4.8(a) shows the complex refractive index of SiO2 obtained from
the optical data (in the range of Si-O stretching mode, from 900 to 1300 cm^-1) as pro-
vided by optical constant handbook [92].

The TO mode arises from the interaction of IR photons with TO mode phonons. The peak
position of TO mode can be calculated from obtaining the maxima of infrared dielectric
constant \( \varepsilon_2 \), which is the imaginary part of the complex dielectric response function [89].

\[
\hat{\varepsilon} = \varepsilon_1 + \varepsilon_2 = (n \pm ik)^2 = (n^2 - k^2) + j(2nk) \quad (4.5)
\]

\[
\varepsilon_1 = n^2 - k^2 \quad (4.6)
\]

\[
\varepsilon_2 = 2nk \quad (4.7)
\]

The peak position of LO mode occurs at the maxima of the energy-loss function as
shown in equation (4.8) [89]:

\[
\text{Im}\left(-\frac{1}{\varepsilon}\right) = \frac{\varepsilon_2}{(\varepsilon_1^2 + \varepsilon_2^2)} \quad (4.8)
\]

The infrared dielectric constant and energy loss function are shown in Figure 4.8(b). The
maxima for the curves are the TO (1090 cm^-1) and LO (1250 cm^-1) mode respectively,
which almost matches the values obtained for measured thermal SiO2 sample (see Table
4.1). It should be noted that the optical constants used [92] in the calculations were based
on glass structure (where the structural composition is different from thermal SiO2).

In addition to the appearance of the Si-O stretching LO mode, the variation of the spectra
of the LO and TO mode region is also intriguing. The line shape and intensities change
dramatically with incident angle. At low incident angle, the LO mode points in the opposite direction as compared to TO mode, bending mode and rocking mode. This phenomenon is also observed for reflectance measurements conducted elsewhere [80, 93]. At or near the Si Brewster angle however (>68° in our infrared measurements), the LO mode inverts and points in the same direction of the TO mode. The Brewster angle for Si can be calculated using the equation below:

\[
\theta_B = \arctan\left(\frac{n_2}{n_1}\right)
\]

The Brewster angle, \(\theta_B\) for Silicon is located at 73.7° using refractive index of 3.42 [92]. However, as shown in the Figure 4.6, the LO phonon mode cannot be observed at 69° instead it is observed at an angle of 73.7°. Recall that the LO phonon mode can only be observed for \(\rho\)-polarized light at Brewster angle, which contradicts our measurement at 69°. This could be due to a large spread (probably around 3° to 4°) of the incident angle from the instrument itself. A larger spread in the incident angle could affect the reflectance significantly near the Brewster angle, where the reflectance is changing more rapidly. In addition, another likely cause is the reflectance from the backside substrate of the silicon wafer. It was assumed early that the Si substrate is infinitely thick and reflectance from the backside is weak due to scattering from the rough back surface and the assumption of an infinitely thick substrate.

As the angle of incidence increases above 69°, the LO mode can be observed again, gaining intensity at the higher angle of incidence. However, the LO mode points in the same direction as the TO mode at this point and dominates the TO phonon mode at this higher incidence angle. This mechanism is due to a manifestation of the optical properties of SiO\(_2\) on Si system due to the offset of the real refractive index, \(\eta\) as explained by Wong et al. [93].

4.4 Measurement of strain/stress from Si-O stretching mode

In infrared spectrum of SiO\(_2\), the main absorption region originates from asymmetric bond stretching of Si-O at 1000-1100 cm\(^{-1}\) which is the strongest Si-O absorption vibra-
tional mode. Although, the study on the PECE effect on SiO$_2$ is mainly focused on the Si-O rocking mode, the Si-O stretching mode is of importance as well. Numerous research works are based on correlating the chemical bonding character, strain, and stoichiometry of the film to the vibrational frequency of the Si-O stretching mode.

As described earlier, the Si-O stretching mode is split into LO and TO phonon modes for thin oxide films measured at oblique angle of incidence. In order to simplify the analysis of Si-O stretching mode, thick SiO$_2$ film (550 nm as measured using ellipsometer with a fixed refractive index of 1.455) was deposited using e-beam evaporatoration. Figure 4.9 shows the absorption spectrum of the Si-O vibrational modes in the 400 to 1400 cm$^{-1}$ region measured at 65° angle of incidence. Although, the LO mode is not clearly observed in the infrared spectra, there exists a shoulder at around 1240 cm$^{-1}$, close to the Si-O TO stretching mode (1097 cm$^{-1}$) which is attributed as the out-of-phase Si-O stretching LO mode. However, Si-O LO mode will not be the focus of this experiment.

As shown in Figure 4.9, the Si-O stretching TO mode is observed at 1094 cm$^{-1}$, which is a blue shift of around 7 cm$^{-1}$ (larger than the TO mode of 1087 cm$^{-1}$ in the 230 Å SiO$_2$ film as described in Section 4.3). The blue shift of the TO absorption mode from 1072 cm$^{-1}$ to 1090 cm$^{-1}$ for samples varying in thickness from 0.05 μm to 1 μm has been reported elsewhere and was described as a relaxation of bond strain as the film thickness increases [94]. A redshift (lower vibration frequency) however, is an indication of a highly strained SiO$_2$ region at the interface [81]. This region is a result of thermal oxidation process, since the SiO$_2$ occupies a 120 % larger molar volume than the Si consumed to grow it. The complete strain relaxation is prevented by the oxide on top of it.

The effect of such interfacial strain on the infrared spectrum are approximated using the central force model, which describes the strain as a decrease in the average tetrahedral Si-O-Si bond angle, $\theta$ [95]. The central force network model described the TO frequency, $\nu_{TO}$ as shown in equation (4.10) [95]:

$$
\nu_{TO} = \nu_0 \sin \frac{\theta}{2}
$$

(4.10)
Where $\nu_0$ is the frequency of unstrained bulk silica, and $\theta$ is the average tetrahedral bond angle in $\alpha$-SiO$_2$, which is 144°.

It should be noted that the Si-O stretching TO frequency, $\nu_{TO}$ is a function of temperature. Theoretical calculations and experimental work (see Figure 4.10) conducted by Ossikovski et al. [96] showed that the position of the Si-O stretching TO mode in the infrared spectrum is due to anomalous dispersion in the refractive index in the region of the absorption band. This is based on the dispersion distortion effect theory, where the thickness-dependent frequency shifts of the TO and LO modes in $\alpha$-SiO$_2$ films on silicon substrates could be due to optical effects [83]. Thus, in order to quantify the measure of strain of the Si-O bonds, the frequency of unstrained bulk silica, $\nu_0$ has to be determined based on the theoretical value of $\nu_{TO}$.

The amount of strain in the SiO$_2$ can be determined using the steps described below:

1) Obtain the theoretical TO frequency (from Figure 4.10) for the particular thickness based on calculations by Ossikovski et al. [96].

2) Determine the frequency of unstrained glass, $\nu_0$

3) Compare the calculated Si-O bond angle using the measured TO phonon mode

For example, in the e-beam deposited 550nm thickness SiO$_2$ sample, the theoretical TO frequency corresponding to the thickness is 1120 cm$^{-1}$. The frequency of unstrained glass, $\nu_0$ is calculated to be 1177.66 cm$^{-1}$ (using the ideal bond angle of 144° and the theoretical TO frequency of 1120 cm$^{-1}$). The measured TO frequency for the 550nm thick SiO$_2$ is 1094 cm$^{-1}$. This corresponds to a bond angle of 136.54 cm$^{-1}$, which indicates a compressive strain of 7.45° in the Si-O bond.

The measure of strain in the SiO$_2$ film can be approximated by comparing the distance between theoretical Si-Si bond length and that due to compressive strain. According to Lucovsky et al. [97], compressive strain is mostly affected by change of the Si-Si bond distance and not the Si-O bond length [97]. The Si-Si distance, $d_{Si-Si}$ is directly related to the Si-O-Si bond angle by the relationship [97]:

76
\[ d_{\text{Si-Si}} = 2 \cdot r_0 \sin \left( \frac{\theta}{2} \right) \]  

(4.11)

Where \( r_0 \) and \( \theta \) are the Si-O bond length and bond angle respectively. Recall that the ideal Si-O bond angle is 144°.

Thus, we can obtain the strain \( \varepsilon \) in the SiO\(_2\) film by correlating the difference between the experimental SiO\(_2\) film’s Si-O bond length and the theoretical Si-O bond length as shown in equation (4.12)[98]:

\[ \varepsilon = \frac{d_{\text{Si-Si}}}{(d_{\text{Si-Si}})_0} - 1 \]  

(4.12)

Thus, the average strain in the 550nm thick e-beam deposited SiO\(_2\) film is:

\[
\begin{align*}
(d_{\text{Si-Si}})_0 &= 2 \cdot r_0 \sin(144/2) \\
(d_{\text{Si-Si}})_{\text{film}} &= 2 \cdot r_0 \sin(136.54/2)
\end{align*}
\]

Thus

\[
\varepsilon = \frac{2 \cdot r_0 \sin(136.54/2)}{2 \cdot r_0 \sin(144/2)} - 1 = \frac{0.9289}{0.951} - 1 = -0.0233
\]

However, it has been reported that the difference in the peak shift in the spectra is also results from structural change in the oxide and not from some optical effects relating only to the thickness of the SiO\(_2\) layer [82, 89]. It has been described by Pai et al. [99] that the vibrational peak shift of the Si-O stretching TO mode is due to sub-stoichiometric formation of silicon suboxide (SiO\(_x\)). In silicon suboxides (SiO\(_x\)) where \( x \) is less than 2, the Si-O stretching mode shifts from ~980 cm\(^{-1}\) for \( x=1 \) to ~1080 cm\(^{-1}\) for \( x=2 \) [99]. There has not been a clear understanding and agreement for the shifts of the Si-O stretching TO vibrational modes. Thus, in our study of the SiO\(_2\) film due to PECE effect, we will ignore the vibrational shift due to sub-stoichiometric formation because our oxide is high-quality stoichiometric thermal oxide and we will focus on the vibrational shift due to strain in the oxide film in the Si-O stretching TO mode.
4.5 Effects of Process Parameters on the RTP-induced PECE effect

4.5.1 Introduction

Initial experimental studies on RTP-induced PECE effect were performed using the RTP equipment at University of Louisville [73]. In 2006, the exactly same model of the RTP equipment (Modular Process RTP-600S) was purchased at University of Kentucky. In order to reproduce the results obtained using the newly purchased RTP equipment, the exact conditions were used to mimic the experiments carried out at University of Louisville, i.e. RTP performed at 1050°C in N₂ ambient. However, leakage current reduction for MOS capacitor as was observed in the previous works using the RTP setup at University of Louisville [72, 100] could not be reproduced at University of Kentucky (see Chapter 7: section 7.2). Later Chen [101] figured out this puzzling issue and pointed out that trace O₂ is needed in order to observe the leakage reduction. As reported previously, the best result was near 5 orders of magnitude reduction of leakage current [72, 100]. Why couldn’t we obtain the previous best results? Thus, FT-IR measurements were performed using the newly purchased RTP equipment at University of Kentucky in order to elucidate this problem. The samples that were used in the FT-IR characterization are N (100) orientation silicon wafer with dopant density of 1×10¹⁹ cm⁻³. The SiO₂ film was grown thermally in a quartz furnace at 900°C. The RTP conditions and experimental setup was described in detail in Chapter 3.

4.5.2 Effect of the N₂ ambient on the absorption intensity

As pointed out by Chen [101], RTP-annealed samples at 1050°C in pure N₂ does not exhibit any leakage current reduction. Instead, this process creates the inverse where the samples produce higher tunnel leakage current. Thus, it is interesting to understand this phenomenon based on analysis using FTIR spectra measurements. Figure 4.11 shows the infrared spectrum in the range of 400 cm⁻¹ to 600 cm⁻¹ in the Si-O rocking region. Both oxide samples exhibit the same thickness (~233 Å) as measured using a spectroscopic ellipsometry (J.A. Woolam model M-500V) with a fixed refractive index of 1.455. The absorption intensity of the RTP-annealed sample in N₂ ambient at 1050°C for 2 mins showed only a 17.8 % increase as compared to the control sample which contradicts the
value (~50% increase of absorption intensity) reported in our previous work [73]. In addition, it has also been reported that SiO₂ films grown at higher oxidation temperature exhibits an increase in the absorption intensity as well due to relaxation of bond strain in the SiO₂ interface [80]. However, the absorption intensity was increased by only ~5% (between 800 °C and 1000°C oxidation temperature) and was observed at the Si-O stretching mode (~1000 to 1200 cm⁻¹ wavenumber), not at the Si-O rocking mode (~400 to 500 cm⁻¹). Thus, we can conclude that the increase in the absorption intensity was partially dependent upon the processing temperature.

As noticed by Chen [101], there exists a slight regrowth of the SiO₂ film after RTP processing (~1Å). The samples that underwent RTP processing using the equipment at University of Kentucky however did not exhibit any oxide regrowth. This may suggest that the large increase in absorption intensity of the Si-O rocking mode after RTP processing at University of Louisville may be due to oxide regrowth. The RTP annealing experiments in a dilute O₂ ambient in Helium (He) instead of in pure N₂ were proposed by Chen [101]. Dilute O₂ in He ambient was chosen in order to eliminate any concern that the SiO₂ film might be nitrided.

4.5.3 Effect of thickness of SiO₂ on the absorption intensity

The thickness of the oxide film is known to correlate with the increase in the absorption intensity of infrared spectra of SiO₂ films as reported elsewhere [85, 102]. Thus, it is of vital importance to separate the absorption intensity increase due to the enhanced coupling between the Si-Si phonon mode and the Si-O rocking mode from that due to an increase in the oxide film thickness.

Silicon oxide films with varying thickness ranging from 230 to 275 Å as determined using ellipsometry measurements were grown at 900°C in pure O₂. The dependence of the film thickness and the absorption intensity of Si-O rocking mode are shown in Figure 4.12. The samples were measured at least 10 times and the average of the absorption intensity was used. A linear regression formula for the SiO₂ film in the range of 230 to 275 Å was obtained by correlating the film thickness to the absorption intensity as shown in
equation (4.13) and in Table 4.2. It should be noted that these values are based on the FT-IR instrument used specifically at University of Kentucky, and should not be used universally as different instrument will produce distinct values.

\[ Absorption \ Int = -0.007622 + (5.7773\times10^{-5} \times SiO_2 \ thickness) \]

(4.13)

Table 4.2: Dependence of Si-O Rocking Mode Absorption Intensity on SiO₂ Thickness

<table>
<thead>
<tr>
<th>Thickness (Å)</th>
<th>Si-O Rocking Absorption Intensity</th>
</tr>
</thead>
<tbody>
<tr>
<td>230.00</td>
<td>0.0056658</td>
</tr>
<tr>
<td>232.00</td>
<td>0.0057813</td>
</tr>
<tr>
<td>234.00</td>
<td>0.0058969</td>
</tr>
<tr>
<td>236.00</td>
<td>0.0060124</td>
</tr>
<tr>
<td>238.00</td>
<td>0.0061280</td>
</tr>
<tr>
<td>240.00</td>
<td>0.0062435</td>
</tr>
<tr>
<td>242.00</td>
<td>0.0063591</td>
</tr>
<tr>
<td>244.00</td>
<td>0.0064746</td>
</tr>
<tr>
<td>246.00</td>
<td>0.0065902</td>
</tr>
<tr>
<td>250.00</td>
<td>0.0068213</td>
</tr>
<tr>
<td>255.00</td>
<td>0.0071101</td>
</tr>
<tr>
<td>260.00</td>
<td>0.0073990</td>
</tr>
<tr>
<td>265.00</td>
<td>0.0076878</td>
</tr>
<tr>
<td>270.00</td>
<td>0.0079767</td>
</tr>
<tr>
<td>275.00</td>
<td>0.0082656</td>
</tr>
</tbody>
</table>

4.5.4 Effect of trace O₂ on the absorption intensity

RTP annealing of SiO₂ film (~235 Å) in dilute O₂: He ambient was performed in order to verify the hypothesis that the mechanism for large increase of the absorption intensity in the Si-O rocking mode is due to a slight regrowth of the oxide film.
Figure 4.13 shows the infrared spectrum of SiO₂ samples processed under varying RTP conditions. The samples were labeled 1 to 4 with the RTP conditions listed below:

a) Sample 21 - RTP at 1080 °C for 2 minutes in pure He ambient
b) Sample 22 - RTP at 1100 °C for 30 seconds in pure He ambient
c) Sample 23 – RTP at 1080 °C for 2 minutes in dilute O₂: He ambient (5 % O₂)
d) Sample 24 – RTP at 1100 °C for 30 seconds in dilute O₂: He ambient (8 % O₂)

Samples 23 and 24 exhibit oxide regrowth of 1 to 3 Å respectively, while the oxide thickness of samples 21 and 22 remained unchanged (235 Å). As expected, samples annealed in pure He ambient exhibit only a slight increase in the absorption intensity of the Si-O rocking mode (~14 to 17 %), which is comparable to the results from pure N₂ ambient RTP-annealed condition. Samples annealed in dilute O₂ ambient however, exhibit a much larger absorption intensity increase (between 41 to 42 %) in the Si-O rocking mode as illustrated in Figure 4.14(a). Taking the regrowth of the oxide film into consideration, the increase of the absorption intensity was still astounding (between 36 to 38 %). Although, sample 24 was annealed at a higher temperature (1100 °C) than sample 23 (1080 °C), both samples exhibit almost the same increase in absorption intensity. It is also interesting to note that RTP annealing time is not an important criteria for the enhancement of the absorption intensity as sample 23 (2 minutes) was annealed at a longer time compared to sample 24 (30 seconds). Thus, the important parameter to obtain the PECE effect is a high temperature annealing (> 1050 °C) with a slight regrowth of the oxide film. The Si-O bending could not be determined from the FT-IR spectra as Si-O bending mode is the weakest of the Si-O absorption modes. The Si-O bending mode is usually not visible for films in this thickness range, in addition to the reflectance measurements used, which usually produce weaker absorption intensity. Table 4.3 summarizes the results of the Si-O rocking mode absorption intensity from this experiment.

As shown in Figure 4.14(b), the Si-O stretching TO mode exhibit only a small absorption enhancement (11 %) from the RTP annealing in dilute O₂ ambient. This is expected since the basis for the PECE effect is due to coupling between Si-O rocking mode and Si-Si
phonon mode. Thus, there should not be a large enhancement of the Si-O stretching mode since it is located at around 1000 to 1200 cm\(^{-1}\), which is far from the Si-Si phonon mode (~ 495 cm\(^{-1}\)). We can assume that the slight enhancement of the absorption intensity in the Si-O stretching TO mode is mainly due to the higher annealing temperature as was observed elsewhere [85, 102]. The same argument applies to the Si-O stretching LO mode as well.

Table 4.3: Comparison of Si-O rocking mode absorption intensity for samples subjected to RTP annealing in pure He and dilute O\(_2\) environment.

<table>
<thead>
<tr>
<th>Sample</th>
<th>Absorption Intensity</th>
<th>(T_{ox}) (Å)</th>
<th>% Int increase from control</th>
<th>% Int increase from thickness</th>
</tr>
</thead>
<tbody>
<tr>
<td>Control</td>
<td>0.00587</td>
<td>235</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Sample 21: RTP @ 1080 °C pure He for 2 mins</td>
<td>0.0067135</td>
<td>235</td>
<td>14.4 %</td>
<td>14.4 %</td>
</tr>
<tr>
<td>Sample 22: RTP @ 1100 °C pure for 30 secs</td>
<td>0.006837</td>
<td>235</td>
<td>16.5 %</td>
<td>16.5 %</td>
</tr>
<tr>
<td>Sample 23: RTP @ 1080 °C O(_2)::He (5 %) 2 mins</td>
<td>0.00829</td>
<td>236</td>
<td>41.2 %</td>
<td>38.1 %</td>
</tr>
<tr>
<td>Sample 24: RTP @ 1100 °C O(_2)::He (8 %) 30 secs</td>
<td>0.00833</td>
<td>238</td>
<td>42 %</td>
<td>36 %</td>
</tr>
</tbody>
</table>

The Si-O stretching TO mode is observed at 1087 cm\(^{-1}\) for all the samples (control and RTP). Using the steps formulated in section 4.4, the bond angle calculated is 145.9°, which is more than the ideal Si-O-Si bond angle of 144°. However, as mentioned in Section 4.4, the location/shift of the Si-O stretching TO mode may be caused either by strain/stress in the film or by non-stoichiometry in the film. The most important information that we obtain from the Si-O stretching mode is that all the samples exhibit the same peak position. Thus, the increase in the absorption intensity is not due to a difference of compressive strain in the Si-O bonds or non-stoichiometry after the RTP. Table 4.4 and Table 4.5 summarizes the absorption intensity results for the Si-O stretching TO and
LO modes respectively.

Table 4.4: Comparison of Si-O stretching $TO$ mode absorption intensity for samples subjected to RTP annealing in pure He and dilute $O_2$ environment.

<table>
<thead>
<tr>
<th>Sample</th>
<th>Intensity</th>
<th>$Tox$ (Å)</th>
<th>% Int increase from control</th>
</tr>
</thead>
<tbody>
<tr>
<td>Control</td>
<td>0.0342</td>
<td>235</td>
<td>-</td>
</tr>
<tr>
<td>Sample 21: : RTP @ 1080 °C pure He for 2 mins</td>
<td>0.034286</td>
<td>235</td>
<td>0.25 %</td>
</tr>
<tr>
<td>Sample 22: RTP @ 1100 °C pure for 30 secs</td>
<td>0.036616</td>
<td>235</td>
<td>7 %</td>
</tr>
<tr>
<td>Sample 23: RTP @ 1080 °C O2:He (5 %) for 2 mins</td>
<td>0.038</td>
<td>236</td>
<td>11.1 %</td>
</tr>
<tr>
<td>Sample 24: RTP @ 1100 °C O2:He (8 %) for 30 secs</td>
<td>0.0377</td>
<td>238</td>
<td>10.2 %</td>
</tr>
</tbody>
</table>

Table 4.5: Comparison of Si-O stretching $LO$ mode absorption intensity for samples subjected to RTP annealing in pure He and dilute $O_2$ environment.

<table>
<thead>
<tr>
<th>Sample</th>
<th>Intensity</th>
<th>$Tox$ (Å)</th>
<th>% Int increase from control</th>
</tr>
</thead>
<tbody>
<tr>
<td>Control</td>
<td>0.007276</td>
<td>235</td>
<td>-</td>
</tr>
<tr>
<td>Sample 21: : RTP @ 1080 °C pure He for 2 mins</td>
<td>0.0078535</td>
<td>235</td>
<td>7 %</td>
</tr>
<tr>
<td>Sample 22: RTP @ 1100 °C pure for 30 secs</td>
<td>0.00756</td>
<td>235</td>
<td>0.0284 %</td>
</tr>
<tr>
<td>Sample 23: RTP @ 1080 °C O2:He (5 %) for 2 mins</td>
<td>0.00794</td>
<td>236</td>
<td>9.1 %</td>
</tr>
<tr>
<td>Sample 24: : RTP @ 1100 °C O2:He (8 %) for 30 secs</td>
<td>0.00796</td>
<td>238</td>
<td>9.4 %</td>
</tr>
</tbody>
</table>
4.5.5 Effect of annealing the SiO$_2$ film in conventional furnace

The previous section described the conditions that are used to observe the enhanced absorption of Si-O rocking mode by annealing the SiO$_2$ film in RTP in dilute O$_2$: He ambient. In addition to a trace O$_2$ environment, it is important to understand whether the enhanced intensity absorption of FT-IR spectrum observed is due to high temperature processing only or could be unique to the RTP process. Thus, annealing of SiO$_2$ sample in conventional furnace at high temperature was performed and measured using FT-IR to understand this phenomenon.

The oxide sample of 233 Å was loaded into the furnace at 900 °C and the temperature was ramped up to 1050 °C at 15 °C/minute. Annealing was performed in dilute O$_2$:N$_2$ ambient (5%) for 4 minutes followed by ramping down the temperature to 800 °C before unloading the sample. The ramp down rate is not controllable and depends purely on thermal diffusion. The thickness of the oxide sample was shown to increase by ~ 3 Å after the annealing process.

Figure 4.15 shows the infrared spectrum of the Si-O rocking mode of samples annealed in conventional thermal furnace at 1050 °C for 4 mins in dilute O$_2$:N$_2$ ambient. The Si-O rocking mode was shown to increase by 13% as compared to samples without the annealing process. However, if the increase of the oxide thickness was taken into consideration, the Si-O rocking mode was only enhanced by 8.8 % as shown in Table 4.6. Thus, this shows that PECE effect could only be observed in the RTP and not in a conventional thermal furnace. This could be due to the rapid heating and cooling process that can only be achieved in the RTP.
Table 4.6: Comparison of Si-O stretching TO mode absorption intensity for samples subjected to furnace annealing in dilute O$_2$:N$_2$ at 1050 °C for 4 minutes

<table>
<thead>
<tr>
<th>Sample</th>
<th>Absorption Intensity</th>
<th>Tox (Å)</th>
<th>% Intensity change</th>
</tr>
</thead>
<tbody>
<tr>
<td>Control</td>
<td>0.0056</td>
<td>233</td>
<td>-</td>
</tr>
<tr>
<td>Furnace Annealing at 1050 °C for 4 mins in dilute O$_2$:N$_2$ ambient</td>
<td>0.0063104</td>
<td>236</td>
<td>-13 % from control&lt;br&gt;- 8.8 % thickness increase taken into consideration</td>
</tr>
</tbody>
</table>

4.5.6 Effect of a photoresist developer MF319

In previous studies [72], it was reported that alkali-based chemicals may be detrimental to the PECE effect. Alkali-based developer such as MF-319, which is used in photolithography process for positive photoresist, contains a chemical called TMAH (Tetramethylammonium hydroxide). TMAH however, is commonly used as wet etchant for silicon in MEMS-based devices, in which SiO$_2$ is used as an etching mask layer. The etch rate for TMAH was found to be in the range of 15-80 Å/hour [103]. Thus, it is of vital importance to examine the effect of MF-319 on the RTP-induced PECE effect samples.

The control sample was a 240 Å thick SiO$_2$ film thermally grown at 900 °C, while the RTP samples were subjected to RTP annealing at 1080 °C in dilute O$_2$: He ambient with a re-growth of 2 Å as described in section 4.5.3. The RTP-annealed sample was then subjected to immersion in MF-319 solution for 5 minutes. FT-IR measurements were performed in the Si-O rocking mode absorption region (400 to 600 cm$^{-1}$) using the conditions described in Section 4.2 at an angle of incidence of 65°. The effect of MF-319 on the RTP-induced PECE effect was shown in Figure 4.16. The samples annealed in RTP chamber at 1080 °C in dilute O$_2$: He ambient was shown to exhibit 37% increase of Si-O rocking mode absorption intensity as expected. However, the absorption intensity was shown to decrease by 16.7% after immersing the RTP sample in MF-319. The absorption intensity is still 16.7 % higher than the control sample although the oxide thickness remained unchanged. The RTP-induced PECE effect was reduced due to immersion in MF-
319 solution. Thus, this result showed that conventional developer used in photolithography processing could have an adverse effect on the RTP-induced PECE effect.

Table 4.7: Comparison of Si-O rocking mode at 478 cm$^{-1}$ between control, RTP, and RTP plus MF-319 immersion samples

<table>
<thead>
<tr>
<th>Sample</th>
<th>Intensity</th>
<th>$T_{ox}$ (Å)</th>
<th>% Intensity change</th>
</tr>
</thead>
<tbody>
<tr>
<td>Control</td>
<td>0.0063</td>
<td>240</td>
<td>-</td>
</tr>
<tr>
<td>RTP sample @1080°C in dilute O$_2$:He ambient</td>
<td>0.00864</td>
<td>242</td>
<td>37 %</td>
</tr>
<tr>
<td>RTP sample after immersing into MF-319</td>
<td>0.0074</td>
<td>242</td>
<td>+ 17.5 % from control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>- 16.7 % from pre-MF319</td>
</tr>
</tbody>
</table>

4.6 Conclusion

In this Chapter, the experimental setup used for the FT-IR measurements was described to justify the obtained IR results. The mechanism for generating the Phonon-Energy-Coupling-Enhancement (PECE) effect was studied using FT-IR [73]. The PECE effect could only be observed in samples annealed in RTP chamber at temperatures exceeding 1050 °C for a short period of time in a dilute O$_2$: He ambient. The key parameter for generating the PECE effect is slight regrowth of oxide after RTP processing. We have also shown that conventional furnace annealing could not produce the PECE effect. In addition, regular developer used in photolithography processing such as MF-319 should be avoided as it contained TMAH chemical, which could suppress the PECE effect. These considerations will be used for the ultra-thin oxide MOS capacitor fabrication in Chapter 7.
Figure 4.1  Illustration of Specular reflectance [78]
Figure 4.2  (a) Schematic diagram of beam path for Reflection-Absorption of a relatively thin film measured by Specular Reflectance technique; (b) Electromagnetic field in the $p$ and $s$-polarized component in Specular Reflectance.
Figure 4.3 Comparison of background spectrum of Silicon substrate (N (100), dopant density of $1\times10^{19}$ cm$^{-3}$) with varying angle of incident from 65 to 75°
Figure 4.4  The background spectrum was measured on a Silicon substrate (N (100), dopant density of $1 \times 10^{19}\text{cm}^{-3}$) at angle of incident of $65^\circ$. Minimal level of Carbon Dioxide (CO$_2$) and moisture (H$_2$O) on the background sample detected after N$_2$ purging overnight of the FT-IR instrument.
Figure 4.5  Schematic representation of the vibrational modes of Oxygen (O) atoms with respect to silicon (Si) atom pairs: Stretching, Bending, and Rocking modes
Figure 4.6  Effect of angle of incidence of reflectance measurements on SiO$_2$ on Silicon substrate. The SiO$_2$ film was grown thermally with a thickness of 230 Å as measured using ellipsometer using a fixed refractive index of 1.455.
Figure 4.7 Effect of angle of incidence of reflectance measurements on thermally grown 230 Å SiO$_2$ in the Si-O rocking mode region.
Figure 4.8  (a) Complex refractive index of SiO$_2$ (b) Calculated infrared dielectric constant and energy loss function of SiO$_2$. Optical data were obtained from Handbook of Optical Constants of Solids [92]
Figure 4.9 Absorption spectrum of 550nm e-beam deposited SiO$_2$ film, measured at incident angle of 65°.
Figure 4.10 Comparison of optical model calculation (solid curves) with experiment peak positions of Si-O stretching LO and TO vibrational modes by Ossikovski et al. [96]
Figure 4.11 Absorption intensity comparison of Si-O rocking mode between control sample (SiO$_2$ film thickness of 233 Å) and RTP annealed sample in N$_2$ @ 1050 °C for 2 mins. No regrowth was observed after the RTP annealing process.
Figure 4.12 Dependence of Si-O rocking mode absorption intensity to SiO$_2$ film thickness. The SiO$_2$ film thickness was measured using spectroscopic ellipsometer.
Figure 4.13  Infrared spectrum of RTP annealed SiO2 sample in varying RTP conditions: Sample 21 - RTP at 1080 °C for 2 minutes in pure He ambient; Sample 22 - RTP at 1100 °C for 30 seconds in pure He ambient; Sample 23 – RTP at 1080 °C for 2 minutes in dilute O2: He ambient (5 % O2); Sample 24 – RTP at 1100 °C for 30 seconds in dilute O2: He ambient (8 % O2).
Figure 4.14 Infrared spectrum in the range of: (a) Si-O Rocking, b) stretching TO from the experiments performed in Figure 4.13.
Figure 4.15 Infrared spectrum of Si-O rocking mode of samples annealed in conventional thermal furnace at 1050 °C for 4 mins in dilute O₂:N₂ ambient.
Figure 4.16 Infrared spectrum of Si-O rocking mode of samples subjected to RTP annealed in dilute $O_2$:He ambient and then immersed in MF-319 solution for 5 minutes.
CHAPTER 5
EFFECT OF ENHANCED PHONON ENERGY COUPLING ON THE STRENGTH OF SI-SI BONDS

5.1 Introduction
The FT-IR experiments conducted and explained in Chapter 4 showed that an increase in the absorption intensity of Si-O rocking mode by 40 to 50 % was due to enhanced energy coupling between the Si-O rocking mode and the Si-Si TO phonon modes after proper RTP processing. The increase in the absorption intensity of the Si-O rocking mode was shown to have a beneficial effect on the tunneling current of Si MOS capacitors, where a reduction of 2-5 orders of magnitude of leakage current, $J_G$, could be achieved [73, 104]. In addition, the oxide breakdown voltage increased by 30-40 %, indicating a more robust Si-O bonds [104-106]. The Si-Si TO phonon mode however, could not be fully distinguished in the FT-IR measurements as described in Chapter 4. This is because the signals from the Si substrate were subtracted from the spectra (Si substrate was used as the background spectrum). Si-Si phonon mode at 495 cm$^{-1}$ was however observed by Wei et al. [107] in infrared normal mode transmission measurements of SiO$_2$ film. The Si-Si phonon mode vibration energy was weak and the vibrational frequency is located close to the Si-O rocking mode as measured at 475 to 480 cm$^{-1}$ in Chapter 4. Thus, the increase of the absorption spectrum in the range of 400 to 500 cm$^{-1}$ could also be due to an increase in IR absorption of the Si-Si phonon modes. If there is evidence that the Si-Si bonds are strengthened after proper RTP process, it will be more convincing that the PECE effect plays a major role in leakage current reduction.

In our previous works on thick SiO$_2$ films (>80nm) [108], RTP-induced PECE effect could not be shown. This could be due to the large thickness of the SiO$_2$ layer, which could hinder any microstructure change of oxide by thermal stress when it is too thick. Therefore, it is unlikely to induce any microstructure change of a silicon wafer because it is too thick (~300-500 µm). If the silicon wafer’s breakdown voltage is increased after RTP and deuterium anneals, on which a thin oxide layer is covered, the only explanation to this is that the phonon energy of the Si-Si bonds is coupled to thin oxide as shown
in Figure 5.1. It should be noted that the PECE effect experiments performed in this work was performed using the RTP equipment at University of Louisville. Thus, there might be some trace O₂ present in the system as was described in the FT-IR experiments in Chapter 4. However, the succeeding sections will show that the trace O₂ content in the RTP chamber does not affect the PN junction breakdown voltage measurements.

5.2 Experimental Setup

A special PN junction diode device was designed and fabricated to study the coupling from the Si-Si bonds to the Si-O bonds as shown in Figure 5.2. On one side of the substrate is a layer of thermally grown oxide and on the other side are the PN junction diodes. The process steps involved in the fabrication of the PN junction diode are listed below and shown schematically in Figure 5.3.

1) The device fabrication process started with growth of a thick thermal field oxide (5000 Å) on the p⁺ substrate (ρ=0.001 Ω·cm). The dopant density of the wafer (Nₐ = 3.8×10¹⁸ cm⁻³) is measured by first obtaining the resistivity using a four-point probe system and correlating it to the “dopant density vs. resistivity” chart. The “dopant density vs. resistivity” chart can be obtained in Ref [109].

2) 3000 Å thickness of SiO₂ layer was grown as the masking layer for the Phosphorus diffusion process. The contact region for the diffusion process was defined using photolithography process and etched in BOE. Note that the oxide on the back of the wafer is etched as well.

3) Diffusion of the N⁺ region was performed using spin-on dopant phosphorus source (Filmtronics P509) in a thermal furnace. The dopant source was spin-coated on the wafer and cured at 150 °C for 10 min on hot plate. Constant source diffusion was carried out at 1000 °C for 1 hour at 10% O₂ and 90% N₂ and the n⁺ region (n=1×10²¹ cm⁻³) of ~0.5 μm deep was formed on the p⁺ substrate.

4) After opening windows for the p⁺ substrate region and removing the field oxide on the front side using buffered-oxide etch (BOE), a thin oxide of 150 Å was thermally grown on the wafer.

5) The PN junction structure on the back side of the wafer was etched in BOE to re-
move the additional 150 Å oxide, while the thin oxide (150 Å) on the front side of the wafer was protected using hard-baked photo resist.

6) RTP at 1050°C in pure nitrogen was then carried out for 4 min.

7) Ohmic contacts were formed by lithography using negative photo resist (Microchem SU-8), thermal evaporation of Al, and post metal annealing in D₂ at 450°C for 30 min. In order to rule out any effect that may be caused by dopant redistribution in RTP, an identical sample that went through the same fabrication processes except for the RTP step was also annealed in furnace at 1050°C in N₂ for 4 min (referred to as furnace anneal) for comparison.

5.3 Results and Discussions

Figure 5.5(a) shows I-V characteristics of a forward-biased PN junction diode in semi-log scale. For V<0.7V, the current exhibits an exponential relationship with the forward-biased voltage. There is not any difference between the control sample, the furnace annealed and the RTP-annealed samples in the exponential regime. For V>0.7V, the current of the RTP- and furnace-annealed samples increases slower than that of the control sample because of the large contact resistance induced by RTP and furnace anneal. In order to study the contact resistance issue in more detail, I-V curves on the linear scale for the forward bias are shown in Figure 5.4(b). The diode can be modeled as an ideal diode with a series resistance which may be caused by dopant redistribution or non-ideal contact after RTP and furnace anneal. The voltage applied across the diode can be expressed as V≈V_d+IR_s, where V_d is the turn-on voltage of the ideal diode (~0.7V) and R_s is the series resistance. The series resistances of the control, the RTP-annealed, and the furnace-annealed samples are ~ 10 Ω, 40 Ω, and 75 Ω separately as shown in Figure 5.5. It is the series resistance that causes the deviation of I-V curves away from the ideal exponential relationship. The impact of the series resistance on I-V curves is only effective at large current (>1 mA). For current lower than 1 mA, the deviation is very small. This can be explained using the above simple diode model. The voltage deviation from the ideal diode can be expressed as ΔV=IR_s. For I= 1 mA, ΔV is only 10 mV for the control sample, 40 mV for the RTP-annealed sample, and 75 mV for the furnace-annealed sample. Excluding the impact of the series resistance, it is clearly shown in Figure 5.4 that the I-V
curves for all samples in the forward-bias voltage are identical.

It is more interesting to examine the breakdown voltage of the PN junction diode as shown in Figure 5.6, where the breakdown voltage of the diode is increased after RTP anneal. The breakdown voltage of the control sample is exactly the same as that of the furnace-annealed samples despite large contact resistance of the furnace-annealed sample. Figure 5.6(b) shows the breakdown voltage, I-V curves in semi-log scale in order to examine the breakdown phenomenon. It can be seen that the breakdown voltage is increased by 0.3 V after RTP. After breakdown the current increases very sharply even on the log scale, suggesting that it is avalanche breakdown. From Figure 5.6, it can be seen that the breakdown voltage is 7.4 V for the control and furnace annealed-samples, and 7.7 V for the RTP-annealed sample.

The question remains: Is the voltage increase really due to stronger Si-Si bonds or because of reduced dopant concentration or large contact resistance after RTP? In order to answer this question, the same control sample was annealed in a conventional thermal furnace using the same parameters as those of RTP (1050°C in N₂ for 4 minutes). From Figure 5.6, the breakdown voltage between the control sample and the furnace-annealed sample is identical. This may suggest that the dopant redistribution after thermal anneal is very small, because the breakdown voltage is strongly dependent on the dopant concentration. In order to determine the dopant density in the diffused region (N⁺), a reverse bias capacitance measurement at high frequency, 100 kHz was performed. The junction capacitance is related to the applied bias voltage by equation (5.1) [110]:

\[
\frac{1}{C^2} = \frac{2(V_{bi} - V)}{A^2 q \varepsilon N_{eff}}
\]

(5.1)

Where \( C, V_{bi}, V, A, q, \varepsilon, N_{eff} \) are junction capacitance, built in potential, area, electronic charge, dielectric constant of silicon and effective dopant density.

\( N_{eff} \) can be described as shown in equation (5.2):

\[
N_{eff} = \frac{N_a N_d}{N_a + N_d}
\]

(5.2)
The plot of “1/C² vs. V” is shown in Figure 5.7. It should be noted that the slope for all the samples; control, annealed in RTP, and annealed in thermal furnace are similar. Thus, we assume that the slopes are identical and was calculated to be \( \sim 1.9 \times 10^{20} \). The area of the PN junction diode is \( 4 \times 10^{-4} \text{ cm}^2 \), in which the effective dopant density, \( N_{\text{eff}} \) of \( 3.9 \times 10^{17} \text{ cm}^{-3} \) is calculated from equations 5.1. We can then obtain the dopant density in the diffused region, \( N_d \) (\( 4.48 \times 10^{17} \text{ cm}^{-3} \)) from the effective dopant density value from equation 5.2 since the substrate dopant concentration, \( N_a \) (\( 3 \times 10^{18} \text{ cm}^{-3} \)) is known.

The theoretical breakdown voltage of the PN junction diode can then be obtained by the dopant density in the diffused region, \( N_d \) from the equation (5.3):

\[
V_{\text{BD}} = \frac{\varepsilon E_{\text{crit}}^2}{2qN_d}
\]  

(5.3)

Where the critical electric field, \( E_{\text{crit}} \) can be obtained from the relation of \( E_{\text{crit}} \) to dopant density as shown in Figure 5.8 [110].

The critical electric field of silicon at a dopant density of \( 4.48 \times 10^{17} \text{ cm}^{-3} \) is around \( 9.5 \times 10^5 \text{ V/cm} \). Thus, the breakdown voltage is:

\[
V_{\text{BD}} = \frac{11.9 \times (8.854 \times 10^{-14} F/cm^2)(9.5 \times 10^5 V/cm)^2}{2(1.6 \times 10^{-19} C)(4.48 \times 10^{17} \text{ cm}^{-3})} = 6.64V
\]  

(5.4)

The theoretical breakdown field is similar to the breakdown voltage as observed. The difference in the calculated and measured breakdown voltage could be due to the non-linear slope of the \( 1/C^2 \) vs. \( V \) plot. However, the important point obtained from the \( 1/C^2 \) vs. \( V \) figure was that the slopes of all the samples are identical. Thus, the increase of the breakdown voltage of the RTP-annealed sample is not due to dopant redistribution. In addition, according to Sze [111], for junctions with breakdown voltages in excess of \( 6E_g/q \), i.e. 6.6 V, the mechanism is avalanche multiplication. Therefore, the breakdown field in the fabricated PN junction diodes is due to avalanche multiplication. It is also important to note that the assumptions made in the theoretical calculations are based on junction but the fabricated PN junction diode structure are actually between the abrupt junction and a linear graded junction due to diffusion [111].
We have shown that the dopant redistribution is not a factor in the increase of the breakdown voltage in the RTP-annealed PN junction devices. In addition, the contact resistance also does not affect the breakdown voltage. This can be explained using the same argument for the forward bias voltage. The voltage change due to the contact resistance is expressed as $\Delta V = IR_s$ and can be estimated using the $R_s$ values obtained in the forward bias measurements. As shown in Figure 5.6(b), the reverse bias current varies from $10^{-7}$ A to $10^{-4}$ A at the onset of breakdown. This leads to a change of voltage, $\Delta V = 1 \mu V - 1 \text{mV}$ for the control sample, $4 \mu V - 4 \text{mV}$ for the RTP annealed sample, and $7.5 \mu V - 7.5 \text{mV}$. All of them are much less than 0.3 V (300 mV) and thus are negligible. Therefore, the contact resistance does not play any role in breakdown voltage increase. The contact resistance plays a significant role only when the current is large than 0.1 mA. Saturation of I-V curves on the log-scale for $I > 0.1$ mA in Figure 5.6(b) confirms the above observation. Therefore, neither the dopant redistribution nor the increase in contact resistance caused the increase in breakdown voltage. The sole reason for the increase in breakdown voltage of the diode is due to its intrinsic properties, i.e. stronger Si-Si bonds after RTP.

### 5.4 Conclusions

FT-IR measurements for thick SiO$_2$ films (>80 nm) showed that the PECE effect could not be observed [108]. Therefore, it is unlikely that RTP can induce the structure change on the thick Si substrate (0.3 mm). Thus, the strengthening of Si-Si bonds as measured using breakdown voltage of PN junction diodes performed in this Chapter could be caused by the thin oxide (15 nm) on the other side of the diode. This may suggest that phonon energy is coupled from the Si-Si bonds to Si-O bonds after RTP annealing. As stated earlier, this work was performed using the RTP equipment at University of Louisville where there might exists a small leakage of air into the chamber. This was explained in the FT-IR experiments performed in Chapter 4. However, the presence of O$_2$ in the system does not affect the increase of the PN junction breakdown voltage since the slight increase of the contact resistance does not play a significant role.
Figure 5.1  Schematic of phonon energy coupling from Si-O bonds to Si-D, and Si-Si bonds (Open block arrows) and that from Si-Si bonds to Si-D and Si-O bonds (Solid block arrows).
Figure 5.2  Schematic of a special PN junction diode with oxide of 15 nm on the other side of the substrate. The breakdown voltage of the diode was studied to show the strength of the Si-Si bonds of the substrate.
Figure 5.3 Fabrication procedure of novel PN junction structure used for PECE experiments.
Figure 5.4  I-V characteristics of the forward-biased PN junction diode in:
(a) log scale   (b) linear scale
Figure 5.5  Comparison of contact resistance measurements between control, furnace annealed (1050 °C), and RTP annealed (1050 °C). The control sample exhibit lowest contact resistance, followed by the RTP annealed and the furnace annealed sample.
Figure 5.6 I-V characteristics of the reverse-biased PN junction diode in (a) linear scale, and (b) log scale
Figure 5.7 Comparison of $1/C^2$ vs. Applied Voltage, V measurements between control, furnace annealed (1050 °C), and RTP annealed (1050 °C) sample to obtain effective surface dopant density, $N_{eff}$. 
Figure 5.8  \( E_{\text{crit}} \) vs. dopant density [111]
CHAPTER 6
BI-LAYER RESIST FABRICATION PROCEDURE: RELIABLE OBSERVATION OF LARGE LEAKAGE CURRENT REDUCTION

6.1 Introduction

Advanced metal-oxide-semiconductor (MOS) devices need extremely thin gate silicon oxide dielectrics (<15Å). Transistors with ultra thin oxides operate in a regime in which direct quantum mechanical tunneling dominates the gate leakage mechanism. Currently, the industry uses alternative high permittivity (high-k) gate dielectrics such as HfO₂ and HfSiON (due to thicker physical dielectric layer) to circumvent the gate leakage problem. However, an interfacial SiO₂ layer (5-6Å) exists between the high-k dielectric and Si to maintain a good interface. The interfacial layer will reduce the equivalent oxide thickness (EOT) Therefore any improvement of leakage current of SiO₂ would be very helpful to MOS transistors.

Recently we discovered a new effect, phonon-energy coupling enhancement (PECE) using Fourier transform infrared (FTIR) spectroscopy, leading to reduction of quantum tunneling current of SiO₂ by 2-4 orders of magnitude [37, 61, 72, 106, 112, 113]. It is suggested that reduction of tunneling current is probably caused by energy-band-structure change of SiO₂ after proper rapid thermal processing (RTP) due to enhanced phonon-energy coupling between Si-O rocking mode and Si-Si TO phonon mode (~460 cm⁻¹). Because of the nature of the phonon coupling, any attack of the SiO₂ structure by chemicals and plasmas may result in partial loss of the PECE effect [37]. Alkaline-based chemicals and plasmas must be avoided, including regular photoresist developer and sputtering deposition as shown in the FT-IR work discussed in Chapter 4. In the past, we patterned Al gate metal by evaporation of Al through shadow masks [37, 61, 72, 106, 112, 113]. This may produce unreliable results because the area of MOS capacitors varies during evaporation through shadow masks at different angles across a large substrate. A new fabrication procedure with a new gate material has to be developed to reliably observe the PECE-effect-induced leakage current reduction. In this paper, we will present a new lithographic fabrication procedure using Ni as a gate metal, in which bilayer of SU-
8/S1813 resist is used.

6.2 Problems for Al-Gate MOS Capacitors with Ultrathin Oxide

In our previous works [37, 61, 72, 106, 112, 113], in order to avoid regular photoresist and sputtering deposition we patterned Al gate metal by thermal evaporation of Al through shadow masks to fabricate MOS capacitors. Post-metal annealing (PMA) of MOS capacitors in forming gas were usually performed to ensure low interface trap density, $D_{it} (<10^{12} \text{ cm}^{-2} \text{ eV}^{-1})$ and good back Ohmic contact. However, Al is known to diffuse through ultra thin oxides (<30 Å) at PMA temperatures (~450 °C), causing short-circuits in the devices. This causes unreliable results and low yield (20-30%) of devices. In order to prevent short-circuiting in our previous works, back Al contact was formed first, followed by annealing in forming gas ambient. Finally, Al front gate was defined using shadow mask by thermal evaporation without PMA process. Using this procedure, we obtained devices with a yield of over 90%. However, there is a cost for this process, i.e. capacitance-voltage (C-V) curves are no longer correct. Figure 6.1 shows experimental C-V curves (measured at 100 kHz) of Al/SiO$_2$/n-Si MOS capacitors fabricated without PMA. The extracted experimental accumulation capacitance value (37 Å) using Berkeley quantum (QM) simulation program is only ~70% of the ideal value (24 Å) measured using spectroscopic ellipsometer (J.A. Woolam model M-2000V). It is very important to analyze why there is such a large discrepancy between the ideal and the experimental value. We propose a theoretical model to explain the discrepancy as follows. Without performing PMA, the Al gate may not adhere well to the oxide, creating an air gap between Al and SiO$_2$ as shown in Figure 6.2. The air gap and oxide capacitances per unit area are given by equations (6.1) and (6.2):

$$C_d = \frac{\varepsilon_0}{d} \quad (6.1)$$

$$C_{ox} = \frac{3.9\varepsilon_0}{T_{ox}} \quad (6.2)$$
The total capacitance is the series combination of the air gap capacitance and the oxide capacitance is shown in equation (6.3).

\[ C = C_{ox} / \left( 1 + \frac{3.9d}{T_{ox}} \right) \]  

(6.3)

Figure 6.3 shows effect of air gap thickness on \( C/C_{ox} \) for oxide thickness of 15-30 Å. It can be seen that the accumulation capacitance decreases rapidly with increase in the air-gap thickness. For oxide of 20Å, an air gap of only 2Å may cause the total capacitance to decrease to \( \sim 70\% \) of its ideal value (See Figure 6.3). This is consistent with the discrepancy of \( \sim 70\% \) in Figure 6.1. Based on the above theory, if the air gap can be closed \((d=0)\), the ideal capacitance value can be obtained. We believed that the PMA step is necessary to eliminate the air gap between the Al metal and the dielectric layer. This will be confirmed later using C-V measurement. In addition, the top electrode for our MOS capacitor was defined using shadow mask evaporation of Al using thermal evaporator, in which slight variations of device area could significantly alter the capacitance values. Thus, the area of the devices has to be determined individually, which makes the extraction of the oxide thickness difficult and unreliable.

6.3 Problems for Fabrication of Ni Gate

It is necessary to choose a stable metal gate which will not diffuse through the thin oxide layer at PMA temperature \( \sim \)450 °C. This requirement could be fulfilled using Nickel as the top gate electrode because of its excellent thermal stability (low/negligible diffusion through SiO\(_2\) at PMA temperature, <500 °C [114]). However, Ni could only be deposited either using either e-beam evaporator or sputtering because of its high melting temperature. The Plasma used in sputtering is not only detrimental to the PECE effect [72] but can also damage thin oxides by energetic ion bombardment [115]. Thus, we chose e-beam evaporation of Ni gate metal and patterning using a lift-off process.

The choice of resist for the lift-off experiment is also critical to our experiments because alkali-based chemicals are also harmful to the PECE effect [72]. MF-319, developer for a
regular positive resist Microposit S1800 may not be used. This is because MF-319 contains TMAH (Tetramethylammonium hydroxide, (CH₃)₄NOH). Etch rate of SiO₂ in TMAH is low, ~15-80 Å /hour, depending on concentration of TMAH and temperature of solution [116]. However, in the case of ultra thin oxides, etch rate of only a few monolayer could have detrimental effects on the oxide quality. Therefore, we chose an all organic-based resist and developer, SU-8. However, there is another problem for Ni gate fabrication. Because of its high melting point, Ni can only be deposited using electron-beam evaporation, where the heat from the source causes a reflow of SU-8 resist so that the “lift-off” process is very difficult.

6.4 Bi-Layer Resist Fabrication Procedure

A key process step in a successful “lift-off process” is an undercut resist profile. The solution is to have an intermediate layer between the resist and the substrate to ensure the undercut profile. To fulfill this requirement, we have developed a bi-layer resist lift-off process utilizing Microposit S1813 positive resist as the intermediate resist layer as shown in Figure 6.4. Since the SU-8 2001 developer consists of 98% 1-Methoxy-2-propyl acetate (C₆H₁₂O₃), which is a solvent for the Microposit S1800 series resist, no additional developer is needed to develop the bottom lift-off resist layer (S1800 series resist). The resist however, has to be “semi-cured” to ensure that the developer does not completely remove the resist layer. The “semi-cured” process is a 130 °C bake for 60s on a hot plate. The detailed lift-off process is shown in Figure 6.4.

Two pieces of SiO₂ samples cut from the same oxide wafer with Tₒₓ of 20-24Å were used. One piece was used as a control sample, while the other one was subjected to rapid-thermal processing at 1120°C in helium with ~300-600 ppm O₂. In order to accurately control the oxygen concentration, a trace oxygen analyzer (Alpha Omega Series 3000) with a range of 1-10000 ppm was installed before the inlet of the gas line. The RTP time can be chosen so that the oxide regrowth was ~1-2Å, measured using ellipsometry (J. A. Woolam M3000V). After RTP, both samples were fabricated using the bi-layer resist process. The first resist layer, S1813 resist, was spin coated at a speed of 2000 rpm and cured by baking at 130°C. This step is important to ensure that the developer does not
completely remove the resist layer in final developing step. The next step entails the coating of SU-8 2001 resist at 3000 rpm and soft baking on a hot plate at 70°C and 120°C for 2 minutes respectively. The resist was exposed using an i-line exposure at a dosage of 90mW/cm² followed by post-exposure bake at 70°C and 120°C for 2 minutes respectively. The development of the resist was carried out using SU-8 developer for 60 seconds followed by a quick rinse in IPA and dried using nitrogen blower. The undercut profile is clearly seen in the image of scanning electron microscopy (SEM) as shown in Figure 6.5. A ~100 nm-thick Ni film was deposited on the patterned resist by electron-beam evaporation and lifted off in SU-8 remover (Remover PG) heated at 80 to 100°C. It should be noted that samples have to be loaded into the vacuum chamber within 10 minutes after development. Otherwise, the Ni gate will peel off. After covering the front electrodes using hard-baked S1813 resist at 140°C for 5 minutes, the back oxide was completely etched using BOE. The final steps consists of removing the protective front resist using Microposit 1165 resist remover and subsequently annealing at 450°C in forming gas for 30 minutes (5% H₂: 95% N₂).

6.5 Results and Discussion:
Figure 6.5 shows the SEM micrograph of the bi-layer resist undercut profile obtained in this study. It is noted that there were intermixing of the resists, so that individual resists could not be distinguished in the SEM image. However, as seen in the figure, the undercut profile was created. In addition to the undercut, another key process step, described as follows, has to be used to ensure a successful lift-off. After development of the bi-layer resist, samples have to be loaded into the vacuum chamber in less than 15 minutes, otherwise, Ni electrodes will be peeled off during the final lift-off step in Remover PG. The detailed mechanism is not understood. It seems that after the development process there might be some organic monolayer still present. After exposure in air for over 15 minutes, it might react with some element in air so that it becomes a barrier layer for Ni to diffuse to the surface of the oxide of the substrate. If samples are loaded in less than 15 minutes, Ni atoms can penetrate through the monolayer during e-beam evaporation, so that it adheres very well on the gate dielectric during the final lift-off step.
MOS capacitors were fabricated using the above bi-layer resist process and their electrical characteristics were measured, including current-voltage (I-V) and capacitance-voltage (C-V) curves. Figure 6.6 shows the C-V curves at 100 kHz of a Ni-gate MOS capacitor with $T_{\text{ox}}$ of 21 Å after post-metal anneal (PMA). The equivalent oxide thickness (EOT), the flatband voltage ($V_{\text{FB}}$), and doping concentration can be obtained using experimental C-V curves and theoretical C-V curves simulated by Berkeley Quantum (QM) simulator. It can be seen clearly that after PMA the C-V curve is the same as that of the ideal one simulated based on the oxide thickness obtained using ellipsometry. This confirms that the discrepancy of C-V curves shown in Figure 6.1 is truly caused by the air gap between the metal gate and oxide and the oxide thickness measured using ellipsometry is very accurate for $T_{\text{ox}}$>20Å.

In order to show its utility for reliable observation of leakage current reduction, we fabricate Ni-gate MOS capacitors with both control oxide ($T_{\text{ox}}$=24Å) and the RTP-processed oxide. The RTP processing was carried out at 1120°C in helium containing trace oxygen (~300-600 ppm). As shown in Figure 6.7, the leakage current of the control oxide sample is $\sim1.0\times10^{-2}$ A/cm² at $V_{\text{G}}-V_{\text{FB}} = 1$V, which is comparable with that reported in the International Technology Roadmap for Semiconductors (ITRS) [5]. After RTP at 1120°C in helium containing trace oxygen, leakage current density is reduced by nearly 4 orders of magnitude. In order to accurately determine the EOT, high-frequency (100 kHz) C-V curves of the devices were measured. Figure 6.8 shows the high frequency (100 kHz) measurements of the MOS capacitor device with circular dimensions. The theoretical C-V curves obtained by the Berkeley QM simulator are also shown in Figure 6.8. The EOT of the control oxide is 24 Å, which is the same as that obtained using ellipsometry. The EOT of the RTP processed sample is 26 Å. There is $\sim2$ Å oxide regrowth. Slight oxide regrowth is the key factor for observation of the large leakage-current reduction [112]. The EOT extracted from the experimental C-V curves using the Berkeley QM simulator is in agreement with optical measurement using spectroscopic ellipsometer (J. A. Woolam M3000V). Usually, for every 2 Å increase in oxide thickness, there is about one order of magnitude leakage current reduction. Therefore, after subtracting the effect of the 2 Å oxide regrowth, the net leakage-current reduction is $\sim3$ orders of magnitude. Both
I-V and C-V curves shown in Figure 6.7 and Figure 6.8 strongly suggest that large leakage-current reduction of ultrathin oxide due to proper RTP processing is reliable and reproducible. Using this fabrication procedure, other researchers should be able to reproduce the large leakage current reduction induced by enhanced phonon-energy coupling.

6.6 Conclusions
We developed a bilayer resist lithographic method based on an all-organic resist and developer to fabricate Ni-gate MOS capacitors. The bilayer resist lift-off procedure uses SU-8 with Shipley S1813 as the intermediate layer. After development, an undercut profile of the bilayer resist is clearly demonstrated. The Ni-gate MOS capacitors are fabricated successfully, which can withstand post-metal anneal. Experimental I-V and C-V curves, together with the C-V curves simulated using the Berkeley Quantum (QM) simulator, demonstrate that large leakage-current reduction (~1000×) can be reliably and reproducibly achieved on ultra-thin SiO₂ (~24 Å) after proper RTP processing.
Figure 6.1  C-V curves of an Al/SiO₂/n-Si capacitor without Post-Metal-Anneal (PMA). The experimental capacitance is only ~70% of the ideal value.
Figure 6.2 MOS capacitor model in accumulation with addition of a capacitance caused by the air gap between Al gate and SiO₂

\[ C = C_{ox} \left( 1 + \frac{3.9d}{T_{ox}} \right) \]
Figure 6.3  Capacitance calculated from the model in Figure 6.2. The existence of an air gap between the Al gate and the oxide reduces the measured capacitance.
Figure 6.4  Fabrication steps of Ni-gate using bilayer resist for lift-off procedure, where SU-8/S1813 resist layers are used to form undercut profile.
Figure 6.5  SEM image of the undercut formed for better lift-off after exposure and development of SU-8/S1813 bilayer resist layers.
Figure 6.6  Experimental and simulated C-V curves of Ni/SiO₂/n-Si MOS capacitors measured at 100 kHz. After PMA, the C-V curve is identical to the ideal/theoretical curve.
Figure 6.7  I-V curves of Ni/SiO$_2$/n-Si MOS capacitor before and RTP anneal at 1120 ºC for 20s in ~500ppm O$_2$. The RTP annealed sample exhibit tunnel leakage current reduction of 4 orders of magnitude.
Figure 6.8  Experimental and simulated C-V curves of the same Ni/SiO$_2$/n-Si MOS capacitors shown in Figure 6.7. The RTP annealed sample in trace O$_2$ (~500 ppm O$_2$) exhibit ~2Å oxide regrowth as determined from the C-V measurement.
CHAPTER 7
EFFECTS OF PROCESS PARAMETERS ON THE PECE EFFECT FOR ULTRA-THIN OXIDE AND OXYNITRIDE

7.1 Introduction
This Chapter describes process parameters such as temperature, trace O₂, and trace moisture on the tunnel current reduction due to RTP-induced Phonon-Energy-Coupling-Enhancement (PECE) effect on metal-oxide-semiconductor (MOS) capacitors. Reduction of gate leakage due to direct tunnel (DT) current of MOS devices is beneficial and vital in sustaining the scaling of CMOS devices. As mentioned in Chapter 1, thinner gate oxides require insulators with higher dielectric constant (high-κ) materials in order to suppress direct tunneling (DT) current. However, there are many issues in implementing high-κ dielectric materials especially in process integration and in device fabrication. It will be of importance to the semiconductor industry if the DT current could be reduced by continuing the use of SiO₂ as gate dielectric. Thus, RTP-induced PECE effect process could provide a solution to the leakage current problem for the semiconductor industry, because the DT current reduction from RTP-induced PECE effect is comparable to that of high-κ dielectrics (3 to 5 orders magnitude reduction). However, the process parameters and conditions used to generate the DT current reduction due to the PECE effect reported in our previous works [37, 72, 73] were incorrect. One year later, the correct parameters were figured out by Chen [112]. The process parameters and conditions required to generate DT reduction will be investigated in detail using Capacitance-Voltage (CV) and leakage current measurements of MOS capacitors in this Chapter.

7.2 RTP annealing in pure N₂ ambient

7.2.1 Introduction
The experimental works on leakage current reduction, J_G due to PECE effects described in Reference [37, 72, 73] were performed using the RTP equipment at University of Louisville. The exact model of the RTP equipment (Modular Process RTP-600S) was purchased at University of Kentucky in 2006. In order to verify the results using the RTP
equipment at University of Kentucky, MOS capacitors was fabricated using the exact RTP conditions at University of Louisville (high temperature RTP annealing in pure N₂ ambient). Ultra thin SiO₂ films were grown on p-type (100) Si substrate with resistivity, \( \rho \) of 1-20 \( \Omega \)-cm. The thickness of the SiO₂ films were approximately 24 \( \AA \pm 0.2 \AA \) as measured from ellipsometer using a fixed refractive index of 1.455. The samples were annealed in varying RTP annealing temperature from 960 °C to 1100 °C using pyrometer control for 30 seconds. The RTP setup is described in detail in Chapter 3. The thickness of the SiO₂ films as measured using ellipsometer were unchanged after the RTP annealing process in pure N₂ ambient. Aluminum (Al) was used as the gate electrode and the back contact in the fabrication of the MOS capacitor devices. Post-Metal Annealing (PMA) annealing however, was not performed, since Al is known to diffuse through thin SiO₂ layer.

### 7.2.2 Results and Discussion

Figure 7.1 shows the tunneling current density, \( J_G \) for the samples used in this study. Capacitance-Voltage measurements could not be performed on these samples due to the high leakage current. The standard for describing the leakage current density, \( J_G \) for MOS devices is defined as the \( J_G \) located at \( V_G - V_{FB} = 1 \) V. Since the flat band voltage, \( V_{FB} \) could not be determined experimentally from C-V measurements, theoretical \( V_{FB} \) was used instead. The tunnel current density at \( V_G - V_{FB} = 1 \) V is listed in Table 7.1. The flatband voltage was calculated theoretically using equation (7.1)\[110\]:

\[
V_{FB} = \Phi_M - \Phi_S
\]

Where \( \Phi_M \) (4.1eV for Al) and \( \Phi_S \) are metal and semiconductor work functions respectively. The p-type semiconductor work function is expressed as [110]:

\[
\Phi_S = \chi_s + \left( \frac{E_G}{2} \right) + kT \ln \left( \frac{N_a}{n_i} \right)
\]

Where \( E_G \) (energy gap for silicon=1.12eV), \( N_a \) (dopant density, \( N_a = 1 \times 10^{15} \) cm\(^{-3} \)), \( n_i \) (intrinsic Si carrier concentration = 1.45 x 10\(^{10} \) cm\(^{-3} \)), and \( \chi_s \) (electron affinity for silicon = 4.15 eV) respectively.
Thus,

\[ V_{FB} = 4.1 - (4.15 + 0.56 + 0.0258 \ln \left( \frac{1e15}{1.45e10} \right)) = -0.897 \, V \]

Table 7.1: Comparison of leakage current density, \( J_G @ V_{G-V_{FB}} = |1 \, V| \) for RTP annealed SiO\(_2\) samples in pure N\(_2\) ambient

| Sample                              | \( J_G @ V_{G-V_{FB}} = |1V| \) |
|-------------------------------------|----------------------------------|
| control                            | 0.016187                         |
| RTP @ 960 °C in pure N\(_2\)       | 0.058206                         |
| RTP @ 980 °C in pure N\(_2\)       | 0.097389                         |
| RTP @ 990 °C in pure N\(_2\)       | 2.2934                           |
| RTP @ 1000 °C in pure N\(_2\)      | 17.417                           |
| RTP @ 1100 °C in pure N\(_2\)      | 23.202                           |

As shown in Table 7.1 and in Figure 7.1, the leakage current density, \( J_G \) for all the RTP samples showed a larger \( J_G \) as compared to the control sample. In addition, higher RTP annealing temperature exhibit larger \( J_G \) as well. This contradicts the results obtained from the previous work on the PECE effect [37, 72, 73]. However, these results correlates with reports obtained elsewhere, where high temperature RTP annealing of SiO\(_2\) (1050 °C) in pure N\(_2\) ambient induce surface roughening [117]. These defects (surface roughening) could create electrical shorting paths from the metal gate to the Si substrate, which could explain the increased \( J_G \) of the RTP-annealed samples (in pure N\(_2\)).

The surface roughening of Si substrate resulting from formation of voids in the oxide film is caused by decomposition of SiO\(_2\) into volatile SiO gas [118-120]. This can be explained from a well-known mechanism occurring during the early stages of oxide loss in high temperature of annealing in a dilute oxygen or high pressure environment [121]. Reaction of O\(_2\) with silicon is a competing process between formation of SiO\(_2\) film and decomposition through volatile SiO gas as shown in the mechanisms described below [119]:

134
a) At high temperature and low oxygen partial pressure:

\[ 2Si + O_2 \rightarrow 2SiO(gas) \]  

(7.3)

b) At low temperature and high oxygen partial pressure:

\[ Si + O_2 \rightarrow SiO_2(solid) \]  

(7.4)

The boundary between these two regions has been established by Lander et al. [122] and can be described by the relationship between the critical \( O_2 \) pressure, \( P_c \) and the surface temperature, \( T_s \) as shown in equation (7.2) below [117]:

\[ P_c = P_0 \exp\left(\frac{-E}{kT}\right) \]  

(7.5)

Where \( P_0 = 4.4 \times 10^{12} \) torr, \( k \) = Boltzman’s constant \((8.617 \times 10^{-5} \text{eV/K})\), and \( E = 3.93 \text{eV} \).

The relation between partial pressure of \( O_2 \) (in torr units) to ppm of \( O_2 \) in torr units is shown in Figure 7.2 and described using the equation below:

\[ P = \left(\frac{\text{ppm}}{1 \times 10^6}\right) \times 760 \]  

(7.6)

The partial pressure of \( O_2 \) in ambient air shown in Figure 7.2 is calculated from the assumption that the concentration of \( O_2 \) in ambient air is 21%.

Figure 7.3 illustrates the Critical Oxygen Pressure, \( P_c \)-Temperature phase diagram for \( O_2 \) interaction with a Si surface. The relationship between the minimum partial pressure of \( O_2 \) (oxygen content is described in parts-per-million, ppm) required to obtain the critical \( O_2 \) pressure, \( P_c \) is also shown in the same figure. The critical oxygen pressure, \( P_c \) and partial pressure of \( O_2 \) (in ppm) corresponding to surface temperature of Si wafer is also listed in Table 7.2. The RTP annealing in pure N\(_2\) experiments conducted involved purging the RTP chamber with N\(_2\) at flow rate of 1 SLM (standard-liter-per-minute) for 5 minutes. This step is necessary to reduce the oxygen concentration in the RTP chamber as the ambient air will stream into the chamber during the loading process. In addition, a high nitrogen flow purge cycle (30 SLM) was performed during the initial annealing process (prior to the ramp up cycle of the RTP process) in order to further minimize the
oxygen concentration in the chamber. However, residual oxygen might be released from the chamber during the heating process. If we assume that the residual oxygen concentration to be in the order of 1 ppm, the $O_2$ partial pressure at temperatures over 990 °C is above the critical oxygen pressure, $P_C$ at (see Table 7.2 in bold). Thus, this might explain the high tunnel current density, $J_G$ exhibited by the RTP-annealed samples at 990 °C and higher (See Figure 7.1).

Table 7.2: Oxygen concentration level (expressed in parts-per-million, ppm) needed at the critical partial pressure to prevent decomposition of SiO₂ at various annealing temperatures.

<table>
<thead>
<tr>
<th>Temp (°C)</th>
<th>Critical O₂ Pressure ($P_C$)</th>
<th>ppm O₂</th>
</tr>
</thead>
<tbody>
<tr>
<td>960.00</td>
<td>0.00037958</td>
<td>0.49945</td>
</tr>
<tr>
<td>980.00</td>
<td>0.00068504</td>
<td>0.90137</td>
</tr>
<tr>
<td>990.00</td>
<td>0.00091385</td>
<td>1.2024</td>
</tr>
<tr>
<td>1000.0</td>
<td>0.0012136</td>
<td>1.5968</td>
</tr>
<tr>
<td>1050.0</td>
<td>0.0047001</td>
<td>6.1843</td>
</tr>
<tr>
<td>1060.0</td>
<td>0.0060872</td>
<td>8.0095</td>
</tr>
<tr>
<td>1070.0</td>
<td>0.0078534</td>
<td>10.333</td>
</tr>
<tr>
<td>1080.0</td>
<td>0.010094</td>
<td>13.282</td>
</tr>
<tr>
<td>1090.0</td>
<td>0.012926</td>
<td>17.008</td>
</tr>
<tr>
<td>1100.0</td>
<td>0.016493</td>
<td>21.702</td>
</tr>
<tr>
<td>1120.0</td>
<td>0.026573</td>
<td>34.964</td>
</tr>
</tbody>
</table>

The high leakage current exhibited by the RTP annealed samples results from electrical shorting paths from the metal electrodes to the voids on the substrate. However, the voids could not be observed clearly on the RTP annealed samples for short time (<1 min). In order to verify this theory, high temperature RTP annealing at 1100 °C at a longer annealing time (2 minutes) was performed. The sample used in this study is similar to the previous RTP experiment (24 Å oxide film). The longer annealing time and higher temperature were needed because experimental work by Liehr et al. [120] showed that the
size and density of the voids created due to decomposition of oxide are dependent on temperature and time.

Figure 7.4(a) shows the SEM image of voids on the Si surface due to thermal decomposition of the SiO₂ film after high temperature RTP annealing (1100 °C) for 2 minutes taken at an angle of 60° at a magnification of 150 ×. The voids can also be seen from a regular optical microscope and they are on the entire wafer. The length/size of the voids is around 15 μm as shown in Figure 7.4(b) (SEM magnification of 5000 ×).

Using low-energy-electron microscopy (LEEM), Hibino et al. [123] found that the growth rate of the voids follows a Arrhenius equation structure (equation (7.7)):

\[
r = r_0 \exp \left( -\frac{E_a}{kT} \right)
\] (7.7)

Where \( r \)= void growth rate (μm/s), \( E_a = 3.9, 4.1, \) and 4.2 eV for 14 Å, 18 Å 22 Å thick oxide respectively, and \( r_0 = 2.8 \times 10^{15}, 1.3 \times 10^{15}, \) and 7.7 \( \times \) 10^{14} μm/s for 14 Å, 18 Å 22 Å thick oxide respectively. It is note that the activation energy, \( E_a \) and growth rate constant, \( r_0 \) are described as function of film thickness.

Figure 7.5(a) shows the temperature dependence of the void growth rate and the void size using these values. These values are calculated from equation (7.7) using the parameters for a 22 Å SiO₂ layer (\( E_a = 4.2 \) eV, \( r_0 = 7.7 \times 10^{14} \) μm/s). Note that the time constant used in the calculation is 2 minutes in order to correlate with the experiment. However, the thickness of the oxide sample used in the thermal decomposition experiment is 24 Å and not 22 Å. \( E_a \) values for oxide films ranging from 14 Å to 22 Å were provided by Reference [123], in which the activation energy of 3.9 to 4.2 eV corresponds to the thickness respectively. Since the activation energy is listed in increasing value for decreasing oxide thickness, we can estimate \( E_a \) for a 24 Å to be around 4.3 eV. Thus, the void growth rate and void size using activation energy of 4.3 eV was calculated and shown in Figure 7.5(b). These data are also listed in Table 7.3. As shown in Table 7.3, the size of voids created during thermal decomposition of SiO₂ at 1100 °C for 2 minutes are 35 and 15 μm for activation energies of 4.2 and 4.3 eV respectively (see Table 7.3 in bold). Recall that
Ea of 4.3 eV was assumed for a 24 Å thick SiO₂ layer and Ea of 4.2 eV was used for a 22 Å thick as provided by Hibino et al. [123]. The size of the voids created in the thermal decomposition experiments of around 15 μm (see Figure 7.4(b)) correlates with the value calculated using Ea of 4.3 eV. Thus, this confirms the estimated guess for the Ea value and also correlates with the model provided by Hibino et al. [123].

Table 7.3: Void growth rate, r (μm/s) as a function of temperature calculated using activation energy of 4.2 and 4.3 eV. The growth time is calculated for 120 seconds. R₀ value of 7.7 x 10¹⁴ μm/s was used.

<table>
<thead>
<tr>
<th>Temperature (°C)</th>
<th>Ea = 4.2 eV</th>
<th>Ea = 4.3 eV</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>r (μm/s)</td>
<td>r @120secs (μm)</td>
</tr>
<tr>
<td>960.00</td>
<td>0.0052324</td>
<td>0.62789</td>
</tr>
<tr>
<td>980.00</td>
<td>0.0098339</td>
<td>1.1801</td>
</tr>
<tr>
<td>1000.0</td>
<td>0.018119</td>
<td>2.1743</td>
</tr>
<tr>
<td>1020.0</td>
<td>0.032760</td>
<td>3.9312</td>
</tr>
<tr>
<td>1050.0</td>
<td>0.077015</td>
<td>9.2418</td>
</tr>
<tr>
<td>1060.0</td>
<td>0.10153</td>
<td>12.184</td>
</tr>
<tr>
<td>1070.0</td>
<td>0.13331</td>
<td>15.997</td>
</tr>
<tr>
<td>1080.0</td>
<td>0.17432</td>
<td>20.918</td>
</tr>
<tr>
<td>1090.0</td>
<td>0.22705</td>
<td>27.246</td>
</tr>
<tr>
<td><strong>1100.0</strong></td>
<td><strong>0.29460</strong></td>
<td><strong>35.352</strong></td>
</tr>
</tbody>
</table>

7.2.3 Conclusion

RTP annealing of thin SiO₂ MOS capacitors in pure N₂ ambient at high temperature was found to exhibit destructive effects on the quality of the SiO₂ film (high tunneling current), which contradicts the experimental results obtained previously [37, 72, 73]. However, this can be explained from the void growth due to thermal decomposition of SiO₂.
annealed at high temperature in sub-atmospheric pressure theory, where the voids in the Si substrate create electrical shorting paths. Large voids in Si substrate was created (at higher annealing temperature, 1100 °C and longer annealing time, 2 minutes) and imaged using SEM, which provided direct evidence to justify the tunnel current measurements. The size of the voids was also found to correlate with the model provided by Hibino et al. [123]. It should be noted that the previous experimental work on direct tunneling current reduction due to RTP-induced PECE effects were performed using the RTP equipment at University of Louisville. It is certain that some impurities might be present since the samples annealed using the RTP equipment at University of Louisville did not exhibit void formations on the Si substrate as was obtained from the experiments conducted in this section (high temperature RTP annealing in pure N₂ ambient).

7.3 Effect of moisture

7.3.1 Introduction

RTP annealing of SiO₂ film in pure N₂ is not the condition needed to generate the PECE effect as described in the previous section and in reference [112]. This is puzzling as reduction of direct tunneling current was clearly observed in our previous publications on PECE effect study [37, 72, 73]. Recent publication of wet thermal oxynitride processed by an situ steam generated method showed a reduction of tunnel current by 10x (one order of magnitude) [124]. This provides an insight that probably some moisture was present in the gas flow to the RTP chamber in the experiments conducted at University of Louisville. In addition, it has also been demonstrated that ultra thin gate oxide grown from steam oxidation showed better reliability than dry thermal gate oxide due to reduced Si-SiO₂ interface roughness, and minimize compressive stress within the strained structure at the interface [125].

7.3.2 Experimental Setup

MOS capacitors were fabricated from phosphorus-doped, n-type Si(100) sample with resistivity, \( \rho \) of 1-20 \( \Omega \)-cm. The SiO₂ film of 21 Å (as measured using ellipsometer with a fixed refractive index of 1.455) was grown in a thermal furnace at 900 °C in a dilute
O₂:N₂ ambient. Post-oxidation annealing (POA) was performed in N₂ at the oxidation temperature (900 °C) for 15 minutes after the oxidation process by turning off the O₂ gas from the furnace. RTP processing was conducted using moisture as the oxide regrowth source. The experimental setup for the moisture experiments conducted is described in detail in Chapter 3. The RTP experiments were conducted at the annealing temperature of 1080 °C using pyrometer control mode for 20 seconds. The specific moisture concentration used for the samples are labeled in the following manner:

1) sample 1: 400 ppm
2) sample 2: 100 ppm
3) sample 3: 600 ppm
4) sample 4: control

The thickness of the samples after the RTP annealing process was measured using an ellipsometer to ensure that the oxide regrowth was in a reasonable range, i.e., within 2 to 3 Å. Back contact metallization of Al was performed prior to defining the electrodes on the front gate oxide. This step is necessary because the post-metal annealing (PMA) process is needed to passivate the interface traps on the Si-SiO₂ interface. However, it is well known that Al can penetrate into weak points of the thin SiO₂ layer leading to an increase in the leakage current as was described in Chapter 6: Section 6.2. The PMA process in forming gas ambient (10% H₂:N₂) was carried out at 450 °C for 30 minutes. This was then followed by defining the Al front gate electrodes using shadow mask in the thermal evaporator chamber. The complete MOS capacitor fabrication process follows the conventional process except that the PMA process in forming gas ambient at 450 °C for 30 minutes was performed prior to gate electrodes metallization.

7.3.3 Results and Discussion

Figure 7.6(a) – Figure 7.9(a) shows the high frequency C-V data for the samples measured at 10 kHz, 100 kHz, and 1 MHz. As shown in these figures, frequency dispersion was not observed indicating a negligible contact resistance. In order to extract the flat-band voltage (V_{FB}) and the thickness of the oxide layer, quantum mechanical C-V simulation software developed by UC Berkeley was used. The C-V data from 100 kHz mea-
surements was used for the simulation purposes, and the extracted data ($V_{FB}$, $T_{ox}$) are shown in Table 7.4.

The interface trap density was calculated using conductance measurement method obtained from 10 kHz measurements as described by Carter et al. [126] using equation (7.8) shown below:

$$D_n = \frac{0.4}{q} \left( \frac{G_p}{\omega} \right)_{10kHz}$$

Where $q$ is the magnitude of electronic charge ($1.6 \times 10^{-19}$ C), $G_p$ is the peak conductance measured at 10 kHz and $\omega$ is radial frequency ($2\pi f$).

Table 7.4: Lists of parameters extracted from C-V and $J_G$ measurements of samples used in the RTP experiments in moisture ambient.

<table>
<thead>
<tr>
<th>Sample</th>
<th>$T_{ox}$ (Å)</th>
<th>$V_{FB}$ (V)</th>
<th>$D_n$ ($cm^2eV^{-1}$)</th>
<th>$J_G$ (A/cm²)@$V_{G-V_{FB}} = 1V$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Control</td>
<td>21</td>
<td>22</td>
<td>-0.44</td>
<td>8.7x10^{12}</td>
</tr>
<tr>
<td>Sample 1: RTP @ 1080°C (400ppm moisture)</td>
<td>24</td>
<td>23</td>
<td>-0.404</td>
<td>1.3x10^{12}</td>
</tr>
<tr>
<td>Sample 2: RTP @ 1080°C (100ppm moisture)</td>
<td>23</td>
<td>22</td>
<td>-0.37</td>
<td>2.6x10^{12}</td>
</tr>
<tr>
<td>Sample 3: RTP @ 1080°C (600ppm moisture)</td>
<td>25</td>
<td>24</td>
<td>-0.35</td>
<td>4.6x10^{11}</td>
</tr>
</tbody>
</table>

The thickness of the oxide as measured using ellipsometry concur with the thickness of the oxide extracted from the C-V simulations. Thus, this certifies that notion that ellipsometry measurements are accurate in determining the thickness of the oxide layer.
samples used in this study exhibit a relatively high-level of interface trap density as compared to the standard level of $10^{10} \text{ cm}^2\text{eV}^{-1}$ (shown in Table 7.4). This attribute could be due to the fabrication process of the MOS capacitors where PMA process was performed prior to depositing the front gate electrodes. It is also interesting to note that flatband voltage, $V_{\text{FB}}$ of RTP-annealed samples in the presence of moisture shifts closer to the calculated ideal $V_{\text{FB}}$ for Al-gate n-type silicon ($V_{\text{FB-IDEAL}} = -0.33$). It is highly possible that a trace amount of water present in the SiO2 layer could react with Al to form atomic hydrogen (H) during the PMA process [65] as described in the equation below:

$$3\text{H}_2\text{O} + 2\text{Al} \rightarrow \text{Al}_2\text{O}_3 + 6\text{H} \quad (7.9)$$

The free atomic H could migrate to the Si/SiO2 interface and reduces the interface states [127]. However, this scenario is unlikely because as mentioned earlier, the PMA step was performed prior to defining the top gate electrode. Experimental works by Yamada et al. [128] showed that the humidity/moisture could reduce the amount of Si dangling bonds at the Si/SiO2 interface. This could be the most likely explanation to describe the $V_{\text{FB}}$ shift to the ideal $V_{\text{FB}}$ as well as the reduction of $D_n$ for the moisture ambient RTP-annealed samples.

The leakage current density, $J_g$ of the RTP samples exhibits tunneling current reduction by 1 to 3 orders of magnitude, with increasing moisture content in the RTP annealing process. It should be noted that the tunneling current density ($J_g$ of $10^{-1}$ A/cm$^2$ for 22 Å) of the oxide layer grown (control sample) is comparable to the quality of SiO2 film reported elsewhere [10]. Thus, the tunnel current reduction from the RTP process is not due to an improvement of the oxide quality from an initial lower quality of SiO2 film. Reduction of $J_g$ of the RTP samples is found to correlate with higher moisture content ranging from 1 to 2 orders of magnitude. The $J_g$ reduction includes the increase of SiO2 layer from the RTP process into consideration, where an order of magnitude $J_g$ reduction results from an increase of 2Å of oxide [10]. As shown in Figure 7.11, RTP annealed sample in the highest moisture concentration (600ppm) exhibits the largest reduction of $J_g$. From this result, it would be logical to assume that higher moisture content would result in a lower $J_g$. However, this is not the case, as the result obtained from this study was based on the most optimum condition. We have observed that higher moisture level RTP
annealing experiments will result in an uncontrollable regrowth of the SiO$_2$ film. In addition, we have also observed “dark circles” encompassing the entire wafer for a higher moisture level than 600 ppm. SEM image of the dark circle was taken and shown in Figure 7.12. The SEM image was taken from the top view in Figure 7.12(a) and tilted at 60° angle in Figure 7.12(b). The diameter of the defects ranged from 2 to 20 μm.

7.3.4 Conclusion

The previous works on the PECE effect using RTP equipment at University of Louisville exhibit a tunnel current density reduction in the range of 3 to 5 orders of magnitude [37, 72]. However, the RTP annealing process was not performed in a pure N$_2$ ambient as what we thought before. Although the tunnel current density reduction from this study (using moisture as the regrowth source) is significant (2 orders of tunnel current reduction), it is believed that moisture ambient is not the ideal and the same condition as that in the RTP experiments performed in the previous PECE effect experiments. This is due to the fact that $J_G$ reduction in the orders of 3 to 5 magnitude was measured and reproduced frequently using the RTP equipment at University of Louisville. In addition, it is also difficult to control the quality of the RTP-annealed process in moisture ambient due to defect formations (see Figure 7.12).

7.4 Effect of trace O$_2$ on tunneling reduction of ultra thin SiON films

7.4.1 Introduction

The process conditions (pure N$_2$ ambient and moisture ambient) to obtain $J_G$ reduction from PECE effect as described in the previous sections experiments did not produce the significant JG reduction as compared to the previous published work [37, 72, 73]. High temperature RTP annealing in pure N$_2$ ambient is destructive to the SiO$_2$ film as described in section 7.2. Thus, some impurities may be present in the RTP chamber in the experiments conducted at University of Louisville since the results obtained in our previous works [37, 72, 73] could not be reproduced. In addition to considering moisture in the chamber, Chen suggested that there might be some trace O$_2$ due to air leak into the RTP chamber at University of Louisville as compared with the RTP machine at Universi-
ty of Kentucky.

7.4.2 Experimental setup

The SiON (Silicon Oxynitride) samples (p-type, Si (100) with dopant density of $5 \times 10^{16}$ cm$^{-3}$) used in this study were provided by Freescale semiconductor. The samples used in this study were cut into small pieces (1 inch $\times$ 1 inch) from the 8 inch silicon wafer. The equivalent oxide thickness (EOT) of the SiON film provided by Freescale semiconductor is 15 Å with dielectric constant, $\varepsilon_r$ of 5. Recall that the dielectric constant of pure SiO$_2$ is 3.9. Thus, the physical thickness of the SiON film is 20 Å.

$$T_{phy} = \frac{\varepsilon_{SiON}}{\varepsilon_{SiO_2}} \times EOT$$  \hspace{1cm} (7.10)

However, the thickness of the SiON was measured to be 22 Å using ellipsometer. This could be due to native oxide growth of the SiON film. The thermal SiON film was grown at Freescale Semiconductor and then shipped to University of Kentucky. During the shipment and the subsequent process, the thin gate oxide was exposed to air for couple of days. Thus, this explains the additional 2Å as measured using ellipsometer.

In order to provide trace amount of O$_2$ in the RTP chamber, mixture of high flow of Helium (He) as the carrier gas and low flow of O$_2$ is needed. Helium was used as the carrier gas to prevent the oxide samples from being nitrided [129]. The RTP annealing of the SiON film was performed at 1080 °C and 1100 °C. The regrowth of the SiON sample due to RTP annealing in trace oxygen is critical. The O$_2$ concentration is controlled by adjusting the amount of O$_2$ in the mixture gas to ensure that the SiON film exhibit only 2 to 3 Å regrowth from the RTP annealing process. The optimized O$_2$ concentration and RTP annealing temperatures used for the samples are labeled in the following manner:

1) sample 1: RTP @ 1080 °C for 45 seconds at 1 % O$_2$: He mixture
2) sample 2: RTP @ 1100 °C at for 45 seconds at 0.5 % O$_2$: He mixture
3) sample 3: control

The complete MOS capacitor fabrication process which includes Post-Metallization-
Annealing (PMA) at 450 °C in forming gas environment (10%H2:N2) is described in detail in Chapter 6. Note that Nickel was used as the gate electrode for this sample. Thus, PMA performed after metal deposition is possible as compared to the MOS capacitor fabrication process in the previous sections, where Al was used as the metal electrode.

### 7.4.3 Results and Discussion

Figure 7.13 shows the high frequency C-V measurements of the RTP samples annealed at 1080 °C (Figure 7.13(a)) and 1100 °C (Figure 7.13(b)) measured at 10 kHz, 100 kHz, and 1 MHz. C-V measurements of control sample is shown in Figure 7.14(a). As shown in these figures, frequency dispersion was observed at 1 MHz due to series resistance from the Nickel gate contact. Contact resistance of Nickel metal is comparatively higher to that of Al metals, which is the reason that frequency dispersion is not exhibited by the samples with Al gates (section 7.2 and 7.3). However, the interface trap density of these samples is of a lower concentration (~10¹⁰ cm²eV⁻¹) than the samples with Al gate electrodes. This is due to the fabrication process, where PMA in forming gas was performed after metal deposition as compared to the Al gate samples. The interface trap density was extracted from conductance measurements as described in the previous section and listed in Table 7.5.

The EOT of the samples extracted from UC Berkeley’s quantum-mechanical C-V simulation are shown in Table 7.5. Notice that the oxide thickness of these samples measured using ellipsometer differ from that of C-V measurements. The discrepancy is because ellipsometer measurements provide physical thickness values, whereas C-V measurements provide the electrical thickness (or EOT). The EOT of the control sample (16 Å) is consistent with EOT value as provided by Freescale Semiconductor (15 Å). Figure 7.14(b) shows the C-V measurements of the samples used in this study, where the difference in thickness is clearly observed in the accumulation region.

The theoretical flat band voltage is calculated as shown below:
Note that the metal work function is 5.1 eV for Nickel. In addition, the Si substrate is p-type semiconductor, thus the semiconductor work function is [110]:

145
Thus,

\[ \Phi_s = \chi_s + \left( \frac{E_G}{2} \right) + kT \ln \left( \frac{N_d}{n_i} \right) \]

\[ \Phi_s = 4.15 + \left( \frac{1.12}{2} \right) + 0.0258 \ln \left( \frac{5 \times 10^{16}}{1.45 \times 10^{10}} \right) = 5.09 \]

\[ V_{FB} = 5.1 - 5.09 = 0.1V \]

The \( V_{FB} \) values extracted from C-V measurements are listed in Table 7.5.

Table 7.5: Lists of parameters extracted from C-V and \( J_G \) measurements of samples used in the trace O\(_2\) RTP experiments.

<table>
<thead>
<tr>
<th>Sample</th>
<th>( \text{Tox} ) (Å)</th>
<th>( \text{Ellipsometer} )</th>
<th>( \text{C-V} ) (V)</th>
<th>( \text{D}_{it} ) (cm(^2)eV(^{-1}))</th>
<th>( \text{J}<em>G ) (A/cm(^2))@ ( V</em>{G-V_{FB}} = 1V )</th>
</tr>
</thead>
<tbody>
<tr>
<td>Control</td>
<td>22</td>
<td></td>
<td>16.2</td>
<td>-0.05</td>
<td>3.2 \times 10^{10}</td>
</tr>
<tr>
<td>Sample 1: RTP @ 1080°C (1 % O(_2))</td>
<td>26</td>
<td></td>
<td>19.7</td>
<td>-0.072</td>
<td>1.7 \times 10^{10}</td>
</tr>
<tr>
<td>Sample 2: RTP @ 1100°C (0.5 % O(_2))</td>
<td>25</td>
<td></td>
<td>18.2</td>
<td>-0.067</td>
<td>1.4 \times 10^{10}</td>
</tr>
</tbody>
</table>

Figure 7.15 illustrates the gate leakage current density vs. gate voltage characteristics, where the RTP annealed sample at 1100 °C exhibits the largest gate leakage density reduction. Even though the RTP annealed sample at 1080 °C shows the lowest leakage current density, the absolute leakage current reduction (taking the regrowth of the oxide layer into consideration) is only 50X lower as compared to the sample annealed at 1100 °C (200X; ~ two orders of magnitude). As shown in Figure 7.15, the leakage current density for the control sample is \( 1 \times 10^0 \), where the EOT of SiON sample is 16 Å. This is already two orders of magnitude lower than the leakage current density for the control sample (taking the thickness into consideration) used in the previous sections. Note that the standard for the leakage current density for a specific oxide thickness is \( 1 \times 10^0 \) A/cm\(^2\).
for an oxide thickness of 20 Å and increases by one order of magnitude for every 2Å reduction of the oxide thickness as shown in Figure 7.16. However, the leakage current density for the control sample is expected because the sample used is not SiO₂ but is SiON film, where the physical thickness is 22 Å.

7.4.4 Conclusion

RTP annealing of industry standard SiON film in the presence of trace O₂ exhibit leakage current reduction by 1 to 3 orders of magnitude. Higher annealing temperature at 1100 °C showed a larger leakage reduction compared to samples annealed at 1080 °C. However, this is still lower than the leakage current reduction observed in our previous work [37, 72, 73]. Although, the results obtained in this study are comparable to the results obtained in the previous section, where RTP annealing was performed in the presence of moisture, it should be noted that the sample used in this study SiON film and not SiO₂. The SiON samples used were of industry standard grade, where the leakage current of the film has been optimized. Thus, a 2 to 3 orders tunnel current reduction is significant. In addition, as compared to the moisture-ambient experiments, the RTP process are less complicated, where only dilute O₂ in He ambient is needed and the regrowth of the oxide film is more controllable. It should be noted that RTP annealing at temperature higher than 1100 °C was not performed. This is due to the conditions imposed by the RTP equipment, where the temperature of the RTP chamber is controlled and calibrated using thermocouple. Temperature measurements exceeding 1100 °C is not possible due to the fast decomposition of the thermocouple materials, which would contaminate the RTP chamber. The effect of RTP annealing in trace O₂ for regular SiO₂ layer is investigated in the next section.

7.5 Effect of trace O₂ on tunneling current reduction of SiO₂

7.5.1 Experimental Setup

MOS capacitors were fabricated on 2 inch, n-type (100) oriented Si wafers with resistivity ρ of 1- 20 Ω-cm was measured. The sample was cut into four pieces, where RTP an-
nealing in trace O₂ was performed on three of the samples while another was used as control. The conditions for the RTP process are as follow:

1) Sample 1: RTP @ 1050°C for 45 seconds (300ppm O₂)
2) Sample 2: RTP @ 1080°C for 45 seconds (200ppm O₂)
3) Sample 3: RTP @ 1100°C for 45 seconds (200ppm O₂)

Note that the oxygen concentration was controlled using a trace oxygen analyzer (Alpha Omega Series 3000) as described in Chapter 3. The regrowth of the oxide layer was regulated by varying the oxygen concentration. The complete fabrication process flow follows the procedure as described in the previous section.

7.5.2 Results and Discussion

Figure 7.17(a) shows the High-frequency C-V (10 kHz, 100 kHz, 1 MHz) measurements of control sample. Figure 7.17(b), Figure 7.18(a), and Figure 7.18(b) shows the high frequency C-V measurements of the RTP samples annealed at 1050 °C, 1080 °C, and 1100 °C respectively. Frequency dispersion at 1 MHz was observed for all samples due to series resistance from the Nickel gate contact as described in the previous section. Figure 7.19 plots the 100 kHz C-V measurements for all the samples used in this study. Oxide regrowth of only around 2 to 3 Å was needed in order to justify the leakage reduction is not from an increase of the oxide layer but is due to the energy coupling between Si-O and Si-Si bonds. Thus, the oxygen concentration needed to produce the expected regrowth was calibrated prior to performing these experiments. As shown in Figure 7.19 and in Table 7.6, the oxygen concentration used for the RTP annealed samples exhibited 2 to 3 Å regrowth as measured using ellipsometer except for the 1080 °C sample, which has only a 1 Å regrowth. The thickness of the oxide layer as determined by C-V measurements (using UC Berkeley QM simulator) is also comparable to the thickness as measured using ellipsometer as listed in Table 7.6.

Theoretical flat band voltage, \( V_{FB} \) is needed to compare with the values extracted from C-V measurements and is calculated using equation (7.1) as follows:

For n-type substrate, \( N_d = 5 \times 10^{15} \text{ cm}^{-3} \)
The equation for calculating the work function is given by:
\[
\Phi_s = \chi_s + \left( \frac{E_G}{2} \right) - kT \ln \left( \frac{N_d}{n_i} \right)
\]

Thus,
\[
\Phi_s = 4.15 + \left( \frac{1.12}{2} \right) - 0.0258 \ln \left( \frac{5 \times 10^{16}}{1.45 \times 10^{10}} \right) = 4.38
\]

\[
V_{FB} = 5.1 - 4.32 = 0.72V
\]

As shown in Table 7.6, the measured \( V_{FB} \) deviates from the ideal \( V_{FB} \). However, all the samples (including control sample) exhibit approximately the same \( V_{FB} \) shifts. This shows that the existence of fixed oxide charges originates from the oxide growth from the thermal furnace and not due to RTP processing.

Interface trap density was extracted from conductance method as described in the previous section and is listed in Table 7.6 as well. However, the values obtained (~7-9 \( \times 10^9 \) cm\(^2\)eV\(^{-1}\)) are too low and this needs to be verified using other characterization methods, such as charge pumping.

Table 7.6: Lists of parameters extracted from C-V and \( J_G \) measurements of SiO\(_2\) samples used in the trace O\(_2\) RTP experiments.

<table>
<thead>
<tr>
<th>Sample</th>
<th>Tox (Å)</th>
<th>( V_{FB} ) (V)</th>
<th>( D_{it} ) (cm(^2)eV(^{-1}))</th>
<th>( J_G ) (A/cm(^2))@ ( V_G-V_{FB} = 1V )</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ellipsometer</td>
<td>C-V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Control</td>
<td>22</td>
<td>22.1</td>
<td>0.63</td>
<td>2 ( \times 10^{10} )</td>
</tr>
<tr>
<td>Sample 1: RTP @ 1050°C (300ppm O(_2))</td>
<td>24</td>
<td>24.1</td>
<td>0.6</td>
<td>7.6 ( \times 10^9 )</td>
</tr>
<tr>
<td>Sample 2: RTP @ 1080°C (200ppm O(_2))</td>
<td>23</td>
<td>23.7</td>
<td>0.61</td>
<td>8.39 ( \times 10^9 )</td>
</tr>
<tr>
<td>Sample 3: RTP @ 1100°C (200ppm O(_2))</td>
<td>25</td>
<td>25.2</td>
<td>0.63</td>
<td>8 ( \times 10^9 )</td>
</tr>
</tbody>
</table>

Figure 7.20 shows the \( J_G-V_G \) curves for the SiO\(_2\) samples used in the trace O\(_2\) RTP annealing experiment. The sample annealed at 1050 °C showed a leakage current reduction...
of $10^6 \times$. If the thickness of the oxide is taken into consideration, $J_G$ reduction is still significant (5 orders of magnitude). It is interesting to note that the reduction of leakage current decreases by an order of magnitude for an increase of $\sim 20$ °C in the annealing temperature, where the samples annealed at 1080 °C showed a reduction by 2 orders and the samples annealed at 1100 °C showed $J_G$ reduction by only 1 order of magnitude. This phenomenon is different from that of SiON film as described in the previous section, where higher annealing temperature results in a lower $J_G$ reduction. This may be caused by process parameter variation and non-uniformity across the wafer. It should also be noted that the RTP annealing process of the SiO$_2$ samples in this study require an optimum oxygen concentration to enable only a slight regrowth of the oxide layer. If the oxygen concentration is too low, decomposition occurs instead of formation of SiO$_2$ layer as described in Section 7.2 (pure N$_2$ annealing). Thus, the competing process between decomposition and oxidation might also play a role in the structural change of the SiO$_2$ layer.

### 7.6 Summary

The electrical characterization work performed in this Chapter showed that the process parameters required to generate leakage current reduction due to RTP-induced PECE effect are optimum temperature and trace amount of O$_2$ or moisture. RTP annealing in pure N$_2$ was found to be destructive due to the decomposition of SiO$_2$ layer at high temperature in pure N$_2$ or He ambient. RTP annealing in the presence of moisture however, showed $J_G$ reduction by 2 orders of magnitude. RTP annealing in the presence of O$_2$ showed $J_G$ reduction by 4-5 orders of magnitude. The variation of leakage current reduction from 2 to 5 orders of magnitude might be caused by process variation. The key factor, however, is a slight regrowth of O$_2$ irrespective of wet or dry RTP thermal regrowth. In addition, trace amount of O$_2$ was also found to improve surface roughening of oxides after annealing in RTP [117].
Figure 7.1  Comparison of leakage current density, $J_G$ @ $V_G-V_{FB} = |1\ V|$ for RTP annealed SiO$_2$ samples in pure N$_2$ ambient [112]
Figure 7.2  Oxygen concentration (parts-per-million, ppm) expressed as a function of Partial pressure.
Figure 7.3  Critical Oxygen Pressure, $P_c$ vs. Temperature phase diagram for O$_2$ interaction with a Si surface. The minimum O$_2$ level correlating to the critical O$_2$ pressure, $P_c$ is also shown.
Figure 7.4  SEM image of voids on the Si surface due to thermal decomposition of the SiO$_2$ film after high temperature RTP annealing (1100 °C) for 2 minutes taken at an angle of 60°: (a) 150X magnification (b) at 5000X magnification. Note the size of the void in length is approximately 15 μm.
Figure 7.5  Temperature dependence of the void growth rate and the void size using the values obtained from Ref [123] for: (a) activation energy of 4.2 eV, (b) activation energy of 4.3 eV. The growth time is calculated for 120 seconds. $R_0$ of $7.7 \times 10^{14}$ μm/s was used.
Figure 7.6  Control sample ($t_{ox} = 21\text{Å}$ Ellipsometer, 22 Å; CV simulation) (a) High-frequency C-V measurement (b) Conductance measurements.
Figure 7.7  Sample 1 (t_{ox} = 24Å Ellipsometer; 23 Å - CV simulation) - RTP @ 1080°C (400ppm moisture) (a) High-frequency C-V measurement (b) Conductance measurements.
Figure 7.8  Sample 2 (tox = 23Å Ellipsometer; 22 Å - CV simulation) - RTP @ 1080°C (100ppm moisture) (a) High-frequency C-V measurement (b) Conductance measurements.
Figure 7.9 Sample 3 (tox= 25Å Ellipsometer; 24 Å - CV simulation) - RTP @ 1080°C (600ppm moisture) (a) High-frequency C-V measurement (b) Conductance measurements.
Figure 7.10 High-frequency (100kHz) C-V measurement of samples used in the moisture RTP experiments ($T = 1080 \, ^\circ\text{C}$ for 20 seconds): Sample 1 (moisture = 400ppm); Sample 2 (moisture = 100ppm); Sample 3 (moisture = 600ppm) and Sample 4 (control)
Figure 7.11 Leakage Current Density, $J_G$ measurement of samples used in the moisture RTP experiments ($T = 1080 \, ^\circ C$ for 20 seconds): Sample 1 (moisture = 400ppm); Sample 2 (moisture = 100ppm); Sample 3 (moisture = 600ppm) and Sample 4 (control).
Figure 7.12 SEM image of defects formed from high moisture (>600ppm) level of RTP annealing of SiO₂ film taken from: (a) top view (b) angle view (60°)
Figure 7.13 High-frequency C-V (10 kHz, 100kHz, 1MHz) of RTP annealed sample in trace O₂ ambient of sample: (a) RTP @ 1080 °C for 45 seconds; (b) RTP @ 1100 °C for 45 seconds. The thickness, EOT and flatband voltage, $V_{FB}$ are obtained using UC Berkeley QM-simulator for the 100 kHz C-V data.
Figure 7.14 (a) High-frequency C-V (10 kHz, 100kHz, 1MHz) of control SiON sample; (b) Comparison of 100 kHz C-V measurements of control and RTP annealed sample in trace O2 (1080 °C and 1100 °C)
Figure 7.15 Leakage Current Density, $J_G$ measurement of samples (SiON) used in the trace O$_2$ RTP experiments: Sample 1 (Temp = 1080 °C for 45 seconds), Sample 2 (Temp = 1100 °C for 45 seconds); Sample 3 (control).
Figure 7.16 Standard leakage current density, $J_G$ (A/cm$^2$) vs. thickness of SiO$_2$ film [10].
Figure 7.17 High-frequency C-V (10 kHz, 100kHz, 1MHz) of: (a) control sample (EOT = 21.5 Å) (b) Sample 1: RTP @ 1050 °C for 45 seconds in 300 ppm O₂ (EOT = 25.2 Å); The thickness, EOT and flatband voltage, $V_{FB}$ are obtained using UC Berkeley QM-simulator for the 100 kHz C-V data.
Figure 7.18 High-frequency C-V (10 kHz, 100kHz, 1MHz) of: (a) Sample 2: RTP @ 1080 °C for 45 seconds in 200 ppm O₂ (EOT = 23.7 Å) (b) Sample 3: RTP @ 1100 °C for 45 seconds in 300 ppm O₂ (EOT = 25.2 Å); The thickness, EOT and flatband voltage, $V_{FB}$ are obtained using UC Berkeley QM-simulator for the 100 kHz C-V data.
Figure 7.19 Comparison of 100 kHz C-V measurements of control and RTP annealed samples in trace O₂ (1050 °C, 1080 °C and 1100 °C).
Figure 7.20 Leakage Current Density, $J_G$ measurement of samples (SiO$_2$) used in the trace O$_2$ RTP experiments: Sample 1 (Temp = 1050 °C for 45 seconds), Sample 2 (Temp = 1080 °C for 45 seconds); Sample 3 (Temp = 1050 °C for 45 seconds) and control. The largest $J_G$ reduction is shown for sample 1, followed by sample 2, and sample 3.
8.1 Introduction

The studies conducted in this dissertation were an attempt to explain and verify the mechanism of Phonon-Energy-Coupling-Enhancement (PECE) effects on Metal-Oxide-Semiconductor (MOS) structures based on material characterization using infrared spectroscopy and electrical characterization using Capacitance-Voltage (CV) and leakage current (I-V) measurements.

Based on material characterizations, we have learned that high temperature RTP annealing on SiO$_2$ films in dilute O$_2$ ambient increases the absorption intensity of the Si-O rocking modes. The increase in infrared absorption intensity is inferred to as energy coupling between the Si-O rocking modes and the Si-Si lattice phonon modes. It was also found that high-temperature annealing in conventional furnace does not produce similar results. The density and stoichiometry of the oxide film was found to be unchanged after the RTP processing.

Device parameters such as flatband voltage, dopant density, interface trap density, and most important of all oxide thickness were extracted from C-V measurements of these devices. We have shown that C-V measurements are easily distorted due to series resistance from metal contacts and also existence of an air gap between the metal and oxide layer. However, leakage current measurements are less affected by these parasitic elements. Thus, we developed a novel lithography procedure, which incorporates the use of SU-8 resist in a manner where lift-off of metals in high-temperature e-beam evaporation could be achieved. The most significant result from this process is that a metal electrode that is inert to oxide layers, such as Nickel could be defined via photolithography process. This enables the device to be subjected to Post-Metallization-Annealing (PMA) process in which accurate C-V data could be obtained. Lastly, electrical characterization of RTP-induced PECE effect was investigated in a variety of process gases, where it was found that trace amount of O$_2$ is the key to generate the leakage current reduction of 3 to 5 or-
ders of magnitude due to the PECE effect.

8.2 Future Work
Although, we have successfully verified the parameters that produce the PECE effects, however, there are still some questions that need to be answered:

1) The FT-IR study was performed on thick SiO$_2$ layer, in which the chemical structure might be different from that of thin oxide. Thus, by employing Attenuated Total Reflectance (ATR) accessory, we could investigate the absorption properties of the Si-O bonds on ultra thin structures. In addition, we could also incorporate this work to high-k structures such as SiON and HfO$_2$ since an interfacial SiO$_2$ layer is always present.

2) Fabrication of MOS transistor structure is also needed to understand the effect of RTP-induced PECE on subthreshold current, mobility degradation as well as hot carrier stress test.

3) Further material characterization to determine the valence band and conduction band offsets of SiO$_2$/Si after proper RTP.

4) Processes for incorporating the PECE effect into the current CMOS device fabrication process flow.
APPENDIX

Matlab Program

Classical C-V curve simulation

% 1-dimensions classical solution for Metal-Oxide-Silicon Capacitor
% at Low Frequency
% Reference:
% Chapter 3: MOS at Low Frequencies
% MOS Physics and Technology, (1982)
% E.H. Nicollian, and J.R. Brews
% ISBN: 0-471-08500-6

clear all;
clc; % Clear memory and print header

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Semiconductor constants
ni=1.45e10;         % Intrinsic carrier concentration (cm-3)
eps0=8.854e-14;     % Permittivity of vacuum (F/cm)
epsi=11.7;          % Relative permittivity of silicon substrate
epsox=3.9;          % Relative permittivity of dielectric (silicon dioxide)
q=1.602e-19;        % Electronic charge (C)
k=1.38e-23;        % Boltzman's constant (J/K)
T = 300;            % Temperature (K)
qf=k*T/q;          % Boltzman's constant at 300oK in electron volts

%****************USER INPUT PARAMETERS******************
%
userfilename=input('File name to save C-V simulation data\n','s');
fid1=fopen(userfilename,'w');   % Initialize output file; first arg is filename
tempi=1;    % temp parameter for while loop
while (tempi==1)
    promptusersubtype=input('Enter substrate type; n for n-substrate, p for p-
substrate\n','s');
    if strcmp(lower(promptusersubtype),'n')==1;
        disp('Substrate type is N-type');
        MOSCsubstrate=-1;
        tempi=0;
    elseif strcmp(lower(promptusersubtype),'p')==1;
        disp('Substrate type is P-type');
        MOSCsubstrate=1;
        tempi=0;
    else
        disp('Please enter either n or p only');
        tempi=1;
    end
end

userdopantdensity=input('Enter dopant density in cm-3, i.e, 1e15\n');
disp('Dopant density entered is');
Ndopant =userdopantdensity;             % Substrate doping concentration (cm^-3)
disp(aa);

usertox=input('Enter oxide thickness in angstrom, i.e, if oxide thickness is 10 Angstrom, enter the value 10\n');
Tox=usertox*1E-8;               % Oxide thickness (cm)
disp('Oxide thickness in cm is ');
disp(Tox);
% For metal gate, please input Vfb here
Vfb=input('Enter flatband voltage in unit Volts\n');
disp(['Flat band voltage is ', num2str(Vfb)])

userVstart=input('Enter start voltage (accumulation), Note that this is NOT gate voltage but surface potential\n');
userVstart=abs(userVstart);
userVend=input('Enter stop/end voltage (inversion), Note that this is NOT gate voltage but surface potential\n');
userVend=abs(userVend);
Nvstep=input('Enter number of simulation voltage points/steps\n'); % number of voltage steps

np=sign(MOSCsubstrate);  % (do not edit this line) n-sub or p-sub
Vstart=(-1)*np*userVstart;  % Silicon Voltage: start (accumulation)
Vend=np*userVend;  % Silicon Voltage: end   (inversion)

% Calculate fermi potential
if MOSCsubstrate==1
    uB=-log(Ndopant/ni);
else
    uB=log(Ndopant/ni);
end

Cox=epsox*eps0/(Tox);  % Oxide capacitance
Lamdaintrinsic=sqrt(epsi*eps0*k*T/(2*(q^2)*ni));  % Intrinsic Debye length (cm)
Lamdaextrinsic=sqrt(epsi*eps0*k*T/((q^2)*Ndopant));  % Extrinsic Debye length (cm)
fprintf(fid1,'Vg(V)    C(F/cm2)   Bend \n');

stepvoltage=-1*((Vstart-Vend)/Nvstep);
Bend(1)=Vstart;
for i=1:Nvstep
    if (Bend(i)==0)
        Cs=epsi*eps0/Lamdap;
        Qs=0;
        VG(i)=0.0+Vfb;
    else
        vs=Bend(i)/0.025875;
        us=vs+uB;
        iu=uB-us;
        F=(sqrt(2))*sqrt(abs((uB-us)*sinh(uB)-(cosh(uB)-cosh(us))));
        Qs=(eps0*epsi/Lmdaintrinsic)*qf*sign(iu)*F;
        Cs=-sign(iu)*(eps0*epsi/Lmdaintrinsic)*(sinh(us)-sinh(uB))/F;
        VG(i)=(-Qs/Cox)-qf*(uB-us)+Vfb;
    end
    Cp=Cs*Cox/(Cs+Cox);
    C(i)=Cp;
    Bend(i+1)=Bend(i)+stepvoltage;

    fprintf(fid1,'%10.4e  %10.4e  %10.4e
', VG(i), C(i), Bend(i));
end

fclose(fid1);
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VITA

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Publications


Pangleen Ong, Chandan Samantaray, Zhi Chen, “Reduction of Gate Leakage Current of Ultra thin Silicon Oxynitride via RTP Induced Phonon Energy Coupling Enhancement,” poster presentation, 64th IEEE Device Research Conference (Penn State University, University Park, PA, June 2006).