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Copper Indium Diselenide Nanowire Arrays in Alumina Membranes Deposited on Molybdenum and Other Back Contact Substrates

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Copper Indium Diselenide Nanowire Arrays in Alumina Membranes Deposited on Molybdenum and Other Back Contact Substrates

________________________________________

DISSERTATION

________________________________________

A dissertation submitted in partial fulfillment of the requirements for the degree of Doctor of Philosophy in the College of Engineering at the University of Kentucky

By
Bhavananda Reddy Nadimpally
Lexington, Kentucky

Co-Director: Dr. Vijay Singh, Professor of Electrical Engineering
Lexington, Kentucky
2013

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ABSTRACT OF DISSERTATION

Copper Indium Diselenide Nanowire Arrays in Alumina Membranes Deposited on Molybdenum and Other Back Contact Substrates

Heterojunctions of CuInSe₂ (CIS) nanowires with cadmium sulfide (CdS) were fabricated demonstrating for the first time, vertically aligned nanowires of CIS in the conventional Mo/CIS/CdS stack. These devices were studied for their material and electrical characteristics to provide a better understanding of the transport phenomena governing the operation of heterojunctions involving CIS nanowires. Removal of several key bottlenecks was crucial in achieving this. For example, it was found that to fabricate alumina membranes on molybdenum substrates, a thin interlayer of tungsten had to be inserted. A qualitative model was proposed to explain the difficulty in fabricating anodized aluminum oxide (AAO) membranes directly on Mo. Experimental results were used to corroborate this model.

Subsequently, a general procedure to use any material that can be deposited using sputtering or evaporation as a back contact for nanowires grown using AAO templates was developed. Experimental work to demonstrate this by transferring thin AAO templates onto flexible Polyimide (PI) substrates was performed. This pattern transfer approach opens doors for a wide variety of applications on almost any substrate. Any material that can be deposited by physical means can then be used as a back contact.
Electron-beam induced deposition using a liquid precursor (LP-EBID) was used to selectively grow preconceived patterns of compound semiconductor (CdS) nanoparticles. Stoichiometric CdS nanoparticle patterns were grown successfully using this method. They were structurally and optically characterized indicating high purity deposits. This approach is promising because it marries the precision of e-beam lithography with the versatility of solution based deposition methods.

**KEYWORDS:** AAO, CuInSe₂, Nanowires, Photovoltaic, LP-EBID

Bhavananda Reddy Nadimpally

1 May, 2013
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1 May, 2013

Date
To

Both the Anumula families,

Amma and Nanna
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Chapter 1: Introduction and Motivation

Silicon is currently the material of choice as a photovoltaic (PV) material, largely due to the availability of raw material, an understanding of the underlying physics and fabrication techniques borrowed from the microelectronics industry. It is essentially the most mature technology and is nearing its theoretical limit of external conversion efficiency. Photovoltaic devices based on gallium arsenide (GaAs) alloys and silicon (Si) have heavily benefitted from the prevalent understanding of semiconductor physics. Ironically, these materials still rely on synthesis and fabrication methods that are far from being considered inexpensive, thus drastically affecting the cost per watt - a key metric that has come to define the merit of almost all PV technologies. Thus began a quest for alternative materials that could be easily synthesized without compromising heavily on the overall efficiency of the cells. Multicrystalline silicon and hydrogenated amorphous silicon (a-Si:H) were among the first such alternative absorber materials followed by cadmium telluride (CdTe), copper indium diselenide (CuInSe$_2$ or CIS) and its sister alloys including the now popular Cu(In$_x$Ga$_{1-x}$)Se$_2$ (CIGS). Organic materials have garnered particular interest in the last decade or so in PV research. Some popular organic photovoltaic (OPV) materials are C$_{60}$, copper phthalocyanine (CuPc) and PTCBI. Despite the progress, grid parity has yet to be
universally achieved. Grid parity is defined as the scenario in which the cost of generating power using alternate means equals or is less than the cost of power attained from the grid that utilizes conventional sources of energy.

The race to lower the cost per watt of photovoltaic modules has spurred innovation essentially through “three generations” of PV technologies. The first generation refers to the wafer based solar cells that utilized electronic grade bulk materials. These devices were moderately efficient. They were however prohibitively expensive for terrestrial use. The active materials accounted for significant portion of the overall cost. The philosophy behind the second generation of solar cells was to reduce the cost of the existing cells using thin films, primarily silicon. The objective of such a move was to scale manufacturing capabilities and minimize the material used. Candidates like CdTe, a-Si:H and CIS were very instrumental in realizing the benefits of such an approach. With time however, as thin film technologies matured, it was expected that cost of other materials used in manufacturing PV modules would become the bottleneck to further improving PV devices (1). It was then considered a more worthwhile pursuit trying to improve the efficiency of the device than to decrease the cost of everything else in the module. Concentrated photovoltaics (CPV) is among the first such methods to be successfully applied to utility scale power generation using record high efficient solar
cells that deploy tandem structures. On a more fundamental level, hot-carrier solar cells, thermo-photovoltaic (TPV) devices, inter-band solar cells and other novel materials including semiconductor nanowires and nanotubes show encouraging signs of improved devices due to their inherently superior material properties. The third generation of PV devices aims to further enhance the feasibility of their use via engineering of such properties where materials and device architectures are fundamentally altered to better suit the applications.

Despite the economic downturn, the installed capacity of PV systems across the world has grown exponentially over the last five years. The info-graphic below reflects this point. This only highlights the growing awareness and a social will to adopt clean energy technologies.
Irrespective of the market dynamics controlling the ultimate cost and thus the profitability of any given technology - single crystalline Si, multi-crystalline Si or thin film, the energy cost of production of solar modules can be viewed as a more reasonable metric when comparing the cost benefits of a given technology. It is called Energy Payback Time or EPBT. More specifically, EPBT is the time it takes to generate the same amount of energy that went into the manufacturing of the solar panel provides a clearer view that strengthens the case of thin film solar cells. Due to the significantly simpler processes and lower quality of materials required for thin films such as CdTe and CIS, the EPBT is generally about half that of Si based systems (2). The two variables that affect this time value is dependent upon on the conversion efficiency of the modules.
and the geographical location of its deployment. For all practical purposes, only the obvious case of increased efficiencies can significantly alter these numbers.

Despite its technical advantages, thin films such as CdTe and CIS based technologies have only accounted for about 14% of the global installed capacity in 2011 (3). Furthermore, only 3% of the global capacity is accounted for CIS based modules. Despite being endowed with material properties that can be customized like only few others and a record efficiency that is as high as 20.4% (4); equaling that of multicrystalline Si, relatively lower rate of adoption is generally attributed to fabrication methods. Although the fabrication process is less energy intensive than any Si based methods, optimization of processes with the presence of 4 elements can sometimes be a complex task. A proven method to consistently yield high efficiency CIS based devices is the so called three stage process - a physical vapor deposition process that is typically associated with low deposition efficiencies (5). Also, with increasing cost of Ga and decreasing Si prices, they appear less attractive. To summarize, the following are some of the critical improvements required to strengthen the case of CIS based alloys for PV systems in a very competitive landscape.
1. Improve fabrication process that utilizes the material more efficiently and yields high efficiencies. Electrochemical methods are the most efficient but are generally less efficient.

2. Minimize the amount of Ga used or replace with cheaper materials. Al and B are being investigated but are in the very early stages of research.

A shift in approach such that advanced device architectures that incorporate enhanced light trapping features may enable the realization of the above mentioned improvements. So far, Si and InP nanowire arrays have been used to fabricate solar cell structures. Si solar cells with nanowire array window layer have already demonstrated a 38.9% improvement in the overall performance when no anti-reflective coatings are used (6). Similarly, when all the active layers in a solar cell are stacked into each individual nanowire of the array, the performance of InP based solar cell exceed the ray optics limit exhibiting 13.8% conversion efficiency (7). This result is significant despite the record planar device (8) of the same material because only 5% of the active material was used. The ramifications of similar improvements due to nanowire arrays when one of the best absorbing materials for PV applications – CIS is used can be significant.
In view of the recent progress in understanding the physics behind nanostructures and their purported advantages along with demonstrated results, the advancement of photovoltaic technologies in its third generation shows great promise. Despite this progress, significantly greater understanding is required to realize the full potential of nanowire based photovoltaics. A great deal of information thus far obtained and conclusions therein are empirical in nature. This stresses the need for successful demonstration of devices and more experimental data. Simultaneously, it is imperative that one understand the primary motive of such work is to effect a change such that the cost – which is among the biggest hurdles in widespread acceptance of any existing PV technology, could witness a favorable change as well. The advent of research on novel electronic materials has ushered a paradigm shift in the primary approach to not just photovoltaic research but other electronic applications as well. It has shifted the conventional “top-down” approach to device fabrication to one that can be considered “bottom-up”. Such a strategy offers many avenues for scientists to tailor the fundamental properties of materials that until now were considered constants. Fundamental material properties are known to change as structures become increasingly small.
Chapter 2: Background and Theory

To appreciate the motivation behind ‘Fabrication of CIS nanowire arrays’ a fair understanding of three aspects will be helpful. Those three are the material (CIS), the design (nanowire array) and the process (AAO based fabrication). This chapter provides the background information on these three key topics.

2.1 CIS based semiconductor materials for photovoltaics

The general device structure of thin film CIGS solar cell device is as shown in Figure 2.1. The architecture employs soda lime glass as the supporting platform to fabricate the device on. It is sputtered with molybdenum which acts as the back contact, followed by the deposition of ~1-2µm thick CIS layer. CIS is a p-type semiconductor. This is followed by the deposition of a very thin cadmium sulfide (CdS) layer (n-type) that acts as the buffer layer. A thin layer (~100nm) of resistive intrinsic zinc oxide (i-ZnO) is then deposited on top of CdS followed by a conducting n-type ZnO:Al (300-500nm) that aids in current collection along with the metal grid constituting of nickel and aluminum bilayer. Although this design is widely used, significant research is being done currently to optimize every aspect of it. Details of the same shall be briefed in the following sections.
CIS, is by no means the ideal photovoltaic material mostly because of its low band gap. It can however be alloyed with other materials to form wider band gap materials. In theory, Ga composition can be gradually changed to alter the bandgap of the material from 1.04 eV (CIS) to 1.7 eV (CGS) (9). Successful implementation of this would in theory yield very high efficiency devices. The best devices thus far have however been limited to devices with $x=0.3$ accounting for 1.2 eV beyond which the electronic and optical properties begin to deteriorate (10). Aluminum can be used to increase energy gaps as well. Similarly, sulfur can be used to partially or fully replace selenium to form materials with higher energy gaps. Lately, a new material called CZTSS (an alloy of Cu, Zn, Sn, Se and S) has been garnering some attention due to the fact that all the materials used in its formation are very abundant and like CIGS, it doesn’t require high cost manufacturing steps to form a PV grade material. Efficiencies as high as
12.6% for CIAS (11) and 9.6% for CTZSS (12) have been achieved so far. Much of the following discussion is relevant to both CIS and CIGS unless specified otherwise.

2.1.1 Atomic Structure

CIS and its alloys are in general referred to as chalcopyrite materials due to the lattice structure they share with chalcopyrite (copper iron sulfide). It has a tetragonal unit cell with a c/a ratio of approximately 2. This ratio causes a distortion in the tetragonal structure. Physically, such a distortion occurs due to the varying strength of the Cu-In, Cu-Se and the In-Se bonds. The unit cell of CIS is as shown in Figure 2.2 (13). One of the biggest advantages polycrystalline CIS has over other photovoltaic materials like Si is its ability to exhibit superior electronic properties in...
polycrystalline state despite significant variations in the elemental composition making it a very forgiving material from a manufacturing standpoint. This relatively high electronic performance of CIS as a polycrystalline material was not fully understood until recently \(^{(13)}\). Theoretical studies were conducted to study defects formed due to compositional variations. In the traditional sense of semiconductor physics, defects due to vacancies and anti-site occupations generally form recombination centers that can severely affect the electronic properties of the material. In CIS however, two Cu vacancies \((V_{\text{Cu}})\) and an In atom in a Cu antisite \((\text{In}_{\text{Cu}})\) form a defect complex that annihilate the effect of each other. Further, the energy cost of formation of such a complex is very low allowing for such defects to have little to no bearing on the energy levels of the material as a whole. This energy of formation can in fact be a negative quantity when the defect complexes are ordered due to the crystal orientation. This explains the formation of ordered defect compounds or ODCs \(\text{discussed below}\).
The formation of CIS is highly dependent on the temperature at which the alloy is formed. CIS films formed at around 500°C are typically slightly In-rich due to the widening of the single phase region of the perfect stoichiometric CIS (25% Cu, 25% In and 50% Se) as seen in Figure 2.3. The alloys formed along the Cu$_2$Se-In$_2$Se$_3$ tie-line on the Cu-In-Se phase diagram are characterized by the ordered defects that are incorporated into the lattice structure while maintaining the chalcopyrite structure. The compounds formed along this line are thus referred to as Ordered Defect Compounds (ODCs). Device quality films are usually characterized by slightly copper deficient compositions - usually in the 22-24% range (13).
2.1.2 Optical and Electronic Properties

CdTe and CIGS, the two dominant thin film photovoltaic device materials possess a property that has essentially made possible the fabrication of thin film devices—absorbing majority of the sunlight using very thin absorbing layers. The physical property that indicates the amount of light absorbed within a certain thickness is the absorption coefficient. The absorption depth can be estimated from these values obtained for different wavelengths. Due to its high absorption coefficient values associated with wavelengths in AM-1.5 sunlight almost all of the sunlight is absorbed within about 1µ of a CIS film. This makes it a very attractive material for thin film devices. Also, it is a direct-bandgap material and hence accounts for more efficient conversion of photons into photogenerated carriers.

Semiconductor materials are characterized by fixed energy bandgaps allowing them to efficiently absorb only at a single wavelength. The available solar spectrum (Air Mass 1.5 or AM 1.5 spectrum), is by definition a spectrum of wavelengths. Provided a fixed spectrum, the photoconversion efficiency of an ideal two-band photoconverter is only a function of the energy bandgap. As a result, the optimal absorption of different spectra of light is characterized by different values of energy bandgaps. That value for AM1.5 spectrum under standard testing
conditions is approximately 1.4eV. A theoretical maximum of about 33% is estimated for a 1.4eV material in a single bandgap photoconverter (14). A clever way to improve the efficiencies is through the use of multi-junction devices. Individual junctions are designed so as to optimize the absorption of a particular segment of the spectrum. These junctions are then stacked in tandem separated by tunnel junctions. Such device architecture is now responsible for almost all of the photovoltaic devices above the 30% efficiency mark. A crucial aspect of such a design has been the ability to sequentially change compositions of GaAs based alloys with Al and In to alter the bandgaps. The ability to tailor bandgaps of materials to improve cell efficiencies had thus far been limited to the expensive GaAs based alloys. Of the current lot of thin film materials used, CIS is the only PV material that can potentially harness the advantage of such flexibilities. Provided below is a comparison of III-V device and CIS based alloys. Instead of using the multi-junction architecture however, different groups have demonstrated that gradation of gallium along the thickness yields high efficiency devices. The highest efficiency so far reported for CIS based devices is 20.3 % (15). While the fabrication procedure for the record cell is unknown, the method used for NREL’s 19.9% efficient device uses fabrication steps that accommodate the gradation of gallium and copper in a three stage co-evaporation process (10). Much is left to be understood about this ternary alloy especially since
it exhibits superior photovoltaic performance in polycrystalline state (15%) compared to its single crystalline counterpart (12.5%) (16). Such counter-intuitive results has thus made the study of grain boundaries and defects in CIS based materials a compelling field of research. An overview of the effects of grain boundaries and defects is provided in the next section.

2.1.3 Grain Boundaries, Defects and Surface Effects

CIS and its alloys are predominantly used as p-type materials in PV devices. Although it is possible to make films that exhibit n-type behavior, it is rather difficult to control the doping concentration of the material. n-type CIS can be grown in selenium poor and indium rich conditions. This is so because the films’ type is a consequence of different atomic compositions and/or defects present in the film and has a much less pronounced effect due to external doping methods. This ability of the material to form both p-type and n-type semiconducting materials allows for fine tuning of thin film compositions to optimize the electrical performance of solar cell devices. CIS solar cells generally use buffer layers and window materials that can cause a significant amount of surface recombination due to the mismatch in lattice parameters (17). Experimentally, this has been well controlled by the use of a Cu deficient surface and due to the intrinsic ability of both materials to interdiffuse to form thin inverted layers.
Experimentally, it has been proven that the high efficiency CIGS devices are characterized by a Cu deficient surface on the absorber layer. It is also well known that significant deficiency in Cu leads to type inversion in CIS based alloys. Such an observation leads to the conclusion that a slight type inversion is necessary for high efficiency devices. The inversion of the absorber material surface near the buffer layer where the Fermi level is only slightly above the midgap allows for the minority carriers reaching the interface to no longer act as minority carriers because of the type inversion within the absorber material. This would thus account for lesser recombination at the interface. By deploying such a design, only a very thin inverted layer is formed so the adverse effects of buried junctions that are detrimental to the open circuit voltage can be avoided and thus not affect the performance of the final device (18), (19).

![Figure 2.4: Effect of grain boundaries on the energy gap of CIS](19)
The valence band maximum in CIS based alloys is a result of the interaction between the Se-p and Cu-d hybridizations. Stable surfaces in chalcopyrites is the polar (112) surface. The stability of these surfaces is because of the Cu vacancies and the In\textsubscript{Cu} antisites resulting in a Cu-poor stoichiometry (19). The growing Se-p forces would thus further eliminate Cu causing a downward shift in the valence band maximum and hence increasing the energy gap at the grain boundaries and the interface as shown in Figure 2.4. The universal presence of such intrinsic effects at all the grain boundaries is not known at this point in time (19). It does however present a hypothesis that could very well explain the superior performance of this polycrystalline material. An extension to the same idea would be to build homojunction devices that could do away with most of the interface recombination. Such an approach would however be plagued with challenges that pertain to the synthesis of an efficient window layer. The implications of such a phenomena in a semiconducting material could have a profound impact on the development of nanostructured devices. The same shall be discussed in the following chapters.

2.1.4 Effect of Sodium

Like many aspects of CIS based solar cells, the impact of Na on the device performance came to light by empirical means. Given the
premise that cost is a significant aspect of any PV technology, soda lime glass (SLG) came to be the substrate of choice for many researchers. Sodium has been known to be an extremely undesirable impurity in the electronics industry. In CIS and its alloys however, it has accidentally proved to be very beneficial to devices. Despite having been almost 18 years since it was first observed by Hedstrom et al., the role of just 0.1 at. % Na boosting the conversion efficiencies by 30-50% is fully not understood (20), (21), (22). Some of the improved characteristics of CIS devices due to Na incorporation are increased adhesion (23), increased open circuit voltage and fill factor (24), increased electrical conductivity (of two orders) of the film and higher net carrier concentration (22). Conflicting reports on its effect on the grain size exist (25), (26).

Several models have been proposed to explain such a phenomena affecting the hole concentration and the electrical conductivity. These models revisit the atomic structure and the presence of Cu vacancies and the In\textsubscript{Cu} antisites. Firstly, as already discussed, at the grain boundaries and the surface, high quality films are slightly Cu deficient. In\textsubscript{Cu} is a donor defect whereas V\textsubscript{Cu} is an acceptor defect. The two models that shall be discussed differ in their approach from here. Contreras et al. proposed that during the growth of the film, when Na and In ‘compete’, Na is more likely to fill the V\textsubscript{Cu} sites and thus inhibits the formation of donor In\textsubscript{Cu} antisites and consequently increases the net hole concentration (22). This
model does not however explain the detrimental effects when Na concentration is increased further and how the formation of ODCs is suppressed in the presence of Na (26). Wei et al. proposed a model that is more comprehensive in its approach to explaining the effects of Na on the electrical properties of CIS. According to this model, Na first eliminates the $\text{In}_{\text{Cu}}$ defects and increases the effective hole concentration. This directly results in the lowering of the Fermi energy level and resulting in a higher $V_{\text{OC}}$. As the concentration of Na increases, it begins replacing the acceptor $V_{\text{Cu}}$ defects resulting in the reduction of net hole concentration. This explains the drop in performance of devices with increased Na concentration. The $V_{\text{OC}}$ is expected to further increase due to the formation of $\text{NaInSe}_2$ at the grain boundaries, a compound with a larger bandgap. The formation of ODCs on the other hand are a direct consequence of the $2V_{\text{Cu}}^- + \text{In}_{\text{Cu}}^{2+}$ defect pairs. With Na essentially replacing the $\text{In}_{\text{Cu}}$ as well as some $V_{\text{Cu}}$ sites, such a mechanism being inhibited can thus be explained (24).

### 2.1.5 Back Contact

In a heterojunction solar cell, stability and formation of an ohmic contact define the merit of the material for this specific application. The back contact of a p-CIS based device would hence require a metal with a high work function to form a stable contact. Molybdenum has a
relatively low work function (~4.55 eV) and yet it is widely considered as the best back contact material for CIS. Indeed, it does form a Schottky contact with barrier of 0.8 eV (25). However, Mo readily forms MoSe$_2$ in the presence of Se above 500°C which effectively removes this barrier resulting in a good ohmic contact (27). This intermediate layer has also been reported to benefit the adhesion properties of the absorber layers (28). Other metal contacts that are known to exhibit ohmic behavior with CIS are Au and Ni (27). Mo films are generally deposited using d.c. sputtering, r.f. sputtering or through e-beam evaporation.

2.2 The case of nanowire arrays for photovoltaic devices

Nanostructured semiconductor materials hold great promise in the field of photovoltaics due to the incredible flexibility they can potentially provide in engineering of materials. Despite its success and its current position as a leader in PV materials, Si nanowire arrays are expected to outperform planar structures. This has to do with some key benefits that nanowire arrays have to offer. Some of the advantages are:

Enhanced Light Absorption – Due to the geometry, reflection of light is significantly reduced, thus increasing the amount of light absorbed by a nanowire array and this has been demonstrated both experimentally and theoretically (29), (30), (31), (32), (33), (34), (35). Such a reduction in
reflection in random nanostructures is not fully understood yet. However, some theories point to gradation in the refractive index. Also, such an arrayed structure can be thought of as an enhanced Lambertian surface that has long been used in PV devices to reduce reflection. Needless to mention, optimization of light absorption is crucial for the functioning of any solar cell device.

Improved Carrier Collection - The collection of minority carriers can be enhanced due to the confined structures resulting in an effective junction area that is significantly larger. This will allow for higher proportion of the photo-generated carriers to be more efficiently collected. This directly translates into a relaxation of the demand for the material used (36). It is particularly more effective in devices that utilize materials whose minority carrier diffusion length is lower than that of the optical depth (37). This makes such architecture extremely relevant for organic semiconductor based PV devices.

Substrate Choice - By deploying such architectures on flexible substrates, performance of the devices can be maintained while not losing out on the added benefits of high quality material. The same has already been demonstrated on CdS nanowire array solar cells. The efficiency of the device barely changed even with the device being bent over several degrees (38).
Experimental data from multiple groups has substantiated that nanowire arrays of Si do indeed improve the absorption properties. The feature size, distribution, and surface properties do affect the extent of this improvement. Some fundamental simulations are provided below pertaining to the improvement of a PV device performance with nanowires in comparison with that of the conventional planar device. Let a simple assumption be made that every photon absorbed generates exactly one electron-hole pair, and not considering any of the loss mechanisms. By using spectral irradiance data from (39) and energy dependent absorption data of a Si wafer and nanowire arrays from (35), the relative change in the maximum photocurrent can be seen in Figure 2.5. If only photons with energy greater than the band gap of Si are absorbed, the increased absorption of sunlight from this analysis indicates that the nanowire array can harvest 41% more photons than the conventional Si wafer.
Figure 2.5: Comparison of maximum photocurrent that can be generated with planar and nanowire array silicon (40)

The key electrical aspects of a typical solar cell that characterize its output are shown below. By considering a solar cell to be a diode in parallel to a light generated current source, the generation of current in a solar cell can be given as:

\[
Current\ Density = J = J_{sc} - J_o \left[ \exp\left( \frac{qV}{kT} \right) - 1 \right]
\]

\( J_o \) is the dark current, \( q \) is the charge of an electron, \( V \) is bias applied, \( k \) is the Boltzmann’s constant and \( T \) is the absolute temperature. The short circuit current density \( (J_{sc}) \) can be thought of as a measure of the number of light generated carriers that are swept across the junction per unit time and the open circuit voltage \( (V_{oc}) \) as the bias across the cell when there is no current is flowing through it (40).
Open Circuit Voltage \( V_{oc} = \frac{kT}{q} \ln \left( \frac{J_{sc}}{J_o} + 1 \right) \)

The external conversion efficiency can then be given as the ratio of the output electrical power \( P_{out} \) to the incident radiant power \( P_{in} \). FF is the fill factor. It can be defined as the ratio of the area described by the J-V curve in the fourth quadrant to the product of the short circuit current and the open circuit voltage.

\[
Conversion\ Efficiency\ \eta = \frac{P_{out}}{P_{in}} = \frac{J_{sc} \times V_{oc} \times FF}{P_{in}}
\]

The minority carrier diffusion length \( (L_n) \) is an important parameter in the consideration of a radial junction solar cell. Ideally, this value would be equal to the optical depth \( (L) \) of the absorbing material in a solar cell device. Let us now consider a record device of known parameters (41): \( V_{oc} = 0.706\text{V}, J_{sc} = 0.0427\text{A/cm}^2, \text{FF} = 0.828 \) and \( \eta = 24.96\% \). Lower minority carrier diffusion length would imply a drop in the current generation. Assuming that the thickness of this device is the same as the optical depth and the minority carrier diffusion length equals that, we can then define the short circuit current as:

\[
J_{sc} = 0.042 \times \frac{L_n}{L}
\]

Now, let the nanowire array cell be defined as having one nanowire of radius \( r \) placed in a \( 2r \times 2r \) square cell. That would imply that
the number of nanowires on a 1m² plate would be $1/4r^2$. Let the emitter layer be of negligible thickness covering the entire array of nanowires. The effective junction area would then be:

$$\text{Effective Junction Area} = 1 \text{ m}^2 + \frac{2\pi rl}{4r^2}$$

Dark current $J_o$ however will scale linearly as area of the junction increases. Therefore, $V_{oc}$ then becomes:

$$V_{oc} = \frac{kT}{q} \ln \left[ \frac{J_{sc}}{J_o \times \text{Effective Junction Area}} + 1 \right]$$

If the radius of the nanowire is such that it equals the value of $L_n$, then as the value of $L_n$ decreases, the performance between a planar and a radial junction solar cell can be compared as shown in the table below.
The table above indicates that the efficiency drops at a significantly lower rate for the nanowire array based design when compared to that of the planar device as the value of $L_n$ decreases. With no additional loss mechanisms, it is interesting to note the efficiency of the nanowire solar cell with 31.77% efficiency. This represents the case when the additional photons are harvested as indicated in Figure 2.5. Obviously, this represents an overly simplified case; it however presents the case of potentially
improving the performance of devices whose minority carrier diffusion lengths are less than their optical depths.

Quantitative analysis of the optical properties of semiconductor nanowire arrays is extremely limited. Even more so are optical functions such as absorption coefficients and refractive indices. For materials such as CIS, with the difficulty involved in fabrication, such data is almost non-existent. Hence, models based on empirical data with significant assumptions are generally used to point to the possibilities of such materials. One such model is the use of experimental data within our group to estimate the possible gain in conversion efficiency of nanowire arrays based solar cells. More specifically, it was estimated that based on a 30 nm shift in the band edge of short CdS nanowire arrays, an increase in efficiency of approximately 27% improvement in CdS-CdTe solar cells with all other parameters that are expected to not be affected by the architecture remain constant. The premise to this model is the absorption of all photons with energies higher than that corresponding to the materials electronic bandgap and nothing beyond. The observed shift in absorption edge accounted for an increased spectral photocurrent density. Relative change in the calculated photocurrent was then used to estimate the possible gain CdS nanowire arrays could have when paired with CdTe thin films. The calculation of photocurrent density was done
using the standard AM 1.5G spectrum made available to the public by NREL. The photocurrent density is given as:

\[ J_n = \frac{q \cdot \Phi_3 \cdot (1 - R_3) \cdot \alpha_{Abs} \cdot L_n}{\alpha_{Abs}^2 \cdot L_n^2 - 1} \left[ \alpha_{Abs} \cdot L_n \right] \]

\[ = \frac{S_n L_n}{D_n} \left( \cosh \left( \frac{x_4 - x_3}{L_n} \right) - \exp(-\alpha_{Abs} \cdot (x_4 - x_3)) + \sinh \left( \frac{x_4 - x_3}{L_n} \right) + \alpha_{Abs} \cdot L_n \right) \exp(-\alpha_{Abs} \cdot (x_4 - x_3)) \]

\[ J_p = \frac{q \cdot \Phi_0 \cdot (1 - R_0) \cdot \alpha_{CdS} \cdot L_p}{\alpha_{CdS}^2 \cdot L_p^2 - 1} \left[ \left( \frac{S_p L_p}{D_p} \cdot \alpha_{CdS} \cdot L_p \right) - \exp(-\alpha_{CdS} \cdot (x_1)) \right] \frac{S_p L_p}{D_p} \left( \cosh \left( \frac{x_1}{L_p} \right) + \sinh \left( \frac{x_1}{L_p} \right) \right) \]

\[ - \alpha_{CdS} \cdot L_p \exp(-\alpha_{CdS} \cdot (x_1)) \]

\[ J_{dr} = q \cdot \Phi_0 \cdot (1 - R_0) \left[ \exp(-\alpha_{CdS} \cdot x_1) - \exp(-\alpha_{CdS} \cdot x_2) \exp(-\alpha_{CdS} \cdot (x_3 - x_2)) \right] \]

\[ J_n = \text{Photocurrent density of electrons in the depletion region edge} \]

\[ J_p = \text{Photocurrent density of holes in the depletion region edge} \]

\[ J_{dr} = \text{Photocurrent density in the depletion region} \]

Optical functions are then interpolated to span all wavelengths which are then used to estimate the current density gain due to the expanded absorption edge. By using the same model, appreciable benefit can be gained by incorporating CdS or CIS nanowires into solar
cell devices. The most gain can however be achieved by an axial junction where both CdS and CIS nanowires are stacked to form an array of superlattice like structure. The possible gain in the ultimate conversion efficiency for different architectures is as tabulated below.

Table 2-2: Expected gain in efficiency due to nanowires using CdS and CIS

<table>
<thead>
<tr>
<th>CdS Nanowire Array - CIS Thin Film</th>
<th>39.3% Improvement to 20.27% Efficiency</th>
</tr>
</thead>
<tbody>
<tr>
<td>CdS Thin Film - CIS Nanowire array</td>
<td>10.8% Improvement to 16.08% Efficiency</td>
</tr>
<tr>
<td>CdS-CIS Superlattice Nanowire Array</td>
<td>55.2% Improvement to 22.5% Efficiency</td>
</tr>
</tbody>
</table>

Clearly, many of loss mechanisms including the yet to be quantified trap density induced recombination effects both in the depletion as well as the surface, shading loss, etc are not factored into this very rudimentary set of calculations. It does however point to the direction of the areas of study that need to be explored and study if such gains can indeed be achieved. Much of this work is an effort to study and remove or work around bottlenecks in the fabrication of CIS nanowire arrays on suitable substrates so that more rigorous studies can then be performed on device-ready nanomaterials. To that end, a thorough understanding of the material itself is crucial. This includes inherent properties of the material, advantages and disadvantages of various processing techniques and its application in PV devices.
2.3 Anodized Aluminum Oxide (AAO) Templates

Anodized Aluminum Oxide (AAO) templates, simply put are robust, porous film that can act as a support structure for the synthesis of nanowires of a wide array of materials. In other words, AAO templates are films with ordered pores that can be used to be filled with a material of choice to eventually make nanostructures for various applications. Self-ordered AAO with hexagonal arrangement of monodispersed pores was first discovered in 1995 by Masuda and Fukuda (42). Efforts to fabricate such templates for a vast number of applications have since illuminated new research avenues and refocused the importance of fundamental studies of anodic films and oxidation of different metal substrates. Many aspects of the fabrication process have been explored from the effect of electrolyte used to the manifestation of the applied potential on the pore formation. Work demonstrating pores with controllable diameters led to the fabrication of the very interesting templates with uniform variation of the same.

The robustness of the template is due to the material itself - Aluminum Oxide (Al₂O₃), a stable, insulating material. An especially attractive aspect of AAO is the simplicity and controllability of the fabrication process. Due to self aligning pores, additional lithographic steps are typically not necessary for the formation of ordered, aligned
pores. Although most fabrication steps depend on the application, the primary step of anodization in a diluted acid solution can be accomplished by using a simple Al foil used in the kitchen. Many groups have successfully used AAO pores for applications in sensing, batteries, energy conversion, etc. However the scope is still limited by some bottlenecks in the fabrication and deployment of such templates. The next few paragraphs will discuss the typical fabrication steps followed by the challenges. Some of the work that my thesis highlights pertains to finding solutions to overcome the same.

Anodization of Al foil is the simplest of many variations involved in the fabrication of AAO templates. Al foil is anodized in an acidic medium such as H$_2$C$_2$O$_4$, H$_3$PO$_4$, H$_2$SO$_4$, etc. A DC potential is applied by using a Pt sheet as the cathode. Two competing processes during anodization are responsible for the formation of pores. The pore alignment and uniformity of pore sizes are dependent generally on the purity and surface roughness of the film. Surface of the starting material is important because the existing film roughness will have a strong impact on how the pores are initiated thus dictating the overall uniformity of pore sizes. Typically, this is overcome in commercially available foils by using a two step anodization method wherein the pores initially formed are etched away resulting in uniform nanopits across the substrate. Higher purity of the film on the other hand will ensure simultaneous increase in the depth of pores across the
substrate. Illustrated below is a simple case of a perfectly smooth surface where anodization is performed using a single step. Concentration of the electrolyte and the potential applied dictate the rate of reaction and the pore width. Finally, the choice of electrolyte affects the porosity of the template. Porosity can be defined as the number of pores per unit area. It is a function of both the diameter and the spacing between pores.

Upon electrochemical anodization, alumina is formed at the anode (43). A platinum sheet is used as the cathode where hydrogen evolves. The anodic and cathodic reactions are shown below.

$$2\text{Al} + 3\text{H}_2\text{O} \rightarrow \text{Al}_2\text{O}_3(\text{s}) + 6\text{H}^+(\text{aq}) + 6\text{e}^-$$

$$6\text{H}^+ + 6\text{e}^- \rightarrow 3\text{H}_2(\text{g})$$

There are two types of alumina formed upon anodization. They are called as barrier-type alumina and porous-type alumina. Barrier-type is formed when the bath consists of insoluble electrolytes while the porous-type alumina is formed when the electrolytes are slightly soluble (44). In the formation of either type, there are two separate layers of oxides. The oxide that is closest to the metal is a pure oxide whereas the oxide on top of that contains adsorbed anions from the electrolyte. The adsorbed species can also be neutral or cationic. Hence, the thickness of the outer oxide (impure oxide) after anodization depends on the species adsorbed, and thus the electrolyte used (45).
Apart from oxidation of aluminum, another key process that dictates the formation of pores is the dissolution of alumina with time which in conjunction with oxidation yields highly ordered pores. This reaction is associated with the dissolution of alumina to form aluminum ions (Al$^{3+}$) at the anode which are then repelled away from anode. The reaction that describes the dissolution process is (46):

$$\text{Al}_2\text{O}_3(s) + 6\text{H}^+(aq) \rightarrow 2\text{Al}^{3+}(aq) + 3\text{H}_2\text{O}$$

The dissolution reaction is caused by two different processes viz. chemical dissolution and field assisted dissolution. Chemical dissolution is associated with a powdering effect of the film due to the concentration
and the type of the electrolyte used. Field assisted dissolution is associated with the generation of heat. At room temperature, with the cumulative effect of the two dissolution processes, it becomes difficult for the substrate to sustain the oxide layer to form pores and hence results in templates of very poor quality. This can easily be offset by having the electrolytic cell contained in a temperature controlled environment that is typically about 6°C (46). Figure 2.6 shows a schematic of the four stages that are typically involved in the growth of pores.

As discussed above, the anodic oxidation of Al, followed by systemic field assisted dissolution of oxide to expose underlying metal layer is widely believed to be the governing process of pore formation. This manifests itself in the current-time (I-t) curve that is generally monitored during the anodization process. The illustrations below correlate the different processes occurring on the Al film and how the same is indicative on the I-t plot.
High purity Al foil is typically used for the fabrication of Free Standing AAO Templates.

Barrier Layer type alumina on the surface. It is characterized by reduced current density.

At constant potential, the alumina surface begins dissolving at points of highest field. These points are generally defined by the surface morphology and/or surface energy. Dissolution increases current density.

Once the pits are formed, they are essentially where the field is the greatest and thus any further dissolution occurs at the bottom of these pits. Oxidation reduces current density.

Current density increases due to dissolution and decreases due to oxidation. It attains equilibrium momentarily.

With all the metal consumed, anodization is completed but a thin oxide layer remains at the bottom that can easily be etched away in Chromic-Phosphoric Acid.

Figure 2.7: Typical Anodization Process of Thick Al Foil
After the entire foil (60µ thick) is anodized (typically done over 21-23 hours), the conducting portion at the bottom of the pores is completely utilized resulting in an oxide layer that can no longer be anodized. For through pores, this barrier layer is removed using a solution containing chromic acid and phosphoric acid. Such thick templates are ideal for some applications. However, due to their extremely fragile nature, it poses a challenge to use them for devices that require subsequent processing steps.
Chapter 3: Fabrication of AAO Templates on Mo and Other Back Contacts

3.1 Introduction

Due to the fragile nature of AAO templates fabricated from thick Al foils, they were not suitable for all applications. Rigid conducting substrates were an automatic choice for the growth of nanoporous alumina as a result. From the discussion about the I-t curve (Figure 2.8), it seems apparent that any conducting film under Al would be quite sufficient to accomplish this. To that end, Indium doped Tin Oxide (ITO) – one of the most widely used transparent conducting oxides (TCO) was an obvious choice for optoelectronic devices integrating nanostructures. Achieving quality AAO templates on ITO however remained a challenge for quite some time due to incomplete anodization resulting from sparking and dissolution of Al and the ITO layer near the air electrolyte interface even before other parts of the Al film was anodized. This was studied in detail by several groups in the past (47), (48). Use of a thin interlayer that could accomplish the task of protecting ITO while providing a conducting back surface to Al were key requirements. This was successfully accomplished by using a very thin layer of Ti (~5nm) as an interlayer (49), (50). AAO has since been fabricated on rigid substrates with several back
contact materials but has never been reported for Mo. A more generic fabrication route was proposed to incorporate and back contact recently (51). However, such a process still requires the fabrication of AAO using thick Al foils - a process where the duration and physical handling are key challenges.

The use of Ti interlayer to grow AAO on ITO is discussed. Also, some of the technical limitations that have restricted the growth of AAO on Mo substrates are discussed. Based on the observations made, a model is proposed that explains the breakdown at the air/electrolyte interface during anodization when some conducting substrates are used. Further, AAO templates are transferred on to PI substrates by simple methods that can be easily scaled and applied to almost any substrate.

3.2 Research Objective

The ultimate objective for proceeding with the following work has been to fabricate CIS nanowire arrays on Molybdenum since it forms a good ohmic contact. In 2009, the only rigid substrates reported to have AAO fabricated on them was ITO/Ti and Si. Since there was an established process within the group to fabricate AAO templates on ITO using Ti interlayer, Ti was a decent place to begin. It was hypothesized at that point, that by being able to successfully build upon an already
established process, we could eventually migrate to a material such as Mo by optimizing conditions as needed. Although little success was achieved, it did however throw light on a few aspects of the anodization technique that highlighted the resurgence of a problem once thought to have been fixed viz. the barrier oxide layer on ITO based templates.

The results discussed here shall include successful electrodeposition of CIS as the measure of success in achieving the objective. CdS nanowire arrays had successfully been grown in 200 nm AAO templates. The very first primary goal was to simply grow CIS nanowires in the AAO template using the established fabrication process and then to extend the same to thicker templates followed by replacing Ti with Mo.

3.3 AAO on ITO with Titanium Interlayer

Whether the template is to be grown on a substrate or made from a sheet of aluminum is dictated by the occurrence of other issues that are unique to each approach. Specifically, AAO templates on ITO/Glass substrates faced some challenges until recently. Weak adhesion at the aluminum/ITO interface and the presence of a thin barrier layer at the bottom of pores essentially obstructed the pores from being through and through to the ITO surface. Titanium is a metal with relatively low conductivity. It can be anodized somewhat in the same conditions as that
of Al. more important however, is the fact that Ti acts as an excellent adhesive layer. As a result, extremely thin layers of Ti can be sufficient for proper anodization of Al on ITO substrates. The use of an ultra thin adhesion layer (titanium) sandwiched between the aluminum layer and ITO addressed this issue (48). To remove the barrier layer without loss of quality of the template, several approaches have been tried including a ramping down of anodizing voltage to gradually reduce the pore diameter and dissolve the alumina in the barrier layer (46). Our group has had more success and uniformity using physical means to etch the barrier layer over chemical methods. Argon ion milling etches both the top of the pores as well as the barrier layer. However, with such thin barrier layers, the reduction in the thickness of the template is negligible compared to its overall thickness.

### 3.3.1 Experimental Details

5.3 nm of Ti was sputtered on clean ITO substrates followed by E-Beam evaporation of 200 nm of Al. Thicker Ti layers (50-200 nm) were also used to form CIS nanowires on Ti instead of ITO. The samples were then anodized in 0.3 wt.% oxalic acid. The I-t curves were recorded. The potential used was 50V. A pore widening step was then performed by letting the sample soak in 5 wt.% phosphoric acid for 1 hour. The samples were rinsed with DI water and dried with flowing nitrogen. Ar ion milling
was then performed for 1 minute to remove any oxide layer that may have been present at the bottom of the pore. This process yielded successful fabrication of high quality CdS nanowire arrays in 200 nm templates in the past (49). With thicker AAO, the duration of ion milling was varied between 1 minute and 6 minutes. Cathodic polarization in dilute (0.25M) KCl was done potentiostatically at 3.5 V until the current saturated. Cathodic electrodeposition of CIS was carried by using an electrolyte as specified elsewhere (52) using a DC potential of -0.8V.

3.3.2 Results and Discussion

It was evident from SEM analysis that nanowires were indeed grown by such a process as shown in Figure 3.1.

Figure 3.1: 200 nm AAO fabricated on Glass/Ti partially filled with CIS.
Although the nanowires were of very poor crystallinity, the first experiment did indicate that it was indeed possible to grow CIS nanowires on ITO based templates. Since significantly longer nanowires are required to improve the scattering events, the pore depth had to be adjusted accordingly. AAO of 600 nm in thickness was then grown using a thicker Ti interlayer. When the thickness of Ti is not adequately increased due to increased Al thickness, delamination and complete disappearance of Al and ITO at the electrolyte/air interface could occur due to large currents. By having adequately thick Ti, it provides longer duration of the Al layer to fully anodized thus resulting in better AAO. Since, the requirement of transparency of the underlying substrate is not of importance for growing CIS nanowires, thicker layers of Ti were used than was required. 50 nm of Ti was used. As expected, anodization proceeded without any of aforementioned interface burn off problems. The pores were uniform and aligned. The barrier layer however remained almost untouched. Characteristic inverted u-shaped barrier layer was formed in most samples indicating that the interlayer metal was indeed affecting the formation of the barrier layer. Successive ion milling was expected to easily etch the same as it had in prior work. That however, was not the case as can be seen in Figure 3.2. Although the ion milling process was successful consistently in 200nm thick templates, the same could not be said for thicker templates. This could be due to two factors. First, thicker templates
require thicker Ti interlayers. As a result, the amount of oxide that Ti forms at the bottom of the pore is higher. Ti based oxides are generally very difficult to etch using dry methods. Secondly, with increasing pore depth, the directionality of the charged ions in the ion milling process becomes extremely critical. With little control over the precise alignment of the pores, it can be a very daunting task to consistently etch the titanium oxide. It is also possible that in electrochemical baths with low conductivities like the one used for CIS, exposure of a good conducting material at the bottom of the nanopores is more important. The results indicated that selective methods that could address the issue with alumina barrier layer and possibly even the TiO$_x$ layer were required.

![Figure 3.2: 500 nm AAO after Ar Ion Milling. The barrier layer is still clearly visible.](image)
Selectively penetrating the barrier layer without the pore depth affecting the process effectively put the onus on chemical methods. Cathodic polarization in a neutral salt solution had been successfully used in AAO templates on Si with Nb interlayer. The premise behind such an approach is the relative ease of dissolving alumina in the presence of OH⁻ ions. In order to selectively drive OH⁻ ions towards the barrier layer without affecting the alumina walls, cathodic means was chosen.

\[
\begin{align*}
\text{Al}_2\text{O}_3 + 2\text{OH}^- & \rightarrow 2\text{AlO}_2^- + \text{H}_2\text{O} \\
\text{H}^+ + \text{AlO}_2^- + \text{H}_2\text{O} & \rightarrow \text{Al(OH)}_3
\end{align*}
\]

The hydroxide could then be dissolved in a mild acid. Experiments were performed to study the effect of cathodic polarization in dilute KCl solution on removing the barrier layer while simultaneously not forming any additional oxides. Samples were subject cathodic polarization in a 0.25M KCl solution at 3.5 V until current saturates. All experiments conducted involved the evolution of bubbles at the surface of the sample. The effect of these bubbles was clearly manifested on the template that was even visible to the naked eye. Since the bubbles rose in the vertically clamped samples, bubbles generated at the bottom of the sample rose up effectively shielding significant portion of the field on the pores closer to the surface. As a result, there was considerably large non-uniformity in the effect of this step on the templates. It was clear however that in regions
where the polarization was effective (lower part of the samples), it was quite effective in forming barrier layer free templates. Shown below is a SEM image of a sample with the cathodic polarization step. Considerably thinner barrier layers (mostly removed) are clearly evident from the results.

Figure 3.3: AAO pore base without cathodic polarization in KCl where barrier layer is obviously present
Figure 3.4: AAO Pore base without cathodic polarization in KCl. Notice the absence of the barrier layer in some pores.

This is consistent with the results we obtained. Nucleation and subsequent growth of nanowires was successful in some samples whereas not in others. In some cases, it was evident that even the barrier layer wasn’t fully removed. As mentioned previously, the effect of rising bubbles shielding the field thus causing large variation in etching profile across the sample can be attributed. Analysis of two SEM images from the same sample where electrodeposition of CIS was done is shown below. The first indicates complete filling of pores with CIS while the exact same sample indicates the complete absence of any filling.
Figure 3.5: CIS successfully electrodeposited in a template where cathodic polarization was performed

Figure 3.6: Unsuccessful deposition of CIS in a template where cathodic polarization was performed
3.3.3 Conclusion

In conclusion, in thicker AAO templates, the use of chemical etching techniques despite their disadvantages proved more effective in the removal of the barrier layer oxide that is crucial to subsequent electrodeposition of any material inside the pores. Due to the vigorous evolution of hydrogen, significantly large variation and non-uniformity occurred in removing the barrier layer. Several attempts were made to alter the experimental setup so that the electrodes in the cell could be placed such that the sample can face up rather than sideways. By doing so, the goal was to ensure uniformity across the sample as the gas rises without affecting the template higher up. With the given resources, it was difficult to come up with a design such that the non-anodized metallic layer of the template is exposed to air while letting the cathodic polarization affect the anodized surface.

3.4 AAO on W/Mo Substrates

A very limited number of materials have thus far been realized as back contact materials for the fabrication of AAO templates on conducting substrates. They include ITO, Ti, Pt, Nb, Au and W. Recently, work demonstrating the fabrication of AAO templates on any conducting substrate (51). Despite the proof of concept that it is indeed possible to
fabricate AAO templates with almost any conducting substrate, a crucial limitation of the process included the use of AAO fabricated from Al foils which were later transferred to the substrate of choice. The limitation is the fact that such templates, as mentioned earlier are very fragile and scalability of such processes can be very difficult. Work by Jihun Oh has also demonstrated that AAO templates can be fabricated on almost any substrate by using a W interlayer (53). The methods adopted by the latter group are more promising than the former simply because of relatively robust fabrication methods. This largely stems from their discovery of tungsten as an excellent interlayer due to some innate properties of the metal itself viz. high ionic conductivity and high Pilling-Bedworth ratio (PBR) relative to that of Al and Al$_2$O$_3$ respectively. The process window associated with this method where successfully exposing the underlying metallic layer without oxidizing the back contact and without causing vigorous evolution of O$_2$ is extremely narrow. Both groups have also demonstrated the use of Au as the back contact material using their respective methods. In this study, AAO templates have been fabricated on Mo substrates with a W interlayer. The objective for the choice of Mo is due to its excellent properties in forming ohmic contact with CIS based PV materials. Hence, for CIS nanowire arrays, Mo is the ideal back contact material.
Mo, like most highly conductive metals makes a poor back contact with AAO. This is largely due to the fact that upon complete anodization of Al, the oxide dissolution of the back contact is very fast and is often accompanied by rapid evolution of oxygen causing structural damage of the template at the air/electrolyte interface. Often, this is breakdown is very rapid and the underlying metal is consumed leaving an open circuit like situation hurting further possibility of electrodeposition in the template. Typically low conductivity materials like Ti and Si are used as back contact materials to partly circumvent this problem. Each has its fair share of challenges.

Recently, it was claimed that when appropriately thick tungsten is used as an interlayer, one can fabricate AAO templates with substrates of almost any material (54). Certain properties specific to tungsten, make it somewhat of an ideal interlayer material. First of the reported properties are the higher ionic conductivity of tungsten than that of aluminum. With this ability, when Al is fully consumed to form Al₂O₃, the oxygen diffusion from the electrolyte through the barrier layer tends to easily form WO₃. Important to note here is that the oxidation of W occurs at the same anodization conditions as that of Al. Secondly, the Pilling-Bedworth ratio of the tungsten oxide to tungsten is 3.6. In other words, the volume of metallic tungsten that is oxidized increases by a factor of 3.6. With such a large PBR value, the alumina barrier layer is physically broken leading to
selective perforation of the barrier layer (53). This in itself merits W as the best interlayer material for AAO on conductive substrates. Finally, the dissolution of WO₃ is favored in a neutral ambient with the pH value approximately around 7. The dissolution of WO₃ is crucial for two reasons. First, WO₃ is stable in acidic medium but dissolves readily in neutral and alkaline solutions. Alumina on the other hand dissolves in highly acidic and highly basic media and is generally not affected by neutral solutions. This variability in the dissolution of the two oxides provides a window of opportunity to selectively etch one over the other. WO₃ can be easily etched to expose metallic layer underneath it by a simple soak in pH7 buffer solution for 5-10 minutes. Secondly, with the relative stability of WO₃ in acidic media, it becomes the rate limiting step that dictates further oxidation of any underlying materials. In other words, due to the relatively low field assisted dissolution of WO₃ relative to alumina, one can avoid the rapid evolution of oxygen that has generally plagued most metal substrates.

To fully understand the significance of the advantages of tungsten, it is important to understand the kinetics that governs the formation of alumina due to anodization. It was illustrated as reproduced below. The same kinetics are applied for the case where a conducting substrate is present and how the oxygen evolution can indeed cause delamination and cause an open circuit at the air/electrolyte interface.
An analytical model describing the kinetics at the air/electrolyte interface in AAO templates on conductive substrates is provided in the following pages. With proven benefits of the W interlayer and its supposed ability to help fabricate AAO on almost any substrate are closely studied. In this case, since the metal of interest is Mo, the same has been used for experimental verification. Also, new insights are provided into the formation of sacrificial oxides when W interlayer is used. These insights are then used as the basis to fabricate flexible AAO templates in a truly universal process that enables the use of essentially any material that can be physically evaporated or sputtered.
3.4.1 Experimental Details

Initially, AAO is fabricated on Mo substrates. This is done by DC sputtering of 1600nm of Mo on clean soda lime glass substrates. This is followed by E-beam evaporation of 500 nm of Al followed by anodization of 0.3M oxalic acid at 6°C. A platinum disc is used as the cathode. The effect of a tungsten interlayer is studied by sputtering W at low power. The thickness of this interlayer is varied from 5nm to 20nm. The I-t curves are recorded during the anodization process. The samples are then soaked in 5 wt.% H₃PO₄ for 50 minutes followed by 10 minutes in a pH 7 buffer solution to etch away the WO₃ formed. The objective is to arrive at a condition such that the interlayer can be etched in-situ to expose the underlying Mo layer.

3.4.2 Enhanced Dissolution at the Air/ Electrolyte Interface

The kinetics of ions during the electrochemical process paint a very simplistic model where the migration of cations and anions are shown with respect to the normal field applied for a two dimensional case of thin films. For the case where AAO includes pores, the breakdown of the metallic layers needs a slightly modified model to explain the spontaneous rise in current values, thus limiting the completion of pore formation. At the air/electrolyte interface, a portion of the metallic layer that is not submersed in the electrolyte remains in its metallic form without
undergoing significant anodization. Shown below is a schematic that the following explanation is used to describe.

Figure 3.8: Qualitative model of anodization kinetics at the air/electrolyte interface

With the premise that an alumina wall is present at the air/electrolyte interface throughout the anodization process, a lateral field exerted by the metallic layer on the inside of the wall can be assumed. This is negligible for very shallow pores. By treating the electrolyte as an infinite source of O$_2^-$ ions, one can expect the lateral field exerted by metallic Al to increase as the pore depth increases. With pores deep enough, the lateral field is no longer a negligible value resulting in more O$_2^-$ ions moving towards the available metallic aluminum directly beneath.
the air/electrolyte interface. As a result, a very shallow region can be expected to be anodized at a faster rate relative to the rest of the sample resulting in the premature exposure of the underlying Mo (or any other conductor used). As a result, the current will rise uncontrollably due to the field assisted dissolution in the presence of a large number of O$_2^-$ ions. With the exposed metal providing the path of least resistance for any of charged ions in the electrolyte, the dissolution is further sped resulting in an exponential rise in current. The analytical model proposed here applies to any conducting substrate. The fact that this type of problem exists even during the anodization of metallic Al foils sometimes confirms that the interface burn off is not as dependent on the conducting substrate as previously expected.

Figure 3.9: Kinetics of Al anodization at the air/electrolyte interface when the lateral field is negligible compared to the vertical field
The delamination and the eventual open circuit formation occurring for some substrates and not for others can be explained by stability of the oxides of respective substrates. Field assisted anodic dissolution of Mo is very rapid. Consequently, the anodization of the rest of the sample is at the mercy of how long it takes to completely dissolve the Mo beyond which there will be no conducting medium connecting the same.

The same however is not true for metals like Ti and W. It has repeatedly been demonstrated that when they are used as conducting substrates, stable AAO templates can be created. This can be attributed to the relatively stable oxides that they form. WO₃, as already shown does not dissolve readily in acidic media. Similarly, Ti forms stable oxides. Once
such an oxide is formed, the rate of anodization is drastically reduced at the air/electrolyte interface despite the complete consumption of Al. Thus, a conducting pathway exists for field to continue anodization in the remaining portions of the sample. That however does not mean that a finite thickness of the interlayer will suffice for any thickness of Al to be anodized. The interlayer thickness required for complete anodization is a function of the time it takes to fully anodize the Al layer. This is because metals such as Ti will eventually be fully consumed although at a much slower rate than Al. The same is true for W. This has experimentally been demonstrated by the use of varying thickness values for a W interlayer on Mo substrates as shall be discussed later.

3.4.3 Results and Discussion

The I-t curves recorded for various thickness values of the tungsten interlayer provides valuable information about the anodization processes. Shown below are curves of 4 samples with the thickness of W varying from 5nm to 20nm. The values were recorded manually. As a result, some resolution in the data was lost. Regardless, the trends expected from the curves are absolute and can be fully relied upon.
Figure 3.11: Fabrication process depicting the exposure of Mo at the bottom of AAO

Figure 3.12: Samples with different W interlayer thicknesses after the anodization.
Figure 3.13: I-t curves of AAO on W interlayers of different thicknesses

All the curves indicate clearly the drop in current values initially resulting from the formation of a thin oxide layer on the Al film. This is followed by an increase in the current values due to field assisted oxide dissolution followed by an equilibrium state. The results until this point only vary in the magnitude of the current density. Tungsten is less conductive than the both Al and Mo. Therefore, with a thicker interlayer one can expect the current density across the film to change accordingly. More obvious however is the drop in current after the equilibrium state is only observed in the case of thicker interlayers and none whatsoever when thinner layers are used. The linear shift in the duration it takes to deviate from the equilibrium state to a condition with unstable currents or
decreased currents paints a clear picture about the processes occurring physically on the sample. The results become clearer when the samples appearance is directly related to whether or not the anodization reaches the fourth stage (current dropping). Samples with 5nm and 10nm of tungsten interlayers appear gloss white indicating incomplete anodization of the Al layers along with a distinctly dark region near the air/electrolyte interface. The latter two however appear dark pink or emerald green depending on the angle it’s viewed at. Also, the latter two did not have any clear indication of the interface layer being burnt out. Cross sectional SEM analysis of the AAO templates thus formed confirms that the first two samples were incompletely anodized whereas the last two anodized successfully. Anodization of tungsten is also clearly visible confirming that the barrier layer has been fully removed by WO$_3$.

Figure 3.14: AAO on 5nm W interlayer away from the interface
In order to test the model proposed, an entire sample with insufficiently thick interlayer (10 nm) was examined. Based on the proposed model above to explain the case of an insufficient interlayer, the dissolution of the template along with complete exposure of Mo should mark the onset of the uncontrollable rise in current. Conversely, if the anodization is terminated precisely at the onset of the uncontrollable rise in current, one should expect to see fully dissolved template exposing the Mo substrate at the interface while regions far away from the interface are incompletely anodized. Shown below are SEM images taken from the same sample – one near the air/electrolyte interface and the other at the farthest point away from the interface (Error! Reference source not found.). Visually, it is clear that the template is fully dissolved at
the interface while incomplete anodization occurs far away from it. The exposure of Mo on the other hand is more subtle. Perforation of the interlayer to expose Mo is not uniform. This behavior is also true for thicker interlayers as shall be demonstrated later. The partial exposure however is enough to cause an elevation in current values which further hastens the dissolution of Mo. This non-uniform exposure is visible in the form of pits that transcend the thickness of the interlayer on the left portion of the image.

Figure 3.16: Region near the air/electrolyte interface after anodization with a 10 nm W interlayer
In samples with sufficient tungsten layers, additional steps were attempted to fully expose the underlying Mo layers. These included the use the reactive ion etching (RIE) with SF$_6$ as the active etchant. The parameters used for RIE are as follows: SF$_6$=5 sccm, Ar = 20 sccm, RF Power = 50W, ICP Power = 250W, pressure = 7.5 mTorr and DC Bias ~220V. The duration was varied from 30s to 180s. Finally, electrodeposition was performed to grow CIS nanowire arrays from an acidic chloride bath. The details of the electrochemical cell setup along with other material, optical and electrical characterizations are discussed in the chapter pertaining to CIS nanowire arrays.
The results from the above experiment were promising yet pointed to a problem that was not anticipated. First, with sufficiently thick tungsten layers, there were signs that the tungsten was beginning to get fully oxidized and expose the underlying Mo. This was however very
inconsistent and non-uniform. A closer look at the bottom of the pores makes this point clearer. It can be inferred that the rise in current despite the presence of tungsten interlayer is due to the exposure of Mo in some of the pores resulting in a path of least resistance for the charged ions in the electrolyte providing them lesser incentive to fully oxidize tungsten. Also, thicker W ensured pin hole free high quality templates. These templates were tested for conductivity by electrodepositing CdS nanowire arrays. The results were the best obtained thus far. The pores were fully filled. No further characterization was performed since W neither forms an excellent Ohmic or a Schottky contact. SEM images reveal the quality of the nanowires deposited in these templates. Similar results were obtained on W coated ITO.

Figure 3.20: CdS Nanowire Array on Mo/W bilayer
Figure 3.21: CdS Nanowire Array on ITO/W. Interlayer thickness required on ITO is significantly lower than that on Mo. Here, 10 nm of W was used.

Figure 3.22: Top view of the template indicating non-uniform exposure of Mo. Close up indicating the same
Thicker W layers (50 nm) were thus used to accommodate uniform pin hole free templates. This approach presented a problem. The tungsten had to eventually be removed. Unlike titanium, tungsten can be etched selectively by using SF$_6$ based chemistry to selectively etch away the remaining tungsten.

Given the extremely small size of the pores and the alumina walls, it is imperative thus to ensure enough anisotropy to prevent the delamination of AAO template. It has been reported previously that the anisotropy can be altered by the radical to ion flux ratio (55). Since the directionality of charged radicals/ions is considerably improved in an inductively coupled plasma assisted RIE (ICP-RIE), the DC bias and thus the etch rate also improve. Therefore, a low radical/ion flux ratio was used in order to prevent an uncontrollable etch rate. This is achieved by using SF$_6$ based chemistry to selectively etch tungsten using inductively coupled plasma assisted reactive ion etch (ICP-RIE). Although the lateral etch rates is comparable to the vertical etch rate, the process does demonstrate the sufficiency of using SF$_6$/Ar based chemistry for this application. Progressive etching of the underlying thick (50nm) W layer is evident from the SEM images below.
Figure 3.23: ICP-RIE performed for 30s to etch W interlayer

Figure 3.24: ICP-RIE performed for 60s to etch W interlayer
Figure 3.25: ICP-RIE performed for 90s to etch W interlayer

Figure 3.25 demonstrates clearly the perforation of the W interlayer and when RIE was performed for 90s. The etched tungsten layer forms a mesh like structure due to its selective etching underneath the AAO template. An interesting aspect is the etching of Mo. It can be seen that Mo is also etched after the tungsten is fully consumed. Prolonged RIE past this stage yielded AAO templates where the template itself started to peel off. In some cases, the mere static in the sample boxes they were stored in was enough to fully peel them off. This condition with fully etched tungsten interlayer was later used to electrodeposit CIS nanowires.

3.4.4 Conclusion

CIS nanowire arrays have successfully been grown by electrochemical deposition in AAO templates on Mo substrates for the first
time. This provides for the first time a platform similar to its thin film counterpart so further optimization work can be done. To achieve this, a deeper understanding of what causes the breakdown of the air/electrolyte interface was required. Direct anodization of Mo is characterized by a breakdown that presents itself at the air/electrolyte interface. This occurs after the interface is anodized at a faster rate than the rest of the template due to an additional lateral field emanating from the non-anodized portion of metallic Al outside the electrolyte. Also, tungsten is an ideal choice as an interlayer material. The use of a W interlayer combined with a dry reactive etch step, the underlying Mo was exposed. These templates were used to electrochemically grow CIS nanowires. More details of the nanowires are provided in the next chapter.

3.5 AAO on Polyimide with Back Contact of Choice

From the results and discussions in the previous section, two things are abundantly clear. Tungsten is an excellent interlayer material and although it may be possible to fabricate AAO with any material as the back contact with a W interlayer, it will require optimization steps unique to individual materials chosen. It will be particularly difficult for substrates whose adhesion with glass isn’t necessarily excellent. Also, with the all the steps included within the anodization process, it could be rather difficult to
achieve the same on flexible substrates. Despite its many desirable attributes, W interlayer has on occasion compromised AAO templates for us. AAO templates peeled off occasionally when dried with flowing air. This indicated poor structural foundation for AAO templates. It did however provide an opportunity that if taken advantage of could result in the easy extraction of the stand alone, through pore, ultra thin templates. This pertains to the oxidation of tungsten. The underlying theme among all the SEM images of AAO with W interlayers is the general pore widening at the base. A closer look at the base reveals an isotropic profile of the pit formed as a result of continued anodization of tungsten. This translates to the oxidation proceeding both along the axis of the pore and that of the substrate. To fully understand the impact of anodization on the tungsten surface experiments were designed to remove AAO leaving behind just the untreated W surface. Results and discussion include this study along with how this poor structural stability of AAO is taken advantage of.

3.5.1 Experimental Details

Clean glass slides were coated with 100 nm of W. Al of appropriate thickness was deposited using the E-beam evaporator. Since, most of the processes have been optimized to 500nm thick templates, the same was initially adopted. That said, with substantially thick W as is used in this case, significantly thicker Al layers could be supported. Anodization setup was
same as the one used for the development of AAO on Mo. The anodization was carried out at 40V until the rate at which current density drops is less than 0.0025 mA/cm²/s. None of RIE steps were used since the objective behind this experiment is to study the effect of anodization on W itself. Pore widening was accomplished as previously noted followed by the removal of WO₃ using pH 7 buffer solution. As anodized samples without pore widening of WO₃ removal were also used to compare the dimensions of the various features. AAO was then peeled off using commercially available double sided adhesive Polyimide tape leaving the bare surface of corroded tungsten. SEM and AFM were used to analyze surfaces of the tungsten as well as the bottom of AAO peeled off. Software including ImageJ and Gwiddion were employed to analyze morphology of the features on these two surfaces.
3.5.2 Results and Discussion

From the initial observations made on AAO with W interlayer, widening at the base occurs. Conversely, thickness of the metallic tungsten beneath the pore walls is reduced. As a result, the structural foundation is no longer as strong. With continued anodization, more WO$_3$ is formed. Due to the passive nature of this oxide in acidic medium, it provides a limiting mechanism where further oxidation becomes difficult. That however, is enough to weaken the base. This is sometimes manifested by the peeling of AAO with strong air blown across the
sample. The first experimental analysis is conducted on once such substrate where there is no AAO left. Shown below is a cross sectional view of a sample as anodized on 100 nm of W without any additional pore widening steps. Of interest is the presence of WO$_3$ and widening of the base. ImageJ was used to more accurately measure the width of the pores. The expected value of the pore diameter for the given anodization condition without the pore widening step is less than 40 nm. A visual representation of the experimental steps is used to discuss the results in the next section.

Figure 3.27: As anodized on 100 nm W layer. Typical pore diameter is ~25 nm
Figure 3.28: Grayscale intensity map depicting 3 pores. The valleys correspond to the pore diameters.

The plot above indicates the linear grayscale profile of a line drawn across the cross section of 3 pores. Although the SEM image was acquired with a tilt, the horizontal dimension will be independent of the tilt. Therefore, all values obtained thereof are reliable. Many such profiles were analyzed across several regions of the sample. A profile representative of all the profiles was chosen. The pore diameter varied between 20 nm and 30 nm. This conforms to the expected value of less than 40 nm. It also indicated significantly large wall thicknesses as is visually evident in the image itself. Typical thickness of alumina walls were ~65 nm.
Figure 3.29: Top view of W surface after the template is peeled

Figure 3.30: Grayscale intensity map depicting 3 pits on the W surface. The valleys correspond to the pit diameters of ~70nm. The peaks corresponding to the rings are ~10 nm

Similar analysis on the top view of the tungsten surface illuminates very interesting results. It should be noted that the pH 7 buffer etch was performed on this sample although no pore widening was done. This step
does not affect the dimensions of AAO or W. Its only impact is on the WO$_3$ formed. Doing so cleans up the surface to provide a better view of the morphology created by the anodization process on the W layer. Typically, the diameter of the pits varied between 65 and 80 nm. Also, the edges of the pits were extremely thin (10-15 nm). These results quantify the isotropic nature of the oxide formation spreading to regions underneath the pore walls as well. AFM was used to study the two surfaces after the pore widening step. The Si tips used proved to have tip-heads too large for profiling pores of such small size. Quantifying the data was difficult due to this reason. However, several line scans proved the existence of a double dip profile coupled with sharp peaks on the flipped AAO template consistently as shown in Figure 3.31 and Figure 3.32. When the triangular tip on the AFM in contact mode moves linearly across a region with tapered alumina walls surrounding nanopores as is expected after the peel off, we can expect to see a local minima and a significantly lower value soon after. The significantly lower profile corresponds to the center of the pore where the depth of the pore is larger than the length of the tip whereas the local minima corresponds the edge of the tapered region before the tip abruptly ‘drops’ into the pore. Such a signature is observed twice in this particular profile. The linearly increasing height followed soon after by an equally linear descent indicates that the regions corresponding to the maximum height are very narrow and sharp as was
expected to the thinning of the base of the pores. Similarly, the profile corresponding to the W surface yields a significantly more periodic profile. This also indicates larger radii of the pits formed as compared to the pore radii in AAO as shown in Figure 3.30. The surface morphology is indicative of the same as shown in Figure 3.35. Also, it is possible to see a deeper profile of the tungsten surface due to its relatively larger ‘pits’ compared to the pores on the template.

Figure 3.31: Linescan of peeled AAO using AFM showing the ‘double dip’ from the peak indicating the tapered pore walls
Figure 3.32: Linescan of the tungsten surface after AAO is peeled. Pit diameter is consistent with the SEM analysis and the double dip is absent as expected.

Figure 3.33: Surface morphology of the FAAO.
Figure 3.34: Surface of FAAO. These pores were at the bottom of the template prior to peeling. The peeling process is a clean process as is indicative of the visibly open pores.

Figure 3.35: Surface morphology of the W surface
The peeling step for transfer of AAO patterns onto flexible adhesive substrates is a relatively clean process and involves no more tools than typical adhesive tapes. The mechanical strength required is very nominal.
in nature. Although no tests to find the threshold adhesive strength have been done, it was found to be relatively simple to peel most templates when a back contact was not used. Shown below is a cross section of AAO on kapton tape (Polyimide). The template is essentially flipped upside down. As a result, bottom on the pores should now be cleaner and be devoid of any non-uniformity that may have arisen during the anodization process. In order to verify that the top and bottom of the template are flipped when transferred on to polyimide, CIS nanowires were only partially electrodeposited. A thin layer of Mo (30 nm) followed by Al₂O₃ (3 nm) were then deposited prior to the transfer onto the polyimide tape as shown in Figure 3.39. Similarly, FAAO with partially and fully grown nanowires of CdS on 250 nm Al are shown in Figure 3.40.
Figure 3.38: FAAO on adhesive polyimide tape

Figure 3.39: FAAO with partially filled CIS nanowires on 30 nm Mo substrate.
Due to the nature of steps involved in the fabrication process, initial experiments resulted in templates that exhibited cracking of the template along the axis normal to that of the peeling axis. This can be attributed to the peeling step where the flexible PI is used to peel the template. This can be seen as shown in Figure 3.41. When the same dual side adhesive PI is supported by a slightly more rigid steel substrate, the amount of cracking was seen to decrease significantly as shown in Figure 3.42.
3.5.3 Conclusion

The flexible AAO (FAAO) thus fabricated will be much more beneficial with a conducting back contact. This is accomplished by sputtering a material of choice along with a thin layer of alumina to increase adhesion prior to peeling off. As a result, the conducting substrate, along with the template can be transferred onto a flexible substrate such as Polyimide or Al with minimal effort. Shown above is FAAO with CIS nanowires filled partially to demonstrate the flipped nature of the templates on Mo substrates.
Chapter 4: CIS Nanowire Arrays on Ohmic Contacts

4.1 Introduction

The absorber layer is by far the most crucial layer in thin films PV devices. Significant gains have been attained by optimization of the processes governing the growth of absorber materials. This emphasis on the growth method of the absorber layer has a lot to do with the cost of manufacturing as well. Close space sublimation (CSS) for CdTe, r.f. sputtering for a-Si and 3-stage co-evaporation for CIS based films have thus far resulted in the highest efficiencies for the respective devices. It is clear from the above mentioned processes that vacuum based methods are crucial for high quality PV thin films. Although most of the high efficiency CIS devices are fabricated using such vacuum based methods, there has been an increased activity in solution based techniques to manufacture thin film solar cells largely due to rapid scalability thus reducing costs. The 3-stage co-evaporation and electrodeposition processes are described to indicate the contrast between the two.

4.1.1 Co-Evaporation

Co-evaporation of constituent elements in a CIGS device is a process that strategically evaporates the metals simultaneously at varying
rates to achieve films of extremely high quality. This is possible because of the extremely flexible nature of process where the stoichiometry of the films can be precisely controlled. Record efficiencies have been possible through this process because gradation of Ga that is hard to incorporate otherwise. Of the different variations, the most efficient method is what is called as the ‘3-stage co-evaporation method’. In this process, a heated substrate is deposited with In, Ga and Se in stage-1, followed by Cu and Se at a higher temperature in stage-2. This results in a Cu-rich film. The desired Cu deficiency is then obtained by depositing In and Ga in a Se ambient in stage-3 (56). It can be seen from the three stages mentioned that Se is included in all the stages while the objective of the different stages was to ensure deficiency of Cu near both the interfaces. This is because elemental Se easily vaporizes, and the presence of additional Se is required to form stoichiometric films. This process of heating or cooling films in a Se ambient is called as Selenization. The 3-stage approach has selenization integrated into the process. Although excellent devices have been fabricated using such a process, it would be an expensive endeavor to scale the same process to manufacture panels at an acceptable cost.

CIS based alloys have also been fabricated using MOCVD (57), spray pyrolysis (58), hydrazine (59), and electrodeposition (60). Each has its share of advantages and disadvantages. Of interest to this proposal is the
electrodeposition method and consequent selenization that is required. More about the method shall be discussed in the following section.

4.1.2 Electrodeposition and Selenization

Electroplating of metals is a very well established science. This field of science has been put to good use by the electronics industry over the past several decades. Much of this work however has been limited to electroplating of single elements like Cu. Electrochemical baths with multiple salts dissolved can be used to simultaneously deposit different materials. The fundamental concept that governs the electrodeposition process is what is called as the redox reaction. As the name suggests, in a redox reaction one species is reduced (gains electrons) while the other is oxidized (loses electrons). By dissolving electron accepting species (Cu$^{2+}$, In$^{3+}$ and SeO$_3^{2-}$) using chloride or sulfate salts, one can obtain a bath from which the three metals can be co-electrodeposited onto a cathode. The concentration of salts in the bath, its pH and the potential applied would then become the three most important factors that dictate the quality and composition of the deposited films. Temperature and current density are other important parameters of the process. The choice of the deposition potential is made based on the standard reduction potentials of each of the ions involved. Based on the Nernst equation, the electrode potentials for elemental Se (+0.74V) and Cu (+0.34V) are more positive
than that of indium (-0.34V) (61). This makes the co-electrodeposition of
stoichiometric CIS a tricky proposition. Many groups have attempted to
achieve device quality films using this method. Most of the theory is based
on experimental work with explanations provided after the fact
hypothesizing observed results. In an ideal case the electrode potentials
for all the elements would be the same for simultaneous codeposition of
the metals. These reduction potentials can however be altered by the pH
and the composition of constituent salts to bring them as close to each
other as possible. Additives such as citric acid, EDTA, ethylene glycol, etc.
are sometimes used as complexing agents in an attempt to reduce the
difference in these potentials.

The pH range within which individual metals are immune to
passivation and corrosion can be understood by what is called as the
Pourbaix diagram. In the case of electrodeposition of a ternary alloy like
CIS, it is crucial then to choose a bath whose pH ensures the immunity of
all the metals involved. The Pourbaix diagrams for elemental Cu, In and Se
are provided in Figure 4.1 along with that of Cu-In-Se system. Clearly, it is
possible to codeposit CIS over a wide range of pH values (0.6-9.5) (62).
The quality of electrodeposited films have improved over the years but recrystallization of the deposited films is a crucial step involved in all CIS fabrication methods. This annealing process is often called ‘Selenization’ since the films are annealed in a Se or H\textsubscript{2}Se ambient. As already discussed, this step is integrated into the co-evaporation process. For electrochemical methods however, due to the lack of a high temperature ambient, an additional annealing step is required. Films are typically selenized at around 450°C in the presence of H\textsubscript{2}Se (63) or at 550°C in a Se vapor flux (64). It is believed that electrodeposition results in a combination of binary and ternary phases of varying compositions (65). Binary phases such Cu\textsubscript{x}Se and In\textsubscript{x}Se\textsubscript{y} are undesirable as they have a significant impact on the device performance. High temperature selenization generally gets rid of these phases (66). Also, it significantly
improves the crystallinity of the film as is usually evident in XRD analyses. Finally, the heat allows for Na diffusion to occur which further improves the grain structure of the film.

A few nanometers thick CIS film was first electrodeposited by Bhattacharya in 1983 (67) on Ti substrates. Much progress has been made since. Photovoltaic devices exhibiting conversion efficiencies as high as 15.4% have been reported (60) using electrodeposition as the method to deposit precursor CIS layers. Additional physical steps were taken in order to adjust the stoichiometry to obtain device quality films. Clearly, that only partially fulfills the advantages of using an electrochemical route to synthesize films. The ultimate goal of this particular field of research would be to produce thin films of device quality without the need for high vacuum and high temperature processes. A positive step in that direction is that stoichiometric films that do not require adjustment via thermal deposition methods have been obtained. Such a method, where only one electrochemical step is used to fully grow the absorber layer, is commonly referred to as the one-step electrodeposition method. Successful fabrication of high efficiency devices via this route could truly reduce manufacturing costs of PV devices in a significant way. Although it is difficult at this point in time to estimate the cost benefit of such an approach on a commercial scale, it is easy to comprehend it.
when electrochemical equipment typically used in laboratories cost less than a third of the typical PVD furnaces.

4.2 Research Objective

The elemental composition of Cu, In and Se is crucial to form semiconducting thin films. Multiple groups have spent well over a decade trying to perfect the art of depositing CIS with only a slightly rich In concentration to be able to make device quality thin films. Much of the difficulty has been due to the spread of reduction potential values of the three elements involved. Even today, only a handful of papers have been published that yield acceptable device efficiencies when CIS thin films are grown exclusively by electrochemical deposition. Since electrochemically depositing CIS nanowires is more controllable and predictable, methods used to electrochemically deposit stoichiometric CIS are adopted. Since alumina dissolves in highly acidic and highly alkaline solutions, enabling the deposition in electrolytes where alumina is not adversely affected during deposition is important. Therefore, the objective was to fill the pores such that compact CIS nanowires are formed. Also, the use of a tungsten interlayer was inevitable. The successful removal of this interlayer without significantly altering the integrity of AAO was therefore imperative.
4.3 Experimental Details

Electrolytes consisting of sulfate salts of Cu and In have typically been reported to yield higher quality films and thus higher efficiencies. Our initial attempts to replicate the same methods published yielded films with much higher concentrations of In than was expected (52). Such compositions generally lead to n-type films as opposed to the p-type absorbers generally preferred. We attempted to optimize this very condition strategically so as to achieve stoichiometric CIS thin films on Mo coated glass substrates. The key parameters involved in this optimization step were the applied potential and the concentration of salts used. Due to the limited availability of Mo substrates, samples were tested one at a time as opposed to an experimental ladder to study the effects over a range of values. Provided below are compositions of CIS thin films for various salt compositions and potentials.

Chloride baths were also used to electrodeposit CIS nanowires. 5.2 mM CuCl₂, 19.2 mM InCl₃, 11 mM H₂SeO₃ and 480 mM LiCl in pH 3 Hydrion buffer solution were typically used. CIS was electrodeposited at -0.6 V (vs SCE) for variable durations. The I-t curve was monitored during deposition. The deposition process was terminated when the current value starts to increase. More details are discussed in the next section. All
experimental methods for the preparation of AAO templates are as discussed in the previous chapter.

CIS nanowires were annealed at 500°C and 550°C for 300 s. The samples were then allowed to sit in 1wt% KCN solution at room temperature for 120s. Heterojunction devices were fabricated by sputtering 100 nm of CdS on the annealed CIS nanowire matrix. Samples were then annealed in Ar ambient at 400°C for 10 minutes followed by applying Ag paste to form the top contact. No attempts were made to optimize the absorption of these devices by integrating TCO layers. The samples were annealed in air at 200°C after the metallization step. IV analysis on several samples was performed.

For some samples the AAO template was dissolved in 5M NaOH for 10 minutes at room temperature. Finally, diode parameters were extracted by fitting the measured data to obtain both the saturation current and the diode ideality factors using Microsoft Excel.

4.4 Results and Discussion

Although considerable effort was put into optimizing the sulfate bath, results similar to the published work were hard to obtain. Therefore, a detailed analysis of different conditions was done to arrive at a condition such that the stoichiometry was slightly In-rich. Based on experimental
data, a slightly different condition yielded optimal conditions compared to what was reported for sulfate baths (63).

Table 4-1: Tabulated results of EDS data for various compositions and potentials

<table>
<thead>
<tr>
<th>Sample</th>
<th>Potential vs SCE</th>
<th>Cu</th>
<th>In</th>
<th>Se</th>
<th>Li</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>-0.55</td>
<td>1.2</td>
<td>12.1</td>
<td>0.6</td>
<td>0</td>
</tr>
<tr>
<td>B</td>
<td>-0.55</td>
<td>1.2</td>
<td>20.4</td>
<td>1.0</td>
<td>36</td>
</tr>
<tr>
<td>C1</td>
<td>-0.45</td>
<td>1.2</td>
<td>23</td>
<td>1.5</td>
<td>31</td>
</tr>
<tr>
<td>C2</td>
<td>-0.55</td>
<td>1.2</td>
<td>21</td>
<td>1.5</td>
<td>36</td>
</tr>
<tr>
<td>D1</td>
<td>-0.45</td>
<td>1.2</td>
<td>20.3</td>
<td>2.0</td>
<td>31.6</td>
</tr>
<tr>
<td>D2</td>
<td>-0.55</td>
<td>1.2</td>
<td>17.8</td>
<td>2.0</td>
<td>32.9</td>
</tr>
<tr>
<td>E1</td>
<td>-0.45</td>
<td>1.2</td>
<td>22</td>
<td>2.5</td>
<td>32</td>
</tr>
<tr>
<td>E2</td>
<td>-0.55</td>
<td>1.2</td>
<td>18.4</td>
<td>2.5</td>
<td>37.3</td>
</tr>
<tr>
<td>F1</td>
<td>-0.45</td>
<td>1.2</td>
<td>23</td>
<td>3.0</td>
<td>33</td>
</tr>
<tr>
<td>F2</td>
<td>-0.45</td>
<td>1.2</td>
<td>23</td>
<td>3.0</td>
<td>34.4</td>
</tr>
<tr>
<td>F3</td>
<td>-0.55</td>
<td>1.2</td>
<td>19.2</td>
<td>3.0</td>
<td>36.6</td>
</tr>
<tr>
<td>F4</td>
<td>-0.55</td>
<td>1.2</td>
<td>20.8</td>
<td>3.0</td>
<td>36.0</td>
</tr>
<tr>
<td>G1</td>
<td>-0.55</td>
<td>1.2</td>
<td>21</td>
<td>3.0</td>
<td>32</td>
</tr>
<tr>
<td>G2</td>
<td>-0.55</td>
<td>1.2</td>
<td>20</td>
<td>3.0</td>
<td>35</td>
</tr>
<tr>
<td>H1</td>
<td>-0.15</td>
<td>1.2</td>
<td>34.27</td>
<td>19</td>
<td>0</td>
</tr>
<tr>
<td>H2</td>
<td>-0.25</td>
<td>1.2</td>
<td>43.24</td>
<td>19</td>
<td>0</td>
</tr>
<tr>
<td>H3</td>
<td>-0.30</td>
<td>1.2</td>
<td>20.7</td>
<td>19</td>
<td>23.11</td>
</tr>
<tr>
<td>H4</td>
<td>-0.45</td>
<td>1.2</td>
<td>18.72</td>
<td>19</td>
<td>26.63</td>
</tr>
<tr>
<td>H5</td>
<td>-0.55</td>
<td>1.2</td>
<td>23.92</td>
<td>19</td>
<td>11.91</td>
</tr>
<tr>
<td>I1</td>
<td>-0.55</td>
<td>1.2</td>
<td>20.3</td>
<td>19</td>
<td>20.97</td>
</tr>
<tr>
<td>I2</td>
<td>-0.35</td>
<td>1.2</td>
<td>22.08</td>
<td>19</td>
<td>20.21</td>
</tr>
<tr>
<td>I3</td>
<td>-0.55</td>
<td>1.2</td>
<td>21.3</td>
<td>19</td>
<td>24.79</td>
</tr>
</tbody>
</table>

From the data above, -0.33 V or -0.34V vs SCE indicate the best stoichiometry. This is so because generally, films after the recrystallization step have a slightly lower Cu/In ratio. Also, depending on the time, temperature and partial pressure of Se in the reactor, a significant portion of the Se could be lost. Most of all reported one step electrodeposited CIS based photovoltaic cells have been selenized in the presence of H$_2$Se – an extremely toxic gas at high temperatures. An alternative to that is the use of elemental Se heated along with the films in the reactor. The
disadvantage to this method despite it being significantly safer is the lack of control. In the home made reactor in our lab, we were able to notice recrystallization but films consistently peeled off at temperatures above 480°C – a common characteristic of films annealed in Se deficient ambient. With little control over pressure, even considerably large amounts of elemental Se proved insufficient to attain device quality CIS thin films. Some devices did however exhibit some rectification. Also, increased conductivity was seen under light as shown in Figure 4.2.

![Figure 4.2: I-V analysis of a planar CIS/CdS device](image)

Unfortunately, a high quality baseline was not able to be achieved despite several other attempts to improve the performance of these films. It may be attributed in a large part to the lack of control over the
selenization reactor resulting in films that consisted of large pin holes. Such pin holes in the absorber layer occur in the electrodeposition step. However, they can be overcome to a large extent by proper recrystallization step. This is so because the semi-molten state of the film during recrystallization compensate for structural non uniformities within the film. With an uncontrolled recrystallization step however, this problem could be amplified resulting in poorly adherent films. These series of experiments helped establish a condition that could be used for the fabrication of CIS nanowires.

Although the quality of the films with sulfate baths was good, the same could not be translated with respect to nanowires. The nanowires grown using sulfate baths were very powdery and had no structural integrity. Chloride baths however resulted in significantly improved nanowires. The most important improvement was that they were very compact.
4.3: CIS nanowires when Sulfate Bath was used.

4.4.1 CISNW on Ti coated glass

As indicated in the previous chapter, Ti was initially used as the back contact material on AAO templates due to an already established process. However, with thicker AAO templates, Ar ion milling was not effective. Consequently, cathodic polarization in dilute KCl solutions helped selectively etch the barrier layer. Because this process was accompanied by significant hydrogen evolution, non-uniformity in the removal of the barrier oxide layer resulted in equally non-uniform filling and growth of CIS nanowires. Similar electrochemical baths were used for electroplating of thin films of CIS. Chloride baths ensured proper nucleation and growth of nanowires at sites where the barrier oxide layer did not exist. The non-uniformity in the growth of CIS nanowire arrays on Ti coated glass substrates was manifested in the growth parameters. In other words, clearly distinguishable patterns indicating the nucleation, growth
and filling of nanowires in AAO templates was not seen in any of the I-t curves monitored during the potentiostatic electrodeposition step.

![Cross section of CIS nanowires in AAO on Ti. Notice the non-uniformity in pore filling. Close-up view of deposited wires.](image)

Wildly fluctuating high current density patterns typically were good signs of any nanowires that may have been deposited. Most samples however were characterized by extremely low currents (~100 nA/cm²). Shown below are two SEM images of well nucleated sites indicating a fairly decent growth of CIS nanowires. However, a slightly larger perspective of the same sample makes it abundantly clear the non-uniformity in the growth across the same sample. Note that the region with overfilled pores is characterized by full length wires whereas the partially filled region is void of any surface layers of CIS. This was expected but what was not expected was for the two varying growth rates on the same sample at such close proximity. This confirmed our theory of non-uniform barrier layer removal as discussed in the previous chapter.
4.4.2 CISNW on Mo/W

Templates on Mo substrates without any interlayers were not suitable for electrodeposition of nanowires because of incomplete anodization resulting from the air/interface region being cut off. Detailed explanation of the same including a model to explain the phenomena are provided in the previous chapter. When tungsten was used an interlayer very high quality and uniform templates were able to be consistently fabricated. Like Mo, W forms WSe$_2$. Hence, it can form a quasi-ohmic contact with CIS like Mo. It has already been reported that tungsten does indeed form an ohmic contact with CIS. It is however not the preferred choice due to the fact that Mo substrates provide lower sheet resistance and high reflectivity than W. The reflectivity of very thin layers of W on Mo substrates was studied. It is clear from the data below that when thin layers of W are used, the reflectivity of Mo layers does in fact increase. Unlike the case used in the study where only one back contact material is used at a time, this is a case where multilayered stack is used and may provide the advantage of improved reflectivity and a better ohmic contact. The conduction band minimum and valence band maximum of WSe$_2$ and MoSe$_2$ are slightly different despite similar band gap values. Both the conduction and valence band of WSe$_2$ are slightly greater than that of MoSe$_2$. If that were true, it conforms to the results reported where tungsten may indeed form a better electrical contact
that Mo. For this design however, it is important that such the WSe$_2$ formed be thinner than the W layer itself. Otherwise, the improvement in the quality of the ohmic contact will be offset by the work function difference between WSe$_2$ and the underlying Mo. Further analysis and optimization of this interlayer scheme is beyond the scope of this project. Some preliminary results do however show that W/Mo and Mo back contact to CIS nanowires have comparable performances.

Figure 4.5: Reflectivity due to thin W layers

Glass substrates with 1600 nm of Mo were supplied by AQT Solar. They were cut cleaned by sonicating in acetone and IPA followed by a DI water rinse and blow dried with nitrogen. The samples are further cleaned in oxygen plasma for 60s to remove any remaining particulates on these samples. 50nm of W was sputtered at a low forward power (30 W)
followed by E-beam evaporation of 500 nm of Al. Anodization and post anodization steps are as described in the previous chapter. Electrochemical deposition was performed using the same optimized conditions that were used for Ti based templates. The as deposited nanowires showed significantly improved morphology. They appeared less flaky and powdery indicating very good conductivity of the templates.

The biggest improvement from the case of Ti interlayer was the drastic change in uniformity. All regions across the template had nanowires of comparable lengths. This was also reflected in the I-t graphs recorded. These plots reflected the different stages of electrodeposition in pores very accurately. An initial spike in current density is associated with the nucleation of the nanowire material at the bottom of the pores. This is followed by a gradual decrease in current due to the resistance added due to the increasing length of the nanowires. When the pores are fully filled, deposition continues resulting in the growth of a thin film over the template. The signature for this on the I-t curve is an increase in current again due to increase in the effective area. It is a good marker for termination of the nanowire growth. Shown below are as deposited nanowires.
Figure 4.6: Uniform growth of compact nanowires was observed across the entire Mo/W substrate.

Figure 4.7: I-t curve indicating the different stages of nanowire growth. Samples were annealed in Ar ambient initially at 500°C for 5 mins. This is done by purging the tube with Ar at room temperature while the
chamber itself is ramped to the set temperature. Once the target temperature is reached, the samples are annealed for a total of 300s and immediately removed from the chamber to cool down rapidly. Because no additional selenium is present in the environment, this RTP like process is used to ensure minimal loss in Se while the required temperature for recrystallization is reached. The samples were structurally intact and no delamination was observed.

To the best of our ability, our search yielded only three reports (68), (69), (52) of vertically aligned CIS nanowire arrays, none of which demonstrates a heterojunction device. Although single nanowire measurements have been made on heterostructures, this demonstrates for the first time the fabrication of vertically aligned CIS nanowire arrays and also forming a diode with the typically used CdS as the window layer. More importantly however is the fact that such a demonstration uses very inexpensive, scalable and relatively fast methods. Similar experiments were conducted at 550°C. The diode ideality factors improved considerably proving that there was still room for improvement of the annealing condition alone. I-V analysis was further performed at several temperatures below room temperature to understand better the transport mechanisms occurring in the device.
It is not clear at this time whether the radial heterojunctions or axial junction architecture will be more beneficial from a device performance standpoint. The advantages and drawbacks for each need to be weighed based on experimental data. Prior work with CdS nanowires indicates that an axial junction between CdS nanowire array and a CdTe thin produced better results (70). Since majority of the absorption occurs in CIS nanowires, the depletion region can be enhanced significantly across the sample in a radial structure increasing the probability of collecting charge. On the other hand however, surface recombination can play an equally detrimental role. With this conundrum, attempts to fabricate both free standing and AAO embedded nanowire arrays were made.

The template was then etched away in 5M NaOH in order to reveal a free standing array of nanowires. This was however not to be the case. As shown in Figure 4.8, when the AAO template is dissolved, the CIS nanowire arrays cannot support themselves on the W layer. This could be due to a couple of reasons. First, the aspect ratio of these nanowires is too high for them to sustain. Second, insufficient adhesion between nanowires and the W film coupled with high aspect ratio could further hurt the prospects of free standing wires. Therefore, from these initial observations, it is clear that for high aspect ratio CIS nanowires on Mo/W substrates, it is important to have AAO present, at least partially. Nanowires scattered across the etched template can be seen on this SEM image.
Figure 4.8: CIS nanowires on W after AAO etch

Figure 4.9: J-V Characteristics of CIS nanowire heterojunction on Mo/W annealed at 550°C
I-V analysis indicates the formation of a good p-n junction. The diode ideality factor was 4.38. Slight improvement was observed when devices were fabricated with Mo being exposed.

Although CIS nanowires have been fabricated on W before (69), no devices have been reported. Tungsten has been shown to work as a good ohmic contact with CIS based materials as well (71). As previously shown in Figure 4.5, Mo/W bilayers may possibly provide improved performance due to improved reflection from the back contact.

4.4.3 CISNW on Mo

The fabrication of AAO on Mo templates has already been discussed. Several methods were tried in order to etch the tungsten surface initially but was met with limited success. With such small features, anisotropy in any etch mechanism was crucial. Since octafluorocyclobutane (C₄F₈) has been widely used as a passivating agent in the past, it was combined with SF₆ to etch away the tungsten interlayer selectively (72). Although some etching of the tungsten was observed, considerable residue remained due to the polymerization of C₄F₈ during the etch process. The presence of this residue however seems to have provided the nanowires with some mechanical stability (Figure 4.8) after the template was etched away unlike the case of CIS nanowires on W as shown in Figure 4.11.
Mixture of SF$_6$ and Ar was eventually the best combination that helped successfully remove tungsten interlayer in order to facilitate an electrical contact between Mo and CIS nanowires. No changes were made to any of the experimental methods involved in the fabrication of CIS nanowires on templates with Mo exposed at the bottom of the pores. Electrodeposited nanowires were annealed face down on glass at 500° C (Sample-A) and 550° C (Sample-B) for 300s. The diode ideality factors
significantly improved when the annealing temperature was raised to 550°C. The samples were generally flipped upside down on clean glass substrates as a reinforcing measure to minimize any loss of Se from the material. XRD of as deposited and samples annealed at 550°C are as shown below. I-V analysis at several temperatures was also performed.

Figure 4.12: CIS Nanowires in AAO with Mo back contact
Figure 4.13: XRD of CIS nanowires in AAO: As deposited and at 550°C

Figure 4.14: J-V characteristics of CIS-CdS on Mo annealed at 500°C

J-V: Dark CISNW-CdS on Mo annealed at 500°C
Figure 4.15: JVT characteristics of CIS-CdS on Mo annealed at 500°C

Figure 4.16: Variation of diode ideality factor and saturation current density with temperature
The exponential rise in current is seen at much lower potential when the annealing condition was adjusted to 550°C for 300s. This reflects a curve more similar to the conventional dark diode curve of a CIS planar device. The currents are also significantly increased indicating a possibly improved crystallinity in the material. An improved annealing profile and optimized CdS/CIS interface can be expected to yield good baseline PV devices. IV analysis of devices annealed at 550°C is as shown in Figure 4.17.

![J-V characteristics of CIS-CdS on Mo annealed at 550°C](image)

Figure 4.17: J-V characteristics of CIS-CdS on Mo annealed at 550°C

Although no photovoltaic effect was detected, an increase in the current density was observed under illumination as shown in Figure 4.17. Diode ideality factor and current density were clearly affected the most.
due to the increase in temperature. This could be attributed to higher recrystallization and conductivity of the nanowire array. At lower temperatures, current transport due to the carrier diffusion is suppressed resulting in a more pronounced contribution of recombination current due to deep level traps and interface states. The best cell on Sample-B on the other hand exhibited an ideality factor of 1.81 at room temperature although saturation current increased significantly. Significantly larger currents were observed in general in the latter case. The linear region at ~0.4V corresponds to the exponential increase in current followed by a saturated region where the rate of current increase drops due to series resistance. At lower voltages however, the relatively high saturation current due to leakage is represented by a linear region with a lower slope. $V_{oc}$ is a strong function of the saturation current density and the absence of a PV effect may be attributed such high values of $J_0$ observed.
Figure 4.18: Logarithmic J-V plot indicates two distinct regions

It is not clear from this study what role AAO template plays in mitigating the surface recombination velocity of the absorber array. With such a large CIS-Al₂O₃ interfacial area, understanding transport and recombination mechanisms at such an interface could go a long way to help achieve efficient PV devices. Although not a fully understood phenomena, the effect of Na in the recrystallization process of CIS has widely been accepted to improve the surfaces of thin films. It is also believed to play an important role in the passivation of grain boundaries (73). Mo films, due to their straw like morphology enable controlled diffusion of Na from soda lime glass substrates. In this case however, the diffusion of Na due to the presence of alumina and larger CIS surface area require more detailed studies. Ex-situ Na incorporation by using NaF
layers may also provide insights into the passivation of grain boundaries and the nanowires themselves.

4.5 Summary and Conclusion

AAO templates on Mo coated glass substrates by using a tungsten interlayer have been fabricated. Selectively exposing Mo using a RIE step ensures the bottom of the pore opens to the Mo substrate. These substrates have been used to successfully grow CIS nanowire arrays using electrodeposition processes. A rapid annealing scheme was used without additional Se to recrystallizes the as deposited nanowires. Structural and electrical properties of these nanowire arrays were studied. To further explore the transport phenomena, CdS/CIS nanowire heterojunction devices were fabricated. I-V analyses indicate that annealing at 550°C yields high quality diodes with a diode ideality of 2.43. Large saturation currents were observed despite excellent rectification indicating that the surface recombination velocities may have increased. Further analysis of the CIS-AAO interface and alternate methods to incorporate Na may help achieve efficient solar cell devices. Notwithstanding above mentioned challenges, this work presents a platform to integrate CIS based semiconductor nanowires for PV devices enabling the conventional Mo/CIS/CdS/ZnO stack.
Chapter 5: LP-EBID of CdS Nanoparticle Arrays

5.1 Introduction

Lithographic methods using focused electron beams (e-beam) to pattern very small features for use in integrated circuits and for mask patterning has been around for decades. However, e-beam lithographic techniques are characterized by low throughput and for that reason it has largely been limited to the confines of academic research and other applications where precision is paramount. Focused electron beam induced deposition (EBID) stemmed from what was initially a problem that researchers had to avoid – contamination due to ion bombardment. It was reported in 1934 (74). This effect was exploited in 1960, where a precursor gas was intentionally injected into a vacuum chamber to subsequently be decomposed by an e-beam (75). An ambient consisting of a precursor is common to both the e-beam etching and deposition schemes. Precursor molecules adsorbed on the substrate surface are broken down into volatile and a non-volatile species in the presence of an electron beam. The fundamental difference between the two processes however is reactivity of the non-volatile species with the substrate. When the non-volatile species adheres to the substrate but reacts to form volatile species, etching occurs while deposition occurs in the case it does
not react (76). Despite its relatively early discovery, very little progress has been made since in deploying the process. However, the last two decades have witnessed significant rise in interest in this field of study. This is evident from the number of publications by year from 1934 to 2008 (76).

![Graph showing popularity of EBID techniques between 1934 and 2008.](image)

**Figure 5.1:** Popularity of EBID techniques between 1934 and 2008 (76)

E-beam induced deposition (EBID) of materials, as mentioned previously requires a precursor. Generally, precursors are the sources of materials that are intended to be deposited. Metal-organic precursors are used in gas phase EBID methods. This is very similar in practice to the growth of thin films using MOCVD. The key difference is that the external energy is focused on extremely small regions of the sample as opposed to the uniform heating of entire substrates. As a result, the chemistry and consequential deposition of materials can be confined to the intended narrow regions on the substrate. Such an approach has been successful in
the growth of features as small as 1 nm (77). With a global pursuit of fabrication methods to achieve smaller features, EBID demonstrates the possibility of significantly scaling down the physical dimensions of components on integrated chips. The availability of gaseous precursors for specific materials is among the leading limitation of further application of this process for a wider array of materials.

A transition from gaseous to liquid precursors opens up opportunities to simplify the EBID process as well as provide a more extensive catalogue of materials that can be deposited. Indeed, a large body of literature exists for electrochemical deposition of thin films, which can be utilized to expand the material sets available to EBID. However, liquids are generally incompatible with the microscopes associated with EBID. Liquid vapors serve to degrade the system vacuum and may cause damage to the optics and electron gun. It is important to shield the apparatus so that it is immune to vacuum around it while being exposed to the e-beam simultaneously. This has been established by the use of commercially available Quantomix cells as shown in Figure 5.2. Liquid precursors have successfully been used so far to deposit high purity Pt (78), Au (79), Ag, Ni, Cr (80) and Si (81).

Extension of the same for binary and ternary alloys is yet to be reported. Gaseous phase EBID is generally characterized by low purity of
elemental deposits (82). The same can be expected for alloys if not worse. This aspect augers particularly well for the LP-EBID technique as the deposits are more pure (81), (83). This work studies the growth of CdS borrowing principles from the chemical bath deposition that is typically used for PV applications. Liquid phase precursors are generally salt based, and lack the carbon and phosphate based ligands used in gas phase precursors - considered to be the primary contamination source in EBID. Previous LP-EBID studies have been limited to one primary reagent in the liquid precursor bath. Hence, the potential for multi-reagent chemistry has not been previously investigated. In this work we demonstrate the versatility of LP-EBID through the deposition and characterization of the semiconductor cadmium sulfide (CdS). CdS has promising applications in opto-electronics and photovoltaics, two fields of research not typically targeted by EBID. Due to its wide direct bandgap, CdS has found a variety of applications in the electronics industry. In the last few decades, it has largely been used as an emitter layer in most thin film solar cells and photodetectors. A growing variety of devices are proving that CdS is a viable material for humidity (84), DNA (85) and gas sensing (86) applications as well. Of particular relevance however, is the application of CdS nanostructures in photonic applications (87). Due to its excellent electronic and optical properties, integration of nanoscale CdS features could pave way to significant improvements in the performance and
efficiency of devices in all of the above mentioned applications. Scientists are only beginning to demonstrate the advantages of photovoltaic devices with integrated nanostructured materials (88), (6). Site specific growth of an emitter material like CdS on absorber features like CdTe and CIS nanowires could perfectly complement and enable a fully integrated process for fabricating nanoscaled photovoltaic devices. Also, CdS nanobelts have successfully been deployed in the fabrication of very high performance nano-MESFETs with ON/OFF current ratio of ~2x10^8 (89). The fabrication of the same however is based on suspension of the material on silicon substrates giving almost no control over the placement of individual nanobelts (90). From a processing standpoint, this simply reinforces the absolute need for processes that enable the growth of site specific CdS nanostructures for scalable purposes.

5.2 Results and Discussion

The Quantomix cell used is as illustrated here. It consists of a stainless steel cell that is lined with a plastic ring. A rubber o-ring provides a seal good enough to ensure that the liquid in the cell is not affected by the vacuum surrounding it. The polyimide film is about 150 nm thick. It is transparent to high energy electrons beams. Precursor solutions for CdS deposition contained 0.02 M cadmium chloride (CdCl₂), 0.015 M Thiourea (SC(NH₂)₂) and 0.0675 M ammonium chloride (NH₄Cl) in DI water.
Quantomix liquid cells (QX-102) were filled with 25 µL of precursor solution, while 50 nm Au spheres were placed on the vacuum side of the polyimide membrane to aid in focusing. Deposition was performed in a Raith e-Line electron beam lithography system operating at 20 keV and beam currents between 150 – 300 pA. Dot arrays were produced with 7×7 elements and a 3 µm pitch with doses ranging from 5 – 200 pC. Arrays with 40×40 elements and pitch sizes of 0.5 and 1.0 µm were deposited for optical analysis. Upon completion of the deposition process, the liquid capsules were removed from the EBL system and the precursor solution was removed. The capsules were twice re-filled with DI water to remove residual precursor solution and let dry overnight. Finally, the top portion of the capsule, containing the polyimide film and metal supporting grid, was removed for ex-situ analysis.

SEM imaging was performed in a FEI Quanta 250 FEG operating in VP mode (0.45 torr) to prevent sample charging. All SEM images shown were taken ex-situ (deposit side up relative to the beam). EDX measurements were taken for 11 nanoparticles at 20 keV using an Oxford X-max detector attached to the FEI Quanta. The NIST DTS-A-II software package was used to simulate x-ray spectra for a 100 nm CdS sphere (including Cl contamination) to confirm the deposit composition. Photoluminescence measurements were performed using a Zeiss Axiovert 405M optical microscope in transmission mode. The CdS deposits were excited using a
405 nm laser diode focused on the sample surface using a 5X objective (N.A. =0.1). Photoluminescence from the nanoparticle arrays was collected using a 20X objective lens (N.A. =0.5) and routed through a longpass filter (cut-on wavelength = 450 nm, Thorlabs Inc.) to separate the luminescence from the excitation light. The luminescence spectrum was resolved using a grating spectrograph (Acton SP-150) fitted with a thermoelectric cooled CCD camera (Princeton Instruments PIXIS 256). A JEOL 2010f operating at 200 keV was used for TEM analysis of deposit nanostructure and phase identification. Samples were sputter coated with a mixture of Au and Pd to prevent charging prior to TEM analysis.

The kinetics governing the growth of CdS thin films via chemical bath deposition have been postulated by several groups (91), (92), (93). Generally, the following reactions are widely accepted to be responsible for the formation of CdS.

\[
NH_4^+ + OH^- \leftrightarrow NH_3 + H_2O \quad \text{..................} \quad (1)
\]

\[
Cd^2_2 + 4NH_3 \leftrightarrow Cd(NH_3)_2^{2+} \quad \text{..................} \quad (2)
\]

\[
Cd(NH_3)_2^{2+} + 2OH^- \leftrightarrow Cd(OH)_2 + 4NH_3 \quad \text{..................} \quad (3)
\]

\[
SC(NH_2)_2 + OH^- \rightarrow S^{2-} + CN_2H_2 + 2H_2O \quad \text{..................} \quad (4)
\]

\[
Cd(NH_3)_2^{2+} + SC(NH_2)_2 + OH^- \\
\rightarrow CdS + 4NH_3 + CN_2H_2 + 2H_2O \quad \text{..................} \quad (5)
\]
The presence of a ligand is essential for controlled nucleation of the film. Addition of NH₄OH simultaneously provides NH₃ and OH⁻ ions. Therefore, hydrolysis of thiourea occurs instantly resulting in spontaneous precipitation of CdS. Decoupling the process of adding NH₃ and OH⁻ ions therefore provides greater control over the nucleation of CdS on the substrate. Ammonia based salts can therefore act as a buffer to this process. The addition of ammonium salts such as NH₄Cl serves two purposes. Due to its mildly acidic nature, it controls the OH⁻ ion concentration. By doing so, all reactions initiated by the hydroxide ions viz. the intermediate formation of Cd(OH)₂ and the hydrolysis of thiourea can be subdued. As a result, the formation of tetraamine complex ions is also
stabilized (93). All solutions used for LP-EBID of CdS therefore contained a buffer ammonia salt. The choice of it being a sulfate or a chloride salt was made to match with corresponding cadmium salt. To further understand the effect of various parameters involved, different salts of cadmium including sulfate, chloride, acetate and iodide salts were studied for their effect on the growth of films grown by the CBD method (94), (92). CdSO₄ yielded films with significantly larger grains (145 nm) than the bath with CdCl₂ (16 nm). Thickness values of the films however were very similar (82-90 nm) for a set time period (94). Initial growth rate on the other hand was reported to 1000 nm/hr for the sulfate bath and 760 nm/hr (92) indicating a considerable contrast that doesn’t fully illuminate the effects of the anions. Clearly, the understanding of kinetics to explain such results is not yet complete.

NH₄OH was not added to any of the solutions to avoid spontaneous precipitation of CdS in the cell. The objective was hence, to study of the effect of a focused electron beam and if it would initiate the reaction mechanisms as discussed for the case of CBD. Experiments conducted included the use of chloride salts of Cd for the LP-EBID of CdS nanoparticles. CdS nanoparticles arrays were successfully fabricated. Some collateral deposition was also found. Varying the concentration of salts did not seem to reduce the amount of collateral deposit.
EDAX analysis of extracted samples yielded a near 50:50 at. % composition confirming the growth of CdS nanoparticles along with significant collateral deposition around the desired patterns. Clearly, there is a noticeable amount of collateral deposit but distinguishable patterns were observed at dosages as low as 10 pC.

Figure 5.3: 40 x 40 CdS pattern at 50 pC

After sample extraction the deposits are imaged facing towards the electron beam, as shown in Figure 5.4 and Figure 5.5. The deposition process is localized around the primary beam spot as shown by the dot array in Figure 5.4, where 20 pC dose yields structures with a diameter of 110 nm. Figure 5.5 shows a 45° tilt image, revealing aspect ratios between...
1:1 and 1:2 for the nanostructures. A dot pitch of 3 µm is used to minimize unintentional, or collateral, deposition to demonstrate the achievable resolution at any particular dose.

Figure 5.4: Extracted sample showing CdS nanoparticles
Figure 5.5: Close up of extracted sample showing CdS nanoparticles

EDX analysis of the deposits reveals a composition of 49.4 ± 1.5 at. % Cd, 44.2 ± 1.3 at. % S, and 6.4 ± 1.6 at. % Cl. The deposits are slightly Cd rich; however the Cd to S ratio remains nearly 1:1 across all samples measured. The primary contaminant is Cl, which is likely incorporated from CdCl₂ and NH₄Cl components of the precursor solution. Incorporation of C and O in the deposits is difficult to quantify as these constituents are present in the supporting polyimide film. To ensure these additional elements are not playing a role in the LP-EBID reaction chemistry, TEM analysis was performed to investigate the internal nanostructure and phase of the deposits. From Figure 5.7, the deposits are polycrystalline with predominant lattice spacings of 3.16 and 3.34 Å, consistent with
hexagonal (JCPDS 80-0006) CdS. The polycrystalline nanostructure is consistent with previous results in gas-phase EBID (95), (96).

Figure 5.6: EDX analysis indicates approximately 1:1 ratio of Cd to S, with 6.4 at. % contamination from Cl
Figure 5.7: HRTEM micrograph detailing the internal nanostructure of CdS deposits. The deposits are comprised of nanocrystallites consistent with hexagonal CdS.

Figure 5.8: Photoluminescence measurements of a 40x40 array with 1 µm dot pitch. The spectra exhibit a primary peak between 515 - 525 nm, consistent with the direct band gap of CdS (2.42 eV, 512 nm).
Further evidence of CdS deposition can be seen in Figure 5.8, where PL measurements of the deposits show a primary peak between 515 – 525 nm. The blue and red lines in Fig. 3 are from separate 40×40 element arrays, showing that the PL peak is similar across multiple depositions. CdS is a direct band semiconductor with a band gap of 2.42 eV (512 nm), consistent with our results. Smytyna et al. investigated PL measurements on CdS nanoparticles whose peaks indicate 520 nm (97). Based on the previous literature and the results shown here, the chlorine contamination likely does not affect the PL response.

Although the choice of Cd salt seems to affect the growth of CdS thin films using the CBD process, the results have been far from conclusive. To that end, LP-EBID of CdS is being conducted using sulfate salts of Cd and ammonium. Initial results indicate similar growth patterns with some collateral deposition; the characterization of the nanoparticles themselves is pending further investigation. Provided below are some images acquired in-situ.
The size and shape of particles relative to those obtained using chloride salts with all other parameters held constant should be able to provide us with some insight into the difference in growth phenomena.
The effect of the buffer salt (ammonium salt) is yet another variable that should help confirm or refute the long standing theoretical models proposing the growth of CdS thin films using CBD. There are a large number of variables whose specific contributions to the end product are yet to be quantified. With carefully designed experiments, it may be possible to precisely control the deposition rate, line width, aspect ratio and possibly the quality of the deposit and thus its crystallinity paving way for site specific growth of device quality CdS nanostructures.

5.3 Conclusion

With the growing relevance of EBID techniques, this work demonstrates the feasibility of adapting CBD based chemistry to synthesize deterministic patterns of a polycrystalline compound semiconductor (CdS) using a liquid precursor. Structural and optical studies were used to confirm the formation of CdS nanoparticle arrays. With respect to CdS alone, a lot remains unknown. Clearly, this method provides considerably greater control and is easier to assess than CBD.

Understanding the mechanisms driving the growth of CdS should help validate some of the theoretical models used to explain the growth of CdS thin films for photovoltaic applications. Despite the presence of materials with better electrical and optical properties for buffer layers in
thin film solar cell devices, CdS continues to yield the best results. Uniformity and simplicity in the growth of very thin CdS films is widely considered to be the reason. Due to its toxicity and increasing demand for solar modules, a strong incentive exists to phase out CdS and make way for other less toxic materials. ZnS(O,OH) has been touted as an alternative that uses similar fabrication methods. Despite having better internal quantum efficiency, the overall efficiency was lower than that of CdS based devices and improving the CBD conditions was necessary (98). Validation of growth models using LP-EBID could greatly benefit the CBD optimization process.

This study has explored one reaction and one material. The study of electrochemical reactions in the presence of an electron beam to deposit alloys for different photonic and sensing applications is yet another avenue that could further affirm the advantages of this fabrication process.
Chapter 6: Summary and Future Work

6.1 AAO Templates on Mo

This work has demonstrated fabrication of AAO templates on Mo substrates. Due to the high rate at which Mo is consumed in typical anodization conditions, a severe restraint is placed on one’s ability to successfully grow AAO templates on it. To that end, a qualitative model depicting the kinetics of anodization at the air/electrolyte interface has been proposed. Experimental work to confirm the same have also been reported. Finally, by using a tungsten interlayer, it has been demonstrated that it is indeed possible to fabricate AAO templates with Mo as the back contact. Subsequently CIS nanowires were electrodeposited on Mo. The fabrication steps involved provide a certain level of immunity to substrates from the electrochemical reactions occurring during anodization. With a very limited number of conducting substrates upon which AAO has been fabricated thus far, the use of other conducting substrates only remains a matter of experimentation. Although no immediate challenges are expected, it is conceivable that some applications may demand the need for AAO on highly unstable substrates such as sodium. Other methods may be required to successfully fabricate AAO on such substrates.
When the tungsten interlayer is oxidized, the base of the template is weakened. AAO templates can be peeled off easily as a result. By coating the top of the template using sputtering or PVD methods before the peeling step, it would then be possible to have AAO on almost any material that can be coated using the aforementioned methods. Thereby, significantly larger number of materials can be used as back contacts. The flexibility of the adhesive layer may be an advantage or a disadvantage depending on the application it is intended for.

Transferring the pattern onto a rigid substrate may require additional thinning of tungsten under AAO. It is conceivable therefore that it may be possible to exfoliate the template using significantly lesser force by doing so. Future work on such a fabrication process may enable the fabrication of templates similar to commercially available Whatman templates but with thicknesses as desired. Physical handling of the same however may require additional care and/or innovative methods.

6.2 CIS Nanowire Arrays

The successful fabrication of CIS nanowire arrays on Mo only accomplishes the first step of physically enabling nanowires in the conventional Mo/CIS/CdS/ZnO for the first time. Devices with the CIS nanowire array - CdS heterojunction were fabricated. Annealing was
performed in the absence of additional Se. This in itself merits an advantage of CIS nanowires over its thin film counterpart due to the fact that typical CIS precursors require the use of a toxic H$_2$Se for selenization. The use of elemental Se on the other hand is very inefficient as only a fraction of the Se is utilized. Also, due to the extremely short annealing step (300 s), the thermal budget is low as well. Structural characterization revealed polycrystalline nature of the nanowires.

I-V analysis showed high rectification indicating the formation of a good diode – the first requirement of any solar cell device. The saturation current density was observed to be high indicating the possibility of high surface recombination velocities due to the increased interface area between CIS and alumina. This might explain the absence of a photovoltaic effect in these devices. Little is known about the impact of alumina on the surface of CIS nanowires. A closer study of the same might be able to illuminate how the interaction between the two surfaces can manifest itself electrically or otherwise.

LP-EBID was used to fabricate patterns of CdS nanoparticles. The liquid precursors used were similar to those used for chemical bath deposition of CdS for typical thin film solar cells. Based on the theoretical explanation of the growth kinetics of CdS thin films, NH$_4$OH was removed from the precursor to prevent spontaneous growth of CdS. By using a
focused electron beam, we were able to grow CdS nanoparticles lithographically. If the premise that OH⁻ ions initiate the growth of CdS thin films using chemical bath deposition is true, then one can confirm that the electron beam interacts with water at the polyimide interface to yield OH⁻ ions and thus selectively initiating site specific growth of CdS. The effect of cadmium salt on the deposition was studied. Collateral deposition was significantly reduced when a chloride salt was used as opposed to a sulfate salt. Further studies into the effect of the buffer salt along with growth rates are required to explain the reduced collateral. This could confirm or refute some fundamental assumptions that have been made to explain the growth of CdS using the traditional chemical bath deposition (CBD). Furthermore, this could pave a path for the growth of high quality window layers on thin films that are Cd free for PV applications.
References


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