A STUDY ON ATOMICALLY THIN ULTRA SHORT CONDUCTING CHANNELS, BREAKDOWN, AND ENVIRONMENTAL EFFECTS

Abhishek Sundararajan

University of Kentucky, abhiss@gmail.com

Right click to open a feedback form in a new tab to let us know how this document benefits you.

Recommended Citation

https://uknowledge.uky.edu/physastron_etds/27

This Doctoral Dissertation is brought to you for free and open access by the Physics and Astronomy at UKnowledge. It has been accepted for inclusion in Theses and Dissertations--Physics and Astronomy by an authorized administrator of UKnowledge. For more information, please contact UKnowledge@lsv.uky.edu.
STUDENT AGREEMENT:

I represent that my thesis or dissertation and abstract are my original work. Proper attribution has been given to all outside sources. I understand that I am solely responsible for obtaining any needed copyright permissions. I have obtained needed written permission statement(s) from the owner(s) of each third-party copyrighted matter to be included in my work, allowing electronic distribution (if such use is not permitted by the fair use doctrine) which will be submitted to UKnowledge as Additional File.

I hereby grant to The University of Kentucky and its agents the irrevocable, non-exclusive, and royalty-free license to archive and make accessible my work in whole or in part in all forms of media, now or hereafter known. I agree that the document mentioned above may be made available immediately for worldwide access unless an embargo applies.

I retain all other ownership rights to the copyright of my work. I also retain the right to use in future works (such as articles or books) all or part of my work. I understand that I am free to register the copyright to my work.

REVIEW, APPROVAL AND ACCEPTANCE

The document mentioned above has been reviewed and accepted by the student’s advisor, on behalf of the advisory committee, and by the Director of Graduate Studies (DGS), on behalf of the program; we verify that this is the final, approved version of the student’s thesis including all changes required by the advisory committee. The undersigned agree to abide by the statements above.

Abhishek Sundararajan, Student
Dr. Douglas R. Strachan, Major Professor
Dr. Tim Gorringe, Director of Graduate Studies
A STUDY ON ATOMICALLY THIN ULTRA SHORT CONDUCTING CHANNELS, BREAKDOWN, AND ENVIRONMENTAL EFFECTS

A dissertation submitted in partial fulfillment of the requirements for the degree of Doctor of Philosophy in the College of Arts and Sciences at the University of Kentucky

By
Abhishek Sundararajan
Lexington, Kentucky

Director: Dr. Douglas R Strachan, Professor of Physics
Lexington, Kentucky 2015

Copyright© Abhishek Sundararajan 2015
ABSTRACT OF DISSERTATION

A STUDY ON ATOMICALLY THIN ULTRA SHORT CONDUCTING CHANNELS, BREAKDOWN, AND ENVIRONMENTAL EFFECTS

We have developed a novel method of producing ultra-short channel graphene field effect devices on SiO$_2$ substrates and have studied their electrical transport properties. A non-linear current behavior is observed coupled with a quasi-saturation effect. An analytical model is developed to explain this behavior using ballistic transport, where the charge carriers experience minimal scattering. We also observe multilevel resistive switching after the device is electrically stressed. In addition, we have studied the evolution of the electrical transport properties of few-layer graphene during electrical breakdown. We are able to significantly increase the time scale of break junction formation, and we are able to observe changes occurring close to breakdown regime. A decrease in conductivity along with $p$–type doping of the graphene channel is observed as the device is broken. The addition of structural defects generated by thermal stress caused by high current densities is attributed to the observed evolution of electrical properties during the process of breakdown. We have also studied the effects of the local environment on graphene devices. We encapsulate graphene with poly(methyl methacrylate) (PMMA) polymer and study the electrical transport through in situ measurements. We have observed an overall decrease in doping level after low-temperature annealing in dry-nitrogen, indicating that the solvent in the polymer plays an important role in doping. For few-layer encapsulated graphene devices, we observe stable $n$–doping. Applying the solvent onto encapsulated devices demonstrates enhanced hysteretic switching between $p$ and $n$–doped states.

KEYWORDS: Graphene Field Effect Devices, Ultra short channel, Electrical Breakdown, Environmental doping

Author’s signature: Abhishek Sundararajan

Date: March 12, 2015
A STUDY ON ATOMICALLY THIN ULTRA SHORT CONDUCTING CHANNELS, BREAKDOWN, AND ENVIRONMENTAL EFFECTS

By
Abhishek Sundararajan

Director of Dissertation: Douglas R Strachan
Director of Graduate Studies: Tim Gorringe
Date: March 12, 2015
I consider myself to be privileged to have known, worked with, and mentored by my advisor Prof. Douglas Strachan. He has been a constant source of inspiration and motivation throughout my course of study. His vast store of ideas and his unbiased way of sharing them with his students has made doing science most enjoyable. I am deeply indebted for his generosity in accepting me as his student, and showing me the ropes in becoming a better researcher and a better person.

I am grateful to all my dissertation committee members for their valuable suggestion and insightful discussions during our yearly review meetings.

I would like to thank Prof. Beth Guiton and Dr. Guohua Li, for providing me an opportunity to learn and contribute to their research.

I acknowledge the Department of Physics and Astronomy for providing me with an opportunity to do research, and for supporting me with a Teaching Assistantship during my initial and final course of study.

The triumph of science is in collaborative efforts. In this regard, I am delighted to have a very friendly and smart group of people as my co-workers. I heartily thank Patrick Hunley, Mathias Boland, Mohsen Nasser, Javad Farrokhi and, Vinayak Bhat, for their suggestions, support and most importantly their comradery. I wish to thank our former postdoctoral scholar Stephen Johnson, for teaching me to use electron beam lithography and LabVIEW program, which are used mainly in fabricating and electrical testing of graphene devices.

Family and friends have been a constant source of comfort throughout my entire journey. I wish to acknowledge all who have encouraged me and supported me with my choices. Mainly I thank my father, Mr. Sundararajan, for being supportive and patient with me, and my wife, Gayathri, for being very understanding and comforting. I could not have come so far without them.
Dedicated to my family
&
In loving memory of my mother.
# CONTENTS

Acknowledgments ................................................................. iii

Contents ........................................................................ iv

List of Figures ................................................................... vi

List of Tables ...................................................................... vii

Chapter 1 Introduction ......................................................... 1
  1.1 Motivation ...................................................................... 1
    1.1.1 Short Channel Effects in MOSFET ......................... 2
    1.1.2 MOSFET Design ................................................... 5
  1.2 Graphene and Its Role .................................................. 6

Chapter 2 Electronic Structure of Graphene ............................. 7
  2.1 Energy Band Structure: Tight-Binding Model .................. 7
    2.1.1 Tight-Binding Hamiltonian ................................... 7
    2.1.2 Application to the Graphene Lattice ...................... 9
  2.2 Electronic Transport In Graphene .................................... 12
    2.2.1 Diffusive Regime: Boltzmann Transport ................. 12
    2.2.2 Ballistic Transport: Landauer Formula .................. 15
    2.2.3 Quantum Transport: Klein Tunneling .................... 18
  2.3 Tuning the Electronic Structure Of Graphene ................... 22
  2.4 Scope Of Present Work ................................................ 24

Chapter 3 Ultra-Short Channel Graphene Field Effect Device ........ 25
  3.1 Introduction ............................................................... 25
  3.2 Experimental Setup .................................................... 26
    3.2.1 Sample Preparation ............................................. 26
    3.2.2 Ultra-Short Channel Fabrication ......................... 26
    3.2.3 Electrical Characterization ................................... 27
  3.3 Results ......................................................................... 29
    3.3.1 Single Layer Graphene Device: I-V Characteristics .... 29
    3.3.2 Bilayer Graphene Device: I-V Characteristics .......... 32
    3.3.3 Resistive Switching .............................................. 33
  3.4 Device Modeling .......................................................... 33
    3.4.1 Model ................................................................. 34
    3.4.2 Results .............................................................. 37
  3.5 Conclusions ............................................................... 38

Chapter 4 Electrical Breakdown of Graphene ......................... 39
LIST OF FIGURES

1.1 NMOSFET .......................................................... 2
1.2 Threshold voltage lowering ...................................... 4

2.1 Electron hopping .................................................. 8
2.2 Graphene Lattice .................................................. 9
2.3 Graphene band Structure ......................................... 11
2.4 Ballistic conductor ................................................ 16
2.5 Tunneling through a potential barrier in graphene .......... 20
2.6 Schematic of top gate doping .................................... 24

3.1 Nanogap formation on top of graphene ......................... 27
3.2 Electromigration of metal on graphene ......................... 28
3.3 SEM of nanogap over SLG ....................................... 29
3.4 Non-linear I-V characteristics: SLG device .................. 30
3.5 dI/dV plots: SLG device ....................................... 31
3.6 I-V simulation ..................................................... 37

4.1 Schematic of experimental setup used ......................... 40
4.2 Flow chart to explaining feedback control method .......... 41
4.3 Electrical stressing cycles data .................................. 42
4.4 SEM image of break junction ................................... 43
4.5 AFM height after one ES cycle ................................ 44
4.6 Simulated temperature rise ..................................... 45
4.7 SEM image of heating residue .................................. 46
4.8 Simulated thermally-induced stress ............................ 47

5.1 A Schematic of experimental setup used for electrical testing 51
5.2 Variations in conductivity of graphene exposed to various environments 52
5.3 Polymer capping of single-layer graphene device ............ 53
5.4 Finite element analysis of capacitance with polymer capping 55
5.5 Polymer processing dependent doping in Few-layer graphene device 56
5.6 Role of solvent in hysteretic switching .......................... 57
5.7 Reduction of hysteresis with polymer encapsulation and annealing 58
5.8 Effect of humidity and oxygen on hysteresis of PMMA capped device 59

1 Lithography steps to fabricate GFET .............................. 67
LIST OF TABLES
Chapter 1 Introduction

1.1 Motivation

In the history of Physics there have been several instances where discovery of a new material, or an adventitious new idea, has revolutionized the field and opened new pathways for further scientific triumphs. Such discoveries have profound influence not just on the scientific community, but also on the general public, as they spark the innate curious nature of humans. The technological progress that has happened in the past few decades, namely the “Digital Age” and “Information Age”, is mostly in part due to discoveries made in Solid State Physics research. Solid State Physics is a branch of physics that is concerned with new materials and their novel electronic properties.

The invention of Field Effect Transistor (FET) has been one of the key inventions that has fueled the present day technological advancements. An FET is an electronic device in which an external electric field is used to control the conductivity of the semiconductor channel material that has one type of majority charge carrier. Silicon is the most common material used as a semiconductor channel although there are many newer materials that have started to replace it. There are several different types of FETs that are produced for various applications. The channel material can be doped to produce one type of majority charge carriers (either $n$-type: electron: negative charge, or $p$-type: hole: positive charge). Additionally the contacts to the channel, namely the source and drain, can also be doped either similar to the channel or opposite to the channel material to produce enhanced conductivity control. Field effect transistors are also distinguished based on the type of insulation constructed between the gate (the contact that controls the external electric field) and the channel. One of the most common type is called MOSFET (Metal-Oxide-Semiconductor FET) where a thin insulating oxide layer is used between the channel and the gate. In the case of a silicon channel material $SiO_2$ is the popular choice. Figure 1.1 shows a cross section of a $n$-type MOSFET.

With enhancements in semiconductor processing technologies, a tremendous improvement in fabricating these FETs has been achieved. This fabrication trend has been following the so called “Moore’s Law” where the observed number of transistors in a dense array of integrated circuits doubles approximately every two years.[1] Such exponential improvement calls for smaller circuit components, achieved by decreasing the size of FETs. This trend of shrinking size-scale is bound to saturate since one cannot keep making smaller devices, and also since “Moore’s Law” is just an observation and not a physical law of nature. The physical laws that prevent the scaling of FETs to any arbitrary size are discussed in following section.
The following two sections are adapted from textbooks and an online resource [2–4].

1.1.1 Short Channel Effects in MOSFET

Let us consider an $n$–type MOSFET as shown in Fig 1.1 and analyze the key parameters for its operation. The source and drain contacts are doped opposite ($n$–type) to the body or channel material ($p$–type). The majority charge carriers in the channel under no bias condition is $p$–type. There is also a depletion region being formed at the interface of the source drain contacts and the channel. This depletion region is similar to a depletion region formed in a $p – n$ junction device.

When a positive gate voltage is applied, the electric field drives the majority charge carriers away from a region close to the oxide-channel interface, thus creating a carrier-free region of immobile minority charge carriers. The minimum gate voltage at which the minority charge carriers are able to bridge the source and drain contacts is called the Threshold Voltage. The current flow is due to electrons that accumulate close to the gate oxide, which is why this type of MOSFET is called NMOSFET since the current carrying charge carriers are the minority in the channel. Some of the critical parameters that need to be addressed when scaling the FETs are

- Length/ extent of depletion region.
- Channel length. (Usually referred to as the effective length of gate oxide)
- Amount of doping in channel.
- Threshold gate voltage at which current starts to flow.
- Gate oxide thickness - this controls the oxide capacitance.

As the FETs are scaled down in size, certain rules need to be followed in order to preserve the long-channel behavior of the same FET. Inevitable deviations to this behavior are termed “Short-Channel Effects”. These arise due to two-dimensional potential distribution and high electric fields present in the channel. The potential distribution in the channel becomes dependent on both the transverse field $E_y$ (controlled by the gate voltage) and the
longitudinal field $E_x$ (controlled by the source-drain bias). In other words, the potential distribution becomes two dimensional, and the gradual channel approximation (i.e., $E_y \gg E_x$) is no longer valid. There are several undesirable electrical effects that come into play as the channel length is shortened.

**Drain-Induced Barrier Lowering (DIBL)**

With shrinking length of channel the depletion region of the drain contact extends and merges with the source, at this point punch-through occurs. Punch-through is an effect where the current in the channel does not flow close to the inversion layer which is close to the gate oxide-channel interface, rather the charge carriers flow through the bulk of the channel. The current flow in the channel depends on creating and sustaining an inversion layer on the surface. If the gate voltage is not sufficient to invert the surface (Gate Voltage $<$ Threshold Voltage), the carriers (electrons) in the channel face a potential barrier that blocks their flow. Increasing the gate voltage reduces this potential barrier and, eventually, allows the flow of carriers under the influence of the channel electric field. In small-geometry MOSFETs, the potential barrier is controlled by both the gate-to-source voltage and the drain-to-source voltage. If the drain voltage is increased, the potential barrier in the channel decreases, leading to drain-induced barrier lowering (DIBL). The reduction of the potential barrier eventually allows electron flow between the source and the drain, even if the gate-to-source voltage is lower than the threshold voltage. The channel current that flows under this conditions is called the sub-threshold current. Punch-through can be minimized with thinner oxides, larger substrate/channel doping, shallower junctions, and obviously with longer channels.

**Surface Scattering**

As the channel length becomes smaller due to the lateral extension of the depletion layer into the channel region, the longitudinal electric field component $E_x$ increases, and the surface mobility becomes field-dependent. Since the carrier transport in a MOSFET is confined within the narrow inversion layer, and the surface scattering (that is the collisions suffered by the electrons that are accelerated toward the interface by $E_y$) causes reduction of the mobility, the electrons move with great difficulty parallel to the interface, so that the average surface mobility, even for small values of $E_x$, is about half as much as that of the bulk mobility.

**Velocity Saturation**

The performance short-channel devices is also affected by velocity saturation, which reduces the transconductance in the saturation mode. At low $E_x$, the electron drift velocity $\theta_{de}$ in the channel varies linearly with the electric field intensity. However, as $E_x$ increases above $10^4 V/cm$, the drift velocity tends to increase more slowly, and approaches a saturation value of $\theta_{de} = 10^7 cm/s$ around $E_x = 10^5 V/cm$ at 300 K. The drain current is limited by velocity saturation instead of pinchoff in this regime. This occurs in short-channel devices when the dimensions are scaled without lowering the bias voltages.
Figure 1.2: Dependence of threshold voltage on channel length and drain bias. Figure is obtained from [2].

**Hot Carrier Effect**

Electric fields tend to be increased at smaller geometries, since device voltages are difficult to scale to arbitrarily small values. As a result, various hot carrier effects appear in short channel devices. The field in the reversed biased drain junction can lead to impact ionization and carrier multiplication. The resulting holes contribute to substrate current and some may move to the source, where they lower source barrier, which results in electron injection from the source into the $p-$region. In fact an $n-p-n$ transistor can result within source channel drain configuration and prevent gate control of the current.

Another hot electron effect is the transport of the energetic electrons over (or tunneling through) the barrier into the oxide. Such electrons become trapped in the oxide, where they change the threshold voltage and I-V characteristics of the device. Hot electron effects can be reduced by reducing the doping in the source and drain regions, so that the junction fields are smaller. However, lightly doped source and drain regions are incompatible with small geometry devices due to contact resistances and other similar problems.

**Threshold Voltage Variation**

One of the key parameters that controls the operation of FETs is the threshold voltage $V_T$. In the case of long channel MOSFETs, the gate has control over the channel and supports most of the charge. As we go to short channel lengths as seen in Figure 1.2, the threshold voltage begins to decrease as the charge in the depletion region is now supported by the drain and the source also. Thus the gate needs to support less charge in this region and as a result, $V_T$ falls down. This phenomenon is known as the *charge sharing effect*. This lowering of $V_T$ causes the device to have leakage current that in turn cause power loss and poor electrical response of the device.
1.1.2 MOSFET Design

So far, silicon MOSFETs have been the major workhorse of the electronics industry. As such, the MOSFET channel length and other dimensions have been pushed to shrink for the benefits of performance and density. While there is much discussion on what dimensions the scaling limits occur at, it is certainly true that device scaling is getting increasingly difficult and has diminishing returns. Many device structures have been investigated to control short-channel effects and improve MOSFET performance, these include:

- **Channel Doping Profile**: The doping level in the channel is slightly reduced in the region below the oxide-channel interface. The low concentration at the surface has the advantages of higher mobility due to reduced normal field and low threshold voltage.

- **Gate Stack**: The gate dielectric material has been $SiO_2$ since the inception of the MOSFET, but as the device scales are reduced, physical problems such as charge tunneling start to appear. To overcome such issues, other materials with higher dielectric constants (high-$\kappa$ materials) have been actively sought after. In comparison to $SiO_2$, higher $\kappa$ materials can have equal or greater gate capacitances with thicker profile, thus reducing both the electric field as well as technological issues such as defects. Materials of interest are $Al_2O_3$, $HfO_2$, $ZrO_2$, $Y_2O_3$, $La_2O_3$, $Ta_2O_5$, and $TiO_2$.

- **Silicon On Insulator (SOI)**: High quality single-crystal silicon is sandwiched between insulating materials, thus confining the channel material, and controlling the transverse electric field more precisely. The advantages of the SOI substrate include improved MOSFET scaling due to its thin body. A thin body can alleviate most problems with punch-through such that the channel can be lightly doped. The buried oxide layer serves as good isolation to reduce capacitance to the substrate, giving rise to higher speed.

- **Three Dimensional Structures**: A design that allows optimal scaling is a MOSFET whose channel is an ultra-thin layer such that the channel is fully depleted under the whole bias range. A design to achieve this more efficiently is to have a surround gate structure that encloses the body layer from at least two sides. Such devices have already overcome the fabrication challenges and are presently being commercially produced.

- **New Channel Materials**: Alternatives to pure silicon as the channel material have been pursued to improve MOSFET performance and scaling. Performance for devices using materials that are strain-engineered, or that have higher charge carrier mobilities have been investigated. Materials include $Ge$, $InAs$, $InSb$, $GaAs$, $In_{0.53}Ga_{0.47}As$, strained $Si_{1-x}Ge_x$, strained $Si$. 
1.2 Graphene and Its Role

The electronics industry is at a major crossroads, with increasing demand for faster and smaller devices, and technologically challenging process integration of new transistor structures and channel materials. As a plethora of electronic devices and gadgets become available for almost all applications, the challenge in keeping up with consumer demand is undoubtedly increasing. Currently there is an active search for non-traditional channel materials whose electrical properties can be controlled by electric field, and can be scaled. Some of the interesting materials include organic semiconductors and carbon nanotubes. Moreover, having a material that is just one atomic layer thick, whose conductivity can be controlled, would be ideal for scaling devices. This is possible with one of the new channel materials, **Graphene**, which has proved to be a strong contender in either replacing or complementing existing Silicon based electronics.

In the last decade, the scientific community has seen a huge surge in graphene research. All this started when the electric field effect was first observed in few-layer graphene films at room temperature\[5\]. Graphene is a naturally occurring two-dimensional (2D) material made up of only carbon atoms arranged in honeycomb type structure made out of hexagons. Graphene is a semi-metallic material in which the charge carriers can be switched between electrons and holes by changing the gate voltage. Owing to its 2D nature all the charge carriers are on its surface, thus making graphene very sensitive to its external environment\[6, 7\]. Some of the interesting properties of graphene are its charge carriers exhibit giant intrinsic mobility, have zero effective mass, and can travel for micrometers without scattering at room temperature\[8\]. Graphene can sustain high current densities and shows record thermal conductivity and stiffness. It has an intrinsically high Tensile strength of 130 $GPa$, and Young’s Modulus of 1 $TPa$, this makes it the strongest material ever to be tested\[9\]. Graphene is the first of many other 2D materials ($h-\text{BN}$, $MoS_2$, $NbS_2$, $MoSe_2$, $WSe_2$, …) that have followed and have been under scientific inquiry.

In this study we focus on the electronic properties of graphene at ultra-short channel length scales. Our study provides insight into the charge carrier transport phenomenon involved at technologically relevant length scales. We also study the evolution of electrical properties of few-layer graphene devices as they experience electrical breakdown at high current densities. Our observations provide insight into a possible mechanism of graphene break junction formation. In addition, we study the effect of environment on graphene devices. Our unique approach of encapsulating the graphene devices with polymer and observing the electrical transport, provides us with a novel standpoint of locally doping graphene, which could be useful in studying superlattice structures with graphene. We start with a discussion of the fundamentals of the electronic properties of graphene in the next chapter.
Chapter 2 Electronic Structure of Graphene

2.1 Energy Band Structure: Tight-Binding Model

The motion of electrons in a solid differs from that in free space. In a solid, the electrons experience a periodic potential due to the ions in the periodic lattice. The tight-binding model presents a simplistic way of understanding the electron motion in the presence of the periodic potential and is also practically applicable.

2.1.1 Tight-Binding Hamiltonian

We begin by considering to first approximation that the electrons are attracted to the ionic centers due to Coulomb interactions. We then modify the simple atomic picture of an electron bound to a single ion by introducing coupling, where electrons are allowed to hop from one ionic site to another. This originates from the fact that the electronic wave functions for each ion has a finite overlap with its neighbors.

Let us consider the motion of electrons on a hexagonal ring as shown in Fig 2.1. For a simple argument we consider that at each site $i$ there is a potential well that has only one energy level, with energy $-\epsilon_0$. This means when the electron occupies that level, the system has an overall energy of $-\epsilon_0$ and if there is no electron in that state then the system energy is zero.

The Hamiltonian in second-quantized notation can be written as $H = -\epsilon_0 c_i^\dagger c_i$. Here the Hamiltonian is an operator whose expectation value gives the energy, and $c_i^\dagger c_i$ will measure the number of electrons in that state. Thus we can rewrite the previous statement as $\langle H \rangle = -\epsilon_0 \langle c_i^\dagger c_i \rangle$. Generalizing the present case to $N$ identical potential wells, each having same binding energy $-\epsilon_0$, the Hamiltonian can be written as $H = \sum_i (-\epsilon_0) c_i^\dagger c_i$, where $c_i^\dagger c_i$ measures electron occupation in the $i$-th site. This statement can be visualized as

\[
\text{(total energy)} = \sum_i (-\epsilon_0) \times \text{(number of electrons at site $i$)}
\]

This simplistic view is not sufficient in explaining real situations. According to quantum mechanics, the wave functions localized at adjacent sites have a non-zero overlap which in turn allows electron tunneling between the localized levels. This tunneling is what aids the electron to hop from site $i$ to an adjacent site $i + 1$. Thus the Hamiltonian needs to be adjusted to include this tunneling effect, which then reads

\[
H = -\epsilon_0 \sum_i c_i^\dagger c_i - t \sum_i (c_{i+1}^\dagger c_i + c_i^\dagger c_{i+1}) \quad (2.1)
\]

Here $t$ is a number that tells us how strong the tunneling effect is, and the term $c_{i+1}^\dagger c_i + c_i^\dagger c_{i+1}$ represents the “hopping”. For example consider a state $|1\rangle_i |0\rangle_{i+1}$ (where $i$ = occupied, and $i + 1$ = empty), the term $c_{i+1}^\dagger c_i$ acting on this state will give $|0\rangle_i |1\rangle_{i+1}$. If $t$ is
non-zero, an electron can hop from \( i \) to \( i + 1 \), and since there is no other external influences, it can continue hopping from \( i + 1 \) to \( i + 2 \) and so on. Thus the electron can make a complete trip around the ring and come back to its initial position. This phenomenon is generally known as “electron delocalization”.

The eigenstate of the Hamiltonian in Eq.2.1 can be written as

\[
c_i = \sum_k \left( \frac{1}{\sqrt{N}} e^{i k r_i} \right) c_k, \quad c_i^\dagger = \sum_k \left( \frac{1}{\sqrt{N}} e^{-i k r_i} \right) c_k^\dagger \tag{2.2}
\]

Here \( r_i = i a \) for the \( i \)-th site, and \( a \) is the lattice constant. \( c_k \) is an operator that removes a particle from site \( k \) just as \( c_i \) is an operator that removes a particle from site \( i \). Since we have chosen a ring structure this imposes a boundary condition such that \( c_{i+N} = c_i \), where \( N = 6 \) in our case. The operator written in Eq.2.2 should also have this property.

\[
c_{i+N} = \sum_k \frac{1}{\sqrt{N}} e^{i k (r_i+N a)} c_k = \sum_k \frac{1}{\sqrt{N}} e^{i k r_i} \times e^{i N k a} c_k \tag{2.3}
\]

The above equation will be valid if \( e^{i N k a} = 1 \). This in-turn will be satisfied only when \( k = (2\pi/Na) \times integer \). We label these integer values by \( m \), and write \( k = 2\pi m/Na \). Now the summation \( \sum_k \) is a sum over all \( m \) values. Thus,

\[
c_i = \frac{1}{\sqrt{N}} \sum_m \exp \left[ 2\pi i \frac{m}{N} \cdot \frac{r_i}{a} \right] c_m \tag{2.4}
\]

Notice that in the above expression \( m \) values that differ by some multiple of \( N \) always give the same value of the exponential. Thus, not all \( m \) values are independent. Moreover, for all \( m = 0, 1, 2 \ldots, N - 1 \), the exponential gives different values, whereas other values will give identical exponential values from the set \( m \in \{0, \ldots, N - 1\} \), and therefore are not independent. This places an upper bound on the sum in Eq. 2.4 so that,

\[
c_i = \frac{1}{\sqrt{N}} \sum_{m=0}^{N-1} \exp \left[ 2\pi i \frac{m}{N} \cdot \frac{r_i}{a} \right] c_m \tag{2.5}
\]
From the second-quantization formalism used above, we recognize $c_m$ and $c_m^\dagger$ as annihilation and creation operators associated with the state labeled by $m$ or $k$, where $k$ is a momentum eigenvalue given by $k = \frac{2\pi m}{Na}$, and the operators $c_m, c_m^\dagger$ add/remove a particle at the momentum eigenstate labeled $k$. Now substituting Eq. 2.5 into the Hamiltonian Eq. 2.1 and re-arranging terms we obtain

$$H = \sum_k (-\epsilon_0 - 2t \cos ka)c_k^\dagger c_k = \sum_k \epsilon_k c_k^\dagger c_k$$

(2.6)

With $\epsilon_k$ as eigenenergy, the above equation can again be visualized as

$$(total\ \text{energy}) = \sum_k (\text{energy of } k\text{-state}) \times (\text{number of electrons in } k\text{-state})$$

If we now let $t = 0$, then we get back the eigenstate labeled by site $i$ where the particle is localized. Since $t \neq 0$, the correct eigenstates are determined by different values allowed for definite momentum $k = (2\pi/Na)m$. There are $N$ different $m$ values leading to $N$ independent eigenstates that have an energy given by $-\epsilon_0 - 2t \cos(2\pi m/N)$. In the case when $t = 0$, there are $N$ different eigenstates in respect to $N$ different localized sites. Even with $t \neq 0$ we still have same number of states, but the difference is that they are all extended. This critical difference allows the electrons to be delocalized and spread out in the presence of potential barriers.

2.1.2 Application to the Graphene Lattice

Figure 2.2: The graphene lattice has two inequivalent sites. The unit cell has two atoms, and the structure is an example of a non-Bravais lattice.

In graphene, the carbon atoms are arranged in a hexagonal lattice structure, with all of the carbon atoms lying on the same plane. There are two inequivalent lattice sites namely the A-site and the B-site, and the unit cell that repeats to form the lattice has one of each site (see Fig.2.2). This type of structure is a good example of a non-Bravais lattice, where there is more than one atom per unit cell. The operators that act on the two lattice sites can be independently written as,

$$c_i^A = \frac{1}{\sqrt{N_A}} \sum_k c_k^A \exp[i k \cdot r_i]$$

$$c_i^B = \frac{1}{\sqrt{N_B}} \sum_k c_k^B \exp[i k \cdot r_i]$$

(2.7)
here \( r_i \) refers to the coordinate of each lattice site. The tight-binding Hamiltonian for such a hexagonal lattice can now be written as

\[
H = -t \sum_{i \in A} c_{Bj}^\dagger c_{Ai} - t \sum_{i \in B} c_{Aj}^\dagger c_{Bi} - \mu \sum_{i \in A} c_{Ai}^\dagger c_{Ai} - \mu \sum_{i \in B} c_{Bi}^\dagger c_{Bi}
\]  

(2.8)

One can write the Hamiltonian in momentum space using Eq. 2.7

\[
H = \begin{pmatrix} c_{Ak}^\dagger & c_{Bk}^\dagger \end{pmatrix} \begin{pmatrix} -\mu & -t \sum_{j \in i} e^{-ik \cdot (r_j - r_i)} \\ -t \sum_{j \in i} e^{ik \cdot (r_j - r_i)} & -\mu \end{pmatrix} \begin{pmatrix} c_{Ak} \\ c_{Bk} \end{pmatrix}
\]  

(2.9)

Diagonalizing the matrix gives the energy spectrum of the hexagonal lattice as

\[
\epsilon_k = -\mu \pm \left| \sum_{j \in i} e^{ik \cdot (r_i - r_j)} \right|
\]

\[
= -\mu \pm \left| e^{ik_x} + e^{ik_x/2 + i\sqrt{3}k_y/2} + e^{ik_x/2 - i\sqrt{3}k_y/2} \right|
\]

\[
= \mu \pm \left| 3 + 2 \left( \cos \left( \frac{k_x}{2} + \frac{\sqrt{3}}{2} k_y \right) + \cos \left( \frac{k_x}{2} - \frac{\sqrt{3}}{2} k_y \right) + \cos \sqrt{3} k_y \right) \right|
\]  

(2.10)

The \( \pm \) sign refers to two different energy values allowed for a given \( k \) value. The + sign denotes the conduction band (\( \pi^* \)) and the – sign represents the valance band (\( \pi \)).

Figure 2.3a represents the energy dispersion of graphene in momentum space as calculated in Eq. 2.10. The valence and conduction bands touch each other at six specific isolated points in \( k \)-space and are called Dirac points or Neutrality points. Symmetry allows the six points to reduce to two, namely \( k \) and \( k' \) points. Other high symmetry points in the graphene brillouin zone and their associated energy dispersion are shown in Fig 2.3c. If we focus on low energies, which are relevant to electron transport, the bands have a linear dispersion and the conduction and valance band can be visualized as two cones touching each other at the Dirac point (See Fig 2.3b). The consequences of such a band structure are quite interesting when compared to regular semiconductors. We can broadly see four qualitative differences between 2D graphene and 2D semiconductor systems (Inversion layer in MOSFETs, heterostructures, quantum wells, etc).

I. 2D semiconductors typically have large (> 1eV) band gaps. In contrast graphene is a gapless semiconductor with charge carriers transitioning from electrons to holes at the Dirac point in a single structure. In other words, the chemical potential (Fermi level) in graphene is always in the conduction band (n-type doping) or the valence band (p-type doping). Whereas semiconductors become insulating below certain voltages when the Fermi level enters the band gap.

II. The charge carriers are chiral in graphene, while in 2D semiconductors they are nonchiral. The chirality of charges in graphene play an important role in quantum transport behavior. (For example, the Klein tunneling is observed in graphene)
III. Single layer graphene has a linear dispersion, while semiconductors have a quadratic dispersion. This leads to significant differences in transport properties of the two systems. The low energy linear dispersion $E = \hbar k v_F$, leads the charge carriers in graphene to behave like massless Dirac Fermions,[12] and can be described by a Dirac-like Hamiltonian with the speed of light being replaced by the Fermi velocity $v_F \approx c/300$.

IV. The charge carriers in graphene are confined to two dimensions since graphene is just one atomic layer thick. In 2D semiconductor structures confinement is due to an external electric field and has a finite width. Therefore, they are only quasi-2D systems.
2.2 Electronic Transport In Graphene

The dynamics of electron flow in a material can be understood by making certain approximations. Electron flow can be visualized as a slow process of diffusion, or steady drift with an applied external bias, or unimpeded transmission within the bulk of the material. A parameter that delineates the processes is called the Mean Free Path $\lambda_m$ and is defined as the average distance an electron travels before it is scattered. If $\lambda_m \ll L$ the length of the material, then we have diffusive transport, and when $\lambda_m \gg L$ we have ballistic or unimpeded transport. We shall discuss both types of transport process here.

The contents of the following sections are adapted from [11–16]

2.2.1 Diffusive Regime: Boltzmann Transport

In 1872 Ludwig Boltzmann devised an equation that describes the statistical behavior of systems in non-thermodynamic equilibrium. Although the original Boltzmann equation was derived using generalized Newton’s laws of motion, here we take a semi-classical approach by using concepts such as band structure and Fermi distribution.

Let us consider an electron moving under the influence of external electric field $\vec{E}(\vec{r})$. The equations of motion can be written as

$$\frac{d(\vec{h}\vec{k})}{dt} = -\nabla_r E_c(\vec{r}) = -q\vec{E}(\vec{r}), \text{ Similar to } \left\{ \frac{d\vec{p}}{dt} = \vec{F}_e \right\}$$

Here $E_c$ is the energy at the bottom of the conduction band and varies slowly on the scale of electron wavelength. If we consider just one dimensional motion the phase-space trajectory of this particle can be represented in 2-dimensions. This trajectory $\vec{T}$ will now be a function of momentum $p_x = \hbar k_x$ and position $x$ which are both a function of time $\vec{T}(t) = [x(t), p_x(t)]$. Along this trajectory the probability that a given state is filled is given by the distribution function under equilibrium $f(x, p_x, t)$. Along the trajectory the probability remains unchanged as the electron follows the path traced. This means the probability at a given position, given momentum, and given time on the trajectory should be related to the probability at an earlier point in the trajectory,

$$f(x, p_x, t) = f(x - v_x dt, p_x - F_e dt, t - dt), \text{ or } \frac{df}{dt} = 0$$

This is the collision-less Boltzmann equation. In real materials we do have collisions that create perturbations to the probability of occupation along the trajectory. We can write the above expression by expanding the derivatives,

$$\frac{df}{dt} = \frac{\partial f}{\partial t} + \frac{\partial f}{\partial x} v_x + \frac{\partial f}{\partial p_x} F_e = 0$$

These are the collision-less Boltzmann equation.
Using the known derivatives we can write the above equation in three dimensions as,
\[
\frac{\partial f}{\partial t} + \vec{v} \cdot \nabla_r f + \vec{F}_e \cdot \nabla_p f = 0
\]  
(2.13)

Here \( f(\vec{r}, \vec{p}, t) \) is the 3-dimensional distribution function and we have used the following relations
\[
\nabla_r f = \frac{\partial f}{\partial x} \hat{x} + \frac{\partial f}{\partial y} \hat{y} + \frac{\partial f}{\partial z} \hat{z}
\]
\[
\nabla_p f = \frac{\partial f}{\partial p_x} \hat{p}_x + \frac{\partial f}{\partial p_y} \hat{p}_y + \frac{\partial f}{\partial p_z} \hat{p}_z
\]

So far we have neglected the effects of scattering, electron generation-recombination processes and electron-electron correlations. Now we introduce scattering into Eq 2.13. When scattering is isotropic and/or elastic, we can use Relaxation Time Approximation, which means the scattering does not change the position, but only the momentum and probability distribution at a given point along the trajectory. The time scale at which this scattering occurs is the momentum relaxation time \( \tau_m \). Scattering processes that increase the distribution are called in-scattering and those that reduce the distribution are called out-scattering. Thus we can write,
\[
\left. \frac{df}{dt} \right|_{coll} = in\text{-scattering} - out\text{-scattering} = \dot{C} f
\]
\[
\dot{C} f = \frac{f_0(\vec{p}) - f(\vec{p})}{\tau_m} = -\frac{\delta f(\vec{p})}{\tau_m}
\]

This is true since in steady state near equilibrium,
\[
f(\vec{p}) = f_0(\vec{p}) + \delta f(\vec{p})
\]
\[
\left| f_0(\vec{p}) \right| \gg \left| \delta f(\vec{p}) \right|
\]
\[
\delta f(\vec{p}) = f(\vec{p}) - f_0(\vec{p})
\]

Thus Eq 2.13 is modified near equilibrium into
\[
\frac{\partial f}{\partial t} + \vec{v} \cdot \nabla_r f + \vec{F}_e \cdot \nabla_p f = -\frac{\delta f(\vec{p})}{\tau_m}
\]  
(2.14)

Equation 2.14 is the generalized form of the Boltzmann Equation.

We know \( \vec{F}_e = -q \vec{E} \) and near equilibrium we can write \( \nabla_r f \approx \nabla_r f_0 \) and \( \nabla_p f \approx \nabla_p f_0 \), thus we rewrite
\[
\delta f(\vec{p}) = -\tau_m \vec{v} \cdot \nabla_r f_0 + q \tau_m \vec{E} \cdot \nabla_p f_0
\]  
(2.15)

Now we can write the distribution function at equilibrium in the familiar form as
\[
f_0(\vec{p}) = \frac{1}{1 + e^{\Theta}} \quad where,
\]
\[
\Theta(\vec{r}, \vec{p}) = \left[ E(\vec{r}, \vec{p}) - F_n(\vec{r}) \right] / k_B T_L
\]
\[
= \left[ E_c(\vec{r}) + E(\vec{p}) - F_n(\vec{r}) \right] / k_B T_L
\]
where \( F_n(\vec{r}) \) is some chemical potential. By changing variables and using relations\(^\text{2.15}\) Eq 2.15 becomes

\[
\begin{align*}
\nabla_r f_0 &= \frac{\partial f_0}{\partial \Theta} \nabla_r \Theta \\
\nabla_p f_0 &= \frac{\partial f_0}{\partial \Theta} \nabla_p \Theta \\
\frac{\partial f_0}{\partial \Theta} &= k_B T_L \frac{\partial f_0}{\partial E}
\end{align*}
\]

Further simplifications are possible by explicitly writing the gradients of \( \Theta(\vec{r}, \vec{p}) \) as

\[
\begin{align*}
\nabla_r \Theta &= \frac{1}{k_B T_L} [\nabla_r E_c - \nabla_r F_n] + \left[E_c + E(\vec{p}) + F_n\right] \nabla_r \left(\frac{1}{k_B T_L}\right), \quad \text{and} \\
\nabla_p \Theta &= \frac{\vec{v}(\vec{p})}{k_B T_L} \\
\delta f &= \tau_m k_B T_L \left[ -\frac{\partial f_0}{\partial E} \right] \vec{v} \cdot \left[ \nabla_r F_n + T_L \left[E_c + E(\vec{p}) - F_n\right] \nabla_r \left(\frac{1}{T_L}\right) \right] \\
\end{align*}
\]

We immediately see that the two forces driving the current flow are the gradients in the quasi-Fermi levels \( \nabla_r F_n \) and the gradients in the (inverse) temperatures \( \nabla_r (1/T_L) \). Thus we can generalize the above equation to write the Boltzmann Transport Equation as

\[
\delta f = \tau_m k_B T_L \left[ -\frac{\partial f_0}{\partial E} \right] \vec{v} \cdot \hat{F}, \quad \text{and}
\]

\[
\hat{F} = -\nabla_r F_n + T_L \left[E_c + E(\vec{p}) - F_n\right] \nabla_r \left(\frac{1}{T_L}\right)
\]

where \( \hat{F} \) is called the \textit{generalized force}.

Since charge carriers in graphene are confined in two dimensions we can write the general form of current density in 2D graphene as

\[
\vec{J}_n(\vec{r}) = \frac{1}{A} \sum_k (-q) \vec{v} \delta f (\vec{r}, \vec{k})
\]

Here \( A \) is the cross sectional area. Using Eq\(^\text{2.17}\) in Eq\(^\text{2.18}\) we can see

\[
\vec{J}_n(\vec{r}) = \frac{-q}{A} \sum_k \tau_m(k) \left[ -\frac{\partial f_0}{\partial E} \right] (\vec{v} \vec{v}) \cdot \hat{F}
\]

Here \( \vec{v} \vec{v} \) is a tensor quantity. If we consider the generalized force to be acting in \( x \)-direction then the current density in the \( x \)-direction can be written as

\[
J_{nx} = \left(\frac{-q}{A} \sum_k \tau_m(k) \left[ -\frac{\partial f_0}{\partial E} \right] \right) \times \frac{dF_n}{dx}
\]

14
Now conductivity is related to current density such as:

\[ J_{nx} = \sigma \frac{1}{q} \frac{dF_n}{dx} \text{ thus } \]

\[ \sigma = \frac{1}{A} \sum_k q^2 v_x^2 \tau_m \left( - \frac{\partial f_0}{\partial E} \right) \]  

(2.20)

To evaluate this quantity we need to work out the sums in \( k \)-space. We note that in 2D the density of states is given by \( N_k = A/2\pi^2 \) and is independent of band structure. Also the discrete sum can be transformed into an integral using:

\[ \sum_k \rightarrow \int \frac{2\pi}{0} \frac{2\pi}{0} k dk d\theta \]

Here \( g_v \) is the valley degeneracy. With these simplifications, we can write

\[ \sigma = \frac{g_v q^2}{2\pi^2} \int_0^{2\pi} \int_0^{\infty} v_x^2 \tau_m(k) k dk d\theta \left( - \frac{\partial f_0}{\partial E} \right) \]  

(2.21)

rewriting \( v_x = v \cos \theta \) and integrating over \( d\theta \) we get

\[ \sigma = \frac{g_v q^2}{2\pi^2} \int_0^{\infty} v_x^2 \tau_m(k) k dk \left( - \frac{\partial f_0}{\partial E} \right) \]  

(2.22)

We finally have the conductivity of 2D graphene in Eq 2.22 which is independent of sample dimensions, since conductivity is a material property.

2.2.2 Ballistic Transport: Landauer Formula

In the previous section, we treated the size of the sample to be large compared to the mean free path of electron (\( \lambda_m \ll L \)). For a conductor the conductance in such situation would be given as \( G = \sigma W/L \), where \( W \) and \( L \) are the width and length of the conductor, respectively. If this ohmic scaling relation were to hold true, then as we reduce the length \( L \) then we would expect the conductance to become indefinitely large. However experimental verifications suggest that conductance reaches a limiting value \( G_0 \) when the length of conductor becomes shorter than the mean free path \( \lambda_m \gg L \). Since we know that in the ballistic regime there is no scattering, the question regarding the origin of this intrinsic conductance limit arises.

As the sample dimensions get smaller, the simple ohmic scaling relation \( G = \sigma W/L \) does not hold. There are two corrections to this law that are needed. Firstly, there is an interface resistance independent of the length \( L \) of the sample. Secondly, the conductance does not decrease linearly with width \( W \). Instead it depends on the number of transverse modes in the conductor and decreases in discrete steps. The Landauer formula incorporates both of these features.

The interface resistance arises from the fact that the conducting channel and the contacts are made of very dissimilar materials. Inside the contacts the current is carried by infinitely
Figure 2.4: (a) A schematic of a ballistic conductor sandwiched between two contacts across which an external bias is applied. (b) Dispersion relation for different transverse modes in the narrow conductor. For reflection-less contacts, the quasi-Fermi level for the \( +k \) states is \( \mu_1 \) while for the \( -k \) states is \( \mu_2 \). Adapted from [14]

many transverse modes, whereas inside the conductor only by a few modes. Any mismatch in energy causes the interface resistance. The minimum value \( G_0^{-1} \) is called the contact resistance.

Consider a piece of conductor stretched between two large contacts as shown in Fig 2.4a. As the length of the conductor is reduced, the measured conductance approaches a limiting value \( G_0 \) as the conductor becomes shorter than the mean free path \( (L \ll \lambda_m) \). At zero temperature the current flow is only in the energy range \( \mu_1 > E > \mu_2 \). Thus the applied bias can be viewed as the energy difference \( \mu_1 - \mu_2 \). We assume that the contacts are 'reflectionless', meaning that the electrons can enter them from the conductor without suffering reflections. This assumption becomes valid at energies that are not too close to the bottom of the band and electrons can exit from a narrow conductor into a wide contact with negligible probability of reflection.

Thus we have \( +k \) states (\( k \) is the wavenumber in the \( x \)-direction) in the conductor occupied by electrons originating in the left contact while \( -k \) states are occupied only by electrons originating in the right contact. This is because electrons coming from right contact populate the \( -k \) states and empty without reflections into the left contact and vise versa. Calling \( \mu_1 \) as the quasi-Fermi level for the \( +k \) states and \( \mu_2 \) as the quasi-Fermi level for the \( -k \), and by the above argument of electron filling we can say that at low temperatures the current is equal to that carried by all the \( +k \) states lying between \( \mu_1 \) and \( \mu_2 \).

The current can be calculated since states in the narrow conductor belong to different transverse modes. Each mode has an energy dispersion \( E(N, k) \) (as shown in Fig. 2.4b) with a cut-off energy \( \varepsilon_N = E(N, k = 0) \) below which it cannot propagate. The number of modes at an energy \( E \) can be found by counting the number of modes having cut-off energy
less than $E$

$$M(E) = \sum_N \vartheta(E - \varepsilon_N) \quad (2.23)$$

Let us now consider a single transverse mode whose $+k$ state is occupied according to some function $f^+(E)$. In a uniform electron gas with $n$ electrons per unit length moving with velocity $v$ the current is given by $env$. Since the electron density associated with a single $k$–state in a conductor of length $L$ is $1/L$ we can write $I^+$, the current carried by the $+k$ states, as

$$I^+ = \frac{e}{L} \sum_k v f^+(E) = \frac{e}{L} \sum_k \frac{1}{\hbar} \frac{\partial E}{\partial k} f^+(E) \quad (2.24)$$

Now assuming periodic boundary conditions and converting the sum to an integral using

$$\sum_k \rightarrow 2(\text{for spin}) \times \frac{L}{2\pi} \int dk$$

we get

$$I^+ = \frac{2e}{\hbar} \int_{-\infty}^{\infty} f^+(E) dE$$

where $\varepsilon$ is the cut-off energy of the waveguide mode. Extending the above relation to multi-mode waveguides we get

$$I^+ = \frac{2e}{\hbar} \int_{-\infty}^{\infty} f^+(E) M(E) dE \quad (2.25)$$

Assuming that the number of modes $M$ is constant in the interval $\mu_1 > E > \mu_2$ we write

$$I = \frac{2e^2}{\hbar} M \frac{(\mu_1 - \mu_2)}{e} \Rightarrow G_0 = \frac{2e^2}{\hbar} M \quad (2.26)$$

so the contact resistance is given by

$$G_0^{-1} \equiv \frac{(\mu_1 - \mu_2)/e}{I} = \frac{\hbar}{2e^2 M} \approx \frac{12.9 \text{ k}\Omega}{M}$$

Immediately we see that contact resistance goes inversely with the number of modes, and for a single-mode conductor $G_0^{-1} \sim 12.9 \text{ k}\Omega$. This is the resistance one would measure if a single-mode ballistic conductor were sandwiched between two contacts and its inverse, $G_0$, is called the Quantum of Conductance.

Although Eq. 2.26 describes the current flow in the conductor, we have assumed each transverse mode $M$ has unit probability that an electron injected in one end of the conductor will transmit to other end, but this may not always be true in general. The influx of electrons from the left contact is given by

$$I_1^+ = \frac{2e}{\hbar} M \left(\mu_1 - \mu_2\right)$$

and the outflux from the right contact is simply the influx from left contact times the transmission probability $T$

$$I_2^+ = \frac{2e}{\hbar} M T \left(\mu_1 - \mu_2\right)$$
the rest of the flux is reflected back to left contact which is reflectionless
\[ I_1^- = \frac{2e}{h} M (1 - T) \left( \mu_1 - \mu_2 \right) \]
So the net current flowing in the conductor is given by
\[ I = I_1^+ - I_1^- = I_2^+ = \frac{2e}{h} M T \left( \mu_1 - \mu_2 \right) \]
and the conductance is given by
\[ G = \frac{I}{(\mu_1 - \mu_2)/|e|} = \frac{2e^2}{h} M T \tag{2.27} \]
This is the Landauer formula for a mesoscopic conductor in the ballistic regime. We shall discuss ballistic transport properties, in the context of ultra-short channel graphene device, in the next chapter.

2.2.3 Quantum Transport: Klein Tunneling

The term Quantum Transport usually refers to the charge current in an electron gas in response to a vanishing external electric field. In this regime the quantum interference effects become important. These are mainly relevant at low temperatures where the electrons are coherent and interference effects do not get washed out by dephasing. Such effects are usually systematically studied using perturbation theory or field-theoretic techniques. If we neglect the lowest order corrections to the diffusive transport we recover the classical Einstein relation \[ \sigma_0 = \frac{e^2}{D(E_F)} \hat{D}, \]
where \( D(E_F) \) is the density of states at \( E_F \), and \( \hat{D} = v_F^2 \tau/2 \) is the diffusion constant. This represent the classical motion of electrons in a diffusive random walk scattering independently off different impurities.

In Quantum mechanics, the impurity potential is typically calculated using the Born approximation. This contributes to the electrical conductivity and is known as semi-classical transport theory. Higher order quantum corrections to the electrical conductivity is achieved with perturbation theory, such that \( \sigma = \sigma_0 + \delta \sigma \) where \( \delta \sigma \ll \sigma \). All such fluctuations/corrections to the conductivity corresponds to charge transport in the diffusive regime.

Quantum transport in mesoscopic structures in the ballistic regime has some interesting effects as well. Here we discuss a system of ballistic noninteracting electrons in graphene. In early studies on quantum-mechanical properties of the Dirac Hamiltonian, a peculiar feature of these Dirac particles was revealed, called Klein Tunneling.[17–23]

Klein Tunneling or the Klein Paradox is a counterintuitive process in which an incoming electron starts penetrating through a potential barrier if its height \( V_0 \) exceeds the electron’s rest energy, \( mc^2 \) (where \( m \) is the electron mass and \( c \) is the speed of light). In this case, the transmission probability, \( T \), depends only weakly on the barrier height, approaching perfect transparency for very high barriers, in stark contrast to the conventional,
non-relativistic tunneling where $T$ exponentially decays with increasing $V_0$. This relativistic effect can be explained with the following argument. A sufficiently strong potential, being repulsive for electrons, is attractive for positrons and results in positron states inside the barrier. These positron states align in energy with the electron continuum outside the barrier. Matching between electron and positron wave-functions across the barrier leads to the high-probability of tunnelling described by the Klein paradox even if the barrier height exceeds the rest energy of the electron. The essential feature of Quantum Electrodynamics (QED) which explains this effect is that the states at positive and negative energies are conjugated or connected. This effect has never been observed experimentally, since it requires a potential drop of $\approx mc^2$ over the Compton length $\hbar/mc$, which yields enormous electric fields ($\varepsilon > 10^{16} V cm^{-1}$) and makes the effect relevant only for such exotic situations as, for example, positron production around super-heavy nuclei with charge $Z \geq 170$. However, graphene with its unique band structure provides an effective medium where relativistic quantum tunneling described by the Klein paradox and other relevant QED phenomena can be tested experimentally.

Owing to the linear energy spectrum, it is expected that quasi-particles in graphene will behave differently from those in conventional metals and semiconductors where the energy spectrum can be approximated by a parabolic (free-electron-like) dispersion relation. Recall that charge carriers in graphene behave similar to massless Dirac Fermions\cite{12} described by a Dirac-like Hamiltonian

$$\hat{H}_0 = -i\hbar v_F \sigma \nabla$$

(2.28)

where, $v_F \approx 10^6 ms^{-1}$ is the Fermi velocity and $\sigma = (\sigma_x, \sigma_y)$ are the Pauli matrices. Although the linear energy dispersion is important, it is not the only essential feature that describes the quantum transport in graphene by the Dirac-like equation. Above zero energy, the current carrying states in graphene are usually electron-like and negatively charged. At negative energies (if the valence band is not full) its unoccupied electronic states behave as positively charged quasi-particles (holes), which are often viewed as a condensed-matter equivalent of positrons. However, electrons and holes in condensed-matter physics are normally described by separate Schrödinger equations, which are not in any way connected. Interestingly, in graphene the electron and hole states are interconnected and exhibit properties analogous to charge conjugation symmetry in QED. This symmetry in graphene arises from its crystal structure and the fact that the two sub-lattice sites (as seen in Fig 2.2) contribute to the two-component wave-function of the quasi-particle. The two-component description for graphene is very similar to the one by spinor wave-functions in QED, but the ‘spin’ index for graphene indicates sub-lattices rather than the real spin of electrons and is usually referred to as pseudospin $\xi$.

The conical spectrum of graphene comes from the intersection of conduction and valance energy bands that originate from the two sub-lattices (see Fig 2.3a). An electron with energy $E$ propagating in the positive direction originates from the same branch of the electronic spectrum (shown in red in Fig 2.5a) as the hole with energy $-E$ propagating in the opposite direction. This means that electrons and holes belonging to the same branch have
Figure 2.5 (a) Schematic of the spectrum of quasi-particles in single-layer graphene at low Fermi energies ($< 1eV$). The Fermi level (dotted lines) lies in the conduction band outside the barrier and the valence band inside it. The blue filled areas indicate occupied states. The pseudospin $\xi$ is parallel (anti-parallel) to the direction of motion of electrons (holes). (b) Schematic of potential barrier of height $V_0$ and width $D$, and definition of angles $\theta$ and $\phi$ used in text. Adapted from [15, 16]

Let us now formulate Klein Tunneling in Single-layer graphene. Consider a rectangular potential barrier that is infinite along the $y$–direction given by

$$V(x) = \begin{cases} V_0 & 0 < x < D, \\ 0 & \text{otherwise}. \end{cases} \quad (2.29)$$

We assume the propagating electron wave is incident at an angle $\phi$ with respect to the $x$–axis. We try the Dirac spinor $\psi_1$ and $\psi_2$ for the Hamiltonian $H = H_0 + V(x)$ in the
following form.

\[
\psi_1(x, y) = \begin{cases} 
(e^{ik_x x} + re^{-i k_x x})e^{ik_y y} & x < 0, \\
(\alpha e^{iq_x x} + be^{-iq_x x})e^{ik_y y} & 0 < x < D, \\
t e^{ik_x x + ik_y y} & x > D,
\end{cases}
\]

\[
\psi_2(x, y) = \begin{cases} 
(s(e^{ik_x x + i\phi} + re^{-i k_x x - i\phi})e^{ik_y y} & x < 0, \\
s'(\alpha e^{iq_x x + i\theta} + be^{-iq_x x - i\theta})e^{ik_y y} & 0 < x < D, \\
s't e^{ik_x x + ik_y y + i\phi} & x > D,
\end{cases}
\tag{2.30}
\]

Here \( k_F = 2\pi/\lambda \) is the Fermi wave vector, \( k_x = k_F \cos \phi \) and \( k_y = k_F \sin \phi \) are wave vector components outside the barrier, \( q_x = \sqrt{(E - V_0)^2/\hbar^2 v_F^2 - k_y^2} \), \( \phi = \tan^{-1}(k_y/q_x) \) is the refraction angle, \( s = \text{sign}(E) \) and \( s' = \text{sign}(E - V_0) \). Applying boundary conditions and matching the coefficients at the boundaries yields the reflection coefficient to be,

\[
r = \frac{(2i e^{i\phi} \sin(q_s D)) \times (\sin \phi - s s' \sin \theta)}{s s' \left[ e^{-i q_s D} \cos(\phi + \theta) + e^{i q_s D} \cos(\phi - \theta) \right] - 2i \sin(q_s D)}
\tag{2.31}
\]

The transmission probability \( T = |t|^2 = 1 - |r|^2 \) can be calculated using the above Eq. \[2.31\] and in the limit of high barriers \( |V_0| \gg |E| \), we can simplify and write

\[
T = \frac{\cos^2 \phi}{1 - \cos^2(q_s D) \sin^2 \phi}
\tag{2.32}
\]

Under resonance conditions i.e, \( q_x D = \pi N, \ N = 0, \pm 1, \ldots \) the equations \[2.31\] and \[2.32\] indicate that the barrier becomes transparent \( (T = 1) \). Furthermore, the barrier always remains perfectly transparent for angles close to normal incidence \( \phi = 0 \). This perfect tunneling can be understood in terms of conservation of pseudospin. An electron moving to the right can be scattered only to a right-moving electron state or left-moving hole state. In Fig. \[2.5a\] charges from the ‘red’ branch of the band can be scattered to the same ‘red’ branch and not into the ‘green’ branch. This matching of pseudospin \( \xi \) for quasi-particles inside and outside the barrier is what causes perfect tunneling.

It is experimentally feasible to create such barriers in graphene, in order to verify Klein Tunneling. Experiments involving the electric field effect using either a thin insulator or local chemical doping have shown evidence of Klein tunneling in graphene sheets. Moreover Dirac fermions in graphene are massless and, therefore, there is no formal theoretical requirement for the minimal electric field to form positron-like states under the barrier. Fields routinely used in experiments \( (\varepsilon \approx 10^5 \ V/cm^{-1}) \) have been found sufficient to create a well-defined barrier in realistic graphene samples with disorder. Such fields are eleven orders of magnitude lower than the fields necessary for the observation of the Klein tunneling for elementary particles. Thus graphene provides a bench-top experimental verification of an analogous relativistic phenomenon. In the next section we discuss the various ways graphene can be locally doped to form potential barriers that are both practically useful as well as provide further insight to quantum transport in graphene.
2.3 Tuning the Electronic Structure Of Graphene

In conventional semiconductors like silicon or germanium, the electronic properties are controlled by doping the intrinsic material. Usually trivalent (Atoms with three valence electrons like boron, aluminum, gallium) or pentavalent (Atoms with five valence electrons like phosphorous, arsenic, antimony) impurity atoms of known concentrations are mixed with pure intrinsic silicon or germanium to achieve $p$–type or $n$–type doping respectively. This allows control of the location of the Fermi level in the material by choosing the type of impurity and its concentration. By fusing two materials with opposite doping we create a $p – n$ junction, which has been the hallmark of the present day electronic industry.

After graphene was first successfully isolated and observed to possess high charge carrier mobility and electric field effect, tuning its electronic properties by doping it or modifying its structure has been extensively studied. However, the methods used to dope graphene are different from the conventional methods used in semiconductor process technology. Electronic structure modification in graphene could be broadly classified into three main categories.

- **Chemical Doping**: Chemical species interact with the graphene surface either by chemical modification or surface adsorption.

- **Structural Modifications**: Confining charge carriers by making graphene nanoribbons and controlling its edge chirality or mechanically straining the lattice.

- **Electrostatic Doping**: An external gate voltage controls the electric field applied to graphene and thus the majority charge carriers.

Here is a brief overview of these methods.

**Surface Adsorption Doping**

Graphene has the highest possible surface to volume ratio, and this allows the charge carriers in graphene to readily respond to their environment. Initially it was shown that water vapor and ammonia dope graphene to be $p$–type and $n$–type respectively. Soon after there has been a race to achieve doping that is both spatially controllable and one that does not compromise the basic nature of graphene which is its high charge carrier mobility. The 2D structure of graphene, although very useful in creating surface adsorption of different chemical species, also causes the charge carriers to scatter due to the presence of such adsorbents, thus undesirably reducing the high carrier mobilities. Moreover, graphene devices fabricated on substrates, (as opposed to free-standing device) without any further chemical treatments, show a built in $p$–type doping. An alternative to using organic or inorganic chemical compounds to dope graphene, is to use adsorbed metals. Since there is a mismatch in work function, different metals tend to dope graphene differently. The effective doping scheme being sought after has to increase one type of charge carrier in the plane of graphene and also not hinder its motion across the 2D lattice.
Doping by Chemical Modification
Since adding chemical species on top of graphene in the interest of doping it has proven to be challenging, doping by modifying its chemical structure has also been investigated. Chemical species have been used to substitute carbon atoms in graphene with other atoms such as boron and nitrogen.\textsuperscript{[44–50]} When compared to carbon, nitrogen has one additional electron and boron lacks one. When nitrogen atoms are incorporated into the basal plane of graphene, they donate electrons to graphene leading to \(n\)-type doping of graphene, and graphene doped with boron would exhibit \(p\)-type behavior. Recently, large-area atomic thickness films of \(h-BNC\) consisting of hybridized hexagonal-boron nitride \((h-BN)\) and C (graphene) domains have been prepared by a CVD method using methane and ammonia borane \((NH_3 - BH_3)\) as precursors. Pure \(h-BN\) and pure graphene domains randomly distribute in \(h-BNC\) and their compositions can be tuned by changing the ratio of the gas concentration, therefore, \(h-BNC\) with different band gaps are obtained.\textsuperscript{[48]}

Structural Modifications: Band Gap Engineering
Since graphene can be considered a zero-band-gap semiconductor, it is highly desirable to induce a band gap in graphene for practical device applications. Several methods have been explored to open a band gap in graphene such as, substrate-induced band gaps,\textsuperscript{[51–54]} straining bi-layer graphene,\textsuperscript{[55–57]} confinement of graphene edges by fabricating graphene quantum dots and nanoribbons.\textsuperscript{[58–65]} Another method to induce a band gap is by adsorption of atomic hydrogen on graphene. Graphene reacts with hydrogen, forming \(C-H\) bonds, thereby changing the \(sp^2\)-bonded carbon into \(sp^3\)-bonded carbon. This causes the conducting \(\pi\)-bands to be eliminated resulting in opening of a band-gap.\textsuperscript{[66–69]}

Electrostatic Doping
In pristine graphene the Fermi level is exactly at the Dirac point and can be easily tuned to be either in the conduction band or the valance band by applying an external electric field. This tunability allows a simple way of choosing either electrons or holes as the charge carriers. Furthermore, using external electric fields does not have the undesirable effect of inducing defects or disorder in graphene, thus it does not affect the high carrier mobility. Moreover, applying the FET principle in graphene to achieve doping is practically useful, and attracts large research interest. In the previous section we discussed Klein tunneling, the experimental verification of which is carried out using local electrostatic doping of graphene. Figure 2.6a shows a schematic of an experimental setup used to construct such doping in a graphene device. An external voltage can be applied on both top and bottom gate electrode, inducing an electric field effect in graphene. When both electrodes induce opposite fields, a potential barrier similar to the one discussed in Fig. 2.5 can be observed.\textsuperscript{[24–26]} By utilizing different gate configurations and gate dielectric materials, other effects such as resonant tunneling, \(p-n\) junctions, superlattice structures consisting of multiple \(p-n\) junctions, etc., have been studied.\textsuperscript{[55, 70–81]}

23
Figure 2.6 (a) A schematic of doping using both bottom and top gate geometry. A positive voltage on the bottom gate electrode forces the graphene to be $n$-doped, while applying a negative voltage on the top gate electrode induces $p$-type doping in the graphene channel, in vicinity of the top electrode. (b) Schematic band diagram representation of doping in graphene. The Fermi-level remains flat throughout the graphene channel, but the doping is governed by the location of this level with respect to the Dirac point.

2.4 Scope Of Present Work

Three important aspects of graphene devices are studied in this present work, which are

1 *Short Channel Effects in Graphene*: Scaling effects in contemporary semiconducting devices have been well understood. As new channel materials like graphene are of interest, scaling of such devices and studying their electronic properties at short length scales become important. In this work, we fabricate an ultra-short channel graphene field effect device and study its electrical transport behavior. An analytical model is also developed to explain the observed non-linear current-voltage characteristics.

2 *Electrical Breakdown of Graphene*: In addition to being used in active circuit elements (like FETs), graphene has shown potential use in the role of interconnects, providing a fast connection and carrying large amounts of current. Understanding the limits of such interconnects and their behavior close to breakdown is pertinent in such applications. Here we study breakdown effects of few-layer graphene devices at high current densities.

3 *Doping and Environmental Effects in Graphene*: Tuning electrical properties of graphene by doping it is a key area that has generated a lot of interest in the scientific community. We here study the doping effect of the environment and polymer encapsulation on graphene devices. Using polymer capping we observe an overall shift from $p$-type to $n$-type doping upon annealing. In addition, upon introducing solvent into the polymer capped device, we observe huge hysteresis in conduction. This provides a dual route to dope graphene where chemical adsorption and electrostatic gating techniques are combined.

Copyright © Abhishek Sundararajan, 2015.
Chapter 3 Ultra-Short Channel Graphene Field Effect Device

3.1 Introduction

Graphene has attracted the attention of the electronics device community, and major integrated chip manufacturers are now active in graphene research. Furthermore, the International Technology Roadmap for Semiconductors, the strategic planning document for semiconductor industry, is considering graphene to be among the candidate materials for post-silicon electronics.[82] Graphene Field effect Transistors (GFET) have also created interest since they can be used for high frequency applications.[83–85] Although long-channel GFET device characteristics have been studied thoroughly,[86–93] short channel effects at lengths shorter than a few tens of nanometers have not yet been addressed. In this study we report fabrication and electrical characteristics of ultra-short channel length GFETs at sub–20 nm length scale.

Electron beam lithography is a conventional method used in manufacturing devices that are a few tens of nanometer in size scale. This technique, however, has some limitations when it comes to the resolution of the smallest feature that can be produced. Small feature sizes on the order of sub–20 nm sizes require the use of high electron incident energies (dose), aberration corrected STEM with patterning capabilities, and use of a special type of polymer resist.[94–96] The use of high electron doses ($\sim 10^3 \mu\text{C/cm}^2$) to produce nested features (as opposed to isolated features) leads to electron scattering in resist and substrate which in turn leads to an undesired influence in the regions adjacent to those exposed by the electron beam. This effect is called the Proximity effect. Thus when fabricating a short channel GFET, such considerations need to be included, since it has been observed earlier that high electron doses and polymer resist residues on graphene tend to modify its physical properties, which is undesirable.[97–101]

We overcome these drawbacks by utilizing an alternative route for achieving sub–20 nm channel length GFETs. We use a feedback controlled electromigration technique[102] to form nanogaps on top of graphene. After fabricating the device, electrical characterization reveals non-linear behavior of current with respect to applied bias voltage. We also observe a quasi-saturation effect of the current with applied bias and gate voltages. An analytical model using ballistic transport is developed to explain the observed effect. In addition, at high gate voltages, as the bias voltage is increased, we observe a resistive switching effect. This switching effect is observed to be stable and affects the low bias transconductance curve of the device. We start our discussions with experimental details.
3.2 Experimental Setup

3.2.1 Sample Preparation

The graphene test devices used in these experiments are isolated on highly $p$-doped silicon substrates with 300 nm of thermally grown $SiO_2$. To eliminate any environmental doping effects when preparing the graphene samples, the substrates are prepared in a glove bag and graphene exfoliated in a dry $N_2$ environment. Graphene flakes are then optically identified and the thickness is confirmed by Raman microscopy using a 633 nm wavelength incident laser. Electron beam lithography is used to create a bow-tie like geometry on top of graphene as seen in Fig.3.1b. Metal electrodes are fabricated by depositing gold of 30 nm thickness using electron beam evaporator. The individual contacts to graphene are not defined, since the electrodes on either side are connected by a small constriction. The constriction in the form of a bow-tie is placed on graphene so that, the nanogap formed at a later stage is on top of graphene. The excess graphene not covered by gold electrodes is then etched using oxygen plasma in a reactive-ion etching (Oxford instruments Plasmalab80plus) using the metal electrodes themselves as an etch mask (See schematic Fig.3.1d). The electromigration process is carried out under a vacuum of $1 \times 10^{-5}$ Torr or lower at room temperatures, and the electrical characterization is carried out at liquid nitrogen temperatures of 77 K using a Lakeshore cryogenic probe station.

3.2.2 Ultra-Short Channel Fabrication

As bias voltage ($V_{SD}$) is applied across the small constriction bridging the electrodes, current flows preferably through the gold constriction, since this path will be of least resistance. An initial gate voltage ($V_G$) sweep at low $V_{SD}$ shows no $V_G$ dependence of resistance across the constriction, as expected. The gold in the constriction is now controllably electromigrated by ramping $V_{SD}$ across the electrodes while monitoring the current. During the first electromigration cycle, the resistance of the device is controllably increased to $\sim 30 \Omega$ higher than its initial resistance. This procedure ensures the slow thinning of metal over graphene and also prevents abrupt breaking of the metal constriction at high bias voltages, which might cause a sudden increase in current flow through the graphene channel. This is undesirable as it can damage the underlying graphene. Gate sweeps at low $V_{SD}$ are taken in between each electromigration cycle to confirm the presence of the graphene channel. After a couple of cycles, the resistance of the device starts to show some dependence on $V_G$. This is due to the resistance in the metal constriction being similar to that of the underlying graphene channel (as a parallel resistor) as seen in Fig.3.2c. Further $V_{SD}$ ramps result in the formation of a nanogap, exposing an ultra-short graphene channel (See schematic in Fig. 3.2d). Once the nanogap is formed, further $V_{SD}$ biasing does not result in more electromigration (orange curve in Fig 3.2b), suggesting the nanogap is stable. Gate sweeps taken after the final electromigration step confirm the presence of the graphene channel, and the opening of a nanogap in the electrodes (Fig 3.2c).
Figure 3.1: (a) Optical image showing a sheet of single and bilayer graphene before de-
position of metal electrodes. (b) Optical image showing three devices constructed on the
same bilayer graphene and one constructed on a single layer graphene sheet as shown in
(a). (c) A schematic side view of electrodes deposited on graphene sheet as shown in (b).
The small constriction in the center connects the electrodes on either side. (d) Schematic
top-view showing constriction in metal contacts patterned on top of graphene.

Scanning electron microscope images of the nanogap formed over graphene are shown in Fig. 3.3a and 3.3b. The images were taken after all the electrical tests on the device were completed to avoid any contamination caused by electron beam. This definitively confirms that the graphene sheet is intact and the nanogap is stable.

3.2.3 Electrical Characterization

Since the electromigration process is carried out under vacuum inside a cryogenic probe station at room temperature, the devices thus formed need not be exposed to ambient at-
mosphere, thereby avoiding any contaminations. As the device remains under vacuum, the sample stage is cooled down using liquid nitrogen to temperatures of 77 K and electrical characterization tests are carried out thereafter.

The current-voltage (I-V) characteristics of the device is carried out by slowly sweeping $V_{SD}$ starting from $-400 \, mV$ to $+400 \, mV$ and back, at $1 \, mV$ steps at a constant known gate
Figure 3.2: (a) A plot of current versus bias voltage $V_{SD}$ showing all cycles of metal electromigration (EM) carried out. (b) Zoomed in section of the plot of current versus bias voltage $V_{SD}$ as shown in (a). After initial EM cycle, the bias voltage need not be ramped to as high voltages to result in further increase in resistance. During EM cycle-4 the metal constriction breaks resulting in the nanogap formation. The plot also shows $V_{SD}$ ramped after nanogap formation, which does not result in further EM of metal indicating that the nanogap is stable. (c) A plot of resistance versus gate voltage $V_G$ showing data taken in between each EM cycle. After the EM cycle-4 a nanogap is formed and a transfer curve corresponding to graphene channel is obtained. (d) Ultra-short channel being defined by creating a nanogap over graphene using electromigration of metal. The nanogap defines the ultra-short graphene channel length scale.

Voltage $V_G \neq 0$. The $V_{SD}$ is stalled for 50 ms after stepping by 1 mV, so that the current in the device can equilibrate. The current is then recorded by a high precision ammeter. After each $V_{SD}$ sweep the gate voltage is stepped through desired value in the range of ±60 V. Low bias ($V_{SD} = 20 \text{ mV}$) gate sweeps are performed before and after each I-V characterization test to make sure the graphene under the nanogap is preserved. Both single-layer and bi-layer graphene devices are fabricated and tested.
3.3 Results

3.3.1 Single Layer Graphene Device: I-V Characteristics

In a conventional long channel MOSFET, at a given gate voltage and source-drain bias voltage such that $V_{SD} < V_G$, the current in the device varies linearly with applied $V_{SD}$. Here the device is said to be operating in the linear or the ohmic region. As the $V_{SD}$ is increased further, the current deviates from the linear region and tends to saturate. This region is called the saturation region.

In comparison, our single layer short channel GFET shows a transition between linear and non-linear current behavior with respect to the applied $V_{SD}$. Although the current does not completely saturate, we observe a so-called quasi-saturation in current. Here the I-V characteristics do not saturate with increasing $V_{SD}$, but rather show an inflection point where the slope of the I-V curve ($dI/dV_{SD}$) has a minimum. We term this behavior as quasi-saturation of current with respect to applied bias. Figures 3.4a and 3.4b show I-V characteristics of a device at various gate voltages taken at 77 K. The slope of the curve changes at the inflection point and gradually settles to a value as the applied bias is increased further. At low positive gate voltages, we see quasi-saturation of current around $V_{SD} \sim 150 \, mV$. This non-linear behavior weakens for higher positive gate voltages $V_G \geq 20 \, V$ within the same bias voltage range. In contrast, at negative gate values the non-linearity becomes enhanced as the gate voltage is increased (Fig. 3.4b) and quasi-saturation in current occurs at higher bias voltages $V_{SD} \sim 200 \, mV$. The quasi-saturation in current is observed to be symmetric with respect to the $V_{SD}$ sweep at any given $V_G$ (as seen in Fig. 3.4c). Conduction of
Figure 3.4  (a) A plot of current versus bias voltage $V_{SD}$, corresponding to a single layer graphene device, showing non-linear behavior of current at various positive gate voltages.  
(b) A plot of current versus bias voltage $V_{SD}$ for the same device, showing non-linear behavior of current at various negative gate voltages. Data sets shown in both (a) and (b) belong to the same I-V characterization test carried out at 77 K.  (c) Plot of current versus bias voltage $V_{SD}$ showing symmetric behavior of current with respect to $V_{SD}$.  (d) Plot of conductance versus gate voltage $V_G$ sweep showing asymmetric behavior with gate voltage.

the device is observed to have an asymmetric response with respect to the $V_G$ sweep. Figure 3.4d shows conduction suppression at positive gate voltages and enhancement at negative gate voltage values. This indicates $p$--type carriers are more preferred in the device. The gate sweep data is taken before and after the I-V characterization tests, and no noticeable change is observed. Very little hysteresis is seen, indicating that the graphene sheet is pristine without any contaminations or adsorbents. The charge neutrality point of this sample is at $V_{CNP} \approx -1.5$ V. We see asymmetric gate response, with higher conductivity for negative gate voltages. This indicates $p$--type doping of the contacts.[105]
Differential conductance \( \frac{dI}{dV_{SD}} \) is studied in devices that show a non-monotonic (non-ohmic) I-V characteristics. Such devices can amplify a signal applied to them, and are used to make amplifiers and oscillators. Since our device exhibits similar non-ohmic behavior, we study its I-V characterization data, and calculate \( \frac{dI}{dV_{SD}} \) by taking the slope of the curve. Figure 3.5a is a contour plot of differential conduction with respect to gate and bias voltage for the same I-V data shown in Fig. 3.4. The differential conduction has a local minimum around \( V_{SD} \approx \pm 0.1 \text{ V} \) that is much more pronounced for positive gate voltages than for negative gate voltages. Figure 3.5b shows \( \frac{dI}{dV_{SD}} \) versus bias voltage \( V_{SD} \) at various gate voltages. For bias voltages greater than \( V_{SD} > \pm 0.2 \text{ V} \) the gate voltage has minimal effect on the differential conductance. This means, at these bias voltages, with further increase in \( V_G \), very few additional charges can be induced in the channel. In a conventional MOSFET, this behavior is enhanced and is termed the Saturation Region, and the MOSFET is considered to be in the active or ON state.

Another important observation that is to be made here is regarding a peak in differential conductance near low (around zero) bias voltage. This effect is usually termed Zero Bias Conductance Peak and is very important in understanding the transport behavior of charge carriers in a given material. This effect is observed (more generally occurs in junctions between normal metal and conventional superconductor) in systems where graphene-superconductor boundaries induces a phase-coherent transport of charge carriers, or enhanced reflectionless tunneling between superconductor and normal metal.\[106, 107\]

In our device, the zero bias conductance peak is controlled by the external gate voltage \( V_G \). We observe the peak to be symmetric about the applied \( V_{SD} \) voltage, but asymmetric about different applied \( V_G \). Figure 3.5b shows the zero bias conductance peak at various gate voltages, and clearly we observe a higher peak conductance value at high negative gate voltages. Furthermore, this peak in conductance vanishes around \( V_G \approx 0 \approx V_{CNP} \). It should
be noted that in our devices, graphene is in contact with gold (non-superconductor) metal alone and all I-V characteristics are performed at no externally applied magnetic field.

### 3.3.2 Bilayer Graphene Device: I-V Characteristics

It is instructive to compare the I-V characteristics of single layer and bilayer graphene devices. Moreover, bilayer graphene has a slightly different band structure. The linear energy dispersion relation in the single layer is replaced by a slightly parabolic one for the bilayer graphene. This definitely affects the charge transport behavior in bilayer graphene.\[108–110\]

After electromigration of the metal contacts on top of a bilayer graphene sheet, the device is electrically tested under the same conditions as the single layer device discussed earlier. Our results show non-linear behavior of current with respect to applied bias voltage $V_{SD}$ at various gate voltages. When compared to the results obtained for a single layer graphene device, shown in Figs. 3.4 and 3.5, the bilayer graphene device show many notable differences which we qualitatively discuss here.

- In the single layer graphene device we observe a quasi-saturation of current, in contrast to the bilayer device where no quasi-saturation of current is observed within the given range of applied bias ($V_{SD} = \pm 400 \text{ mV}$) voltages.

- The I-V curve for the bilayer device is asymmetric in both $V_{SD}$ and $V_G$, although it is more asymmetric in $V_G$ than in $V_{SD}$.

- The I-V curve for positive gate voltages shows minimal current enhancement due to applied gate, whereas at negative gate voltage values, current is seen to be controlled by the applied gate.

- Differential conductance plots at positive and negative gate voltages show no zero bias conductance peak. Furthermore, the differential conductance seem to be varying a little with applied positive gate when compared to negative gate voltages. This indicates $p-$type carriers are preferred in bilayer graphene device.
3.3.3 Resistive Switching

In our single layer graphene device, as we ramp the bias voltage at a fixed gate voltage, we observe a current saturation followed by a region where the device shows a negative differential conduction (NDC), where the current decreases as $V_{SD}$ is increased. Current saturation occurs around $V_{SD} \approx 0.6$ V on the positive voltage sweep (from zero towards high positive volts at 1 mV steps). At this point an increase in $V_{SD}$ does not result in an increase in current. Beyond this voltage the device moves into an NDC regime, where an increase in $V_{SD}$ results in a decrease in current. As the bias voltage is further increased, the device begins to show increasing current with increasing voltage and reverts back to the usual ohmic behavior. This effect can possibly be attributed to hot carrier injection into the oxide substrate.[111, 112] Upon ramping down the bias voltage, we observe a large hysteresis in the current. This whole cycle of ramping the $V_{SD}$ to a high value and back to zero corresponds to performing a write, and the observed hysteresis affects the transconductance behavior of the device. A subsequent gate sweep at small bias voltage (transconductance plot) reveals a large shift in the charge neutrality point (CNP). By performing a write at different gate voltages, we are able to shift the CNP to various positions. A read can be performed by measuring the device resistance at low bias voltage (in this case $V_{SD} = 20$ mV) at $V_G = -60$ V. Writing at three different gate voltages results in three distinct resistances when the device is measured at $V_G = -60$ V. This indicates that these devices are possible candidates for multi-bit storage.

3.4 Device Modeling

There are several models that have been studied which, when calibrated, can accurately describe the I-V characteristics of graphene devices.[90, 113, 114] Such models are based on drift-diffusion equations, describing the device under the diffusive limit. They provide a good understanding of device characteristics at relatively long channel lengths, where scattering is significant. The scattering of charge carriers causes velocity saturation of the charge carriers, and in turn causes the current in the device to saturate.[88, 89, 92, 115]

In the case of extremely scaled GFETs, simulations have been performed using more sophisticated models. Graphene exhibits high charge carrier mobility which additionally reduce the scattering rate, and thus justifies the use of ballistic transport.[116] In such models, quantum transport within the non-equilibrium Green’s function (NEGF) formalism, using either the tight-binding or a Dirac Hamiltonian, is combined with a self-consistent electrostatics.[105, 117, 118] Although these models are more suitable for simulating the ballistic limit electron transport of the device and can include Klein tunneling, they are computationally demanding and not suitable for device optimization studies.

In the past, only few models for short channel GFETs utilizing semi-analytical ballistic transport have been proposed.[119–121] In graphene, due to ambipolar nature of charge transport, two regimes are observed: a quasi-saturation regime and the negative differential conductance (NDC) regime. Both phenomenon have been experimentally observed in long channel graphene devices.[86, 122] We observe both these effects in our ultra short channel
graphene device as well. Moreover, most of the models proposed so far address the device characteristics either in the quasi-saturation regime or the NDC regime. Furthermore, the models proposed so far do not show symmetric current with respect to the applied $\pm V_{SD}$. Here, we develop a semi-analytical model based on ballistic charge transport, to describe our single layer graphene device behavior in quasi-saturation regime (in low applied $V_{SD}$).

### 3.4.1 Model

In our model for GFET, the source and drain regions are assumed to be made of graphene layer with a metal film deposited on top. Within the semi-analytical model, we assume a simple square potential barrier, where $E_{dS}$, $E_{dG}$, and $E_{dD}$ are the energy of the Dirac point in the source, graphene channel and drain regions respectively. The metal contacts to graphene induce doping and thus control the $E_{dS}$ and $E_{dD}$ of the source and drain electrodes. This is a good assumption since the deposited metal have different work functions when compared to graphene and have shown to dope the underlying graphene. [38, 120]

This metal induced doping of graphene is incorporated in our model through a fixed energy difference $\Delta E_{con}$ between the Fermi level and the Dirac point of the source and drain electrodes. Thus $\Delta E_{con} = \mu_S - E_{dS}$ or $\Delta E_{con} = \mu_D - E_{dD}$.

Recalling the expression for current in ballistic transport, given by Eq.2.25 and rewriting it under zero temperature approximation we get

$$I = \frac{2q}{h} \int_{\mu_S}^{\mu_D} M(E) dE$$

(3.1)

where $h$ is Planck’s constant, and $M(E)$ represents number of propagating modes in graphene channel at energy $E$. The integral is calculated in the energy window for transport, and is the one between the Fermi levels $\mu_S$ and $\mu_D$ of the source and drain regions, respectively. In order to compute the integral we need to write the electron and hole concentrations in the channel region, and is given by

$$n = \int_{E_{dG}}^{\infty} dE \left[ D_L(E) f_S(E) + D_R(E) f_D(E) \right]$$

$$p = \int_{-\infty}^{E_{dG}} dE \left[ D_L(E)(1 - f_S(E)) + D_R(E)(1 - f_D(E)) \right]$$

(3.2)

Here $f_{S/D}(E)$ is the contact Fermi distribution in source/drain electrode with Fermi level $\mu_{S/D}$, and $D_{L/R}(E)$ is the density of states (DOS) in the channel at energy $E$ relative to injection from source and drain (for the left moving and right moving charges). Further simplifications to Eq. 3.2 are made by assuming that the DOS in the channel to be symmetric for both left and right moving charges, and neglecting the effects of Fermi distribution (since zero temperature is assumed earlier). Furthermore, not all energies in the channel contribute to the conduction, only the energies in the range $\mu_S$ and $\mu_D$ participate.
in conduction. Thus we can write the carrier densities in the channel as

\[ n = \int_{E_{dG}}^{\mu_D} dE[D(E)] \]  \hspace{1cm} (3.3)

\[ p = \int_{\mu_S}^{E_{dG}} dE[D(E)] \]

Here the DOS is given by

\[ D(E) = \frac{1}{\pi(h\vartheta_f)^2} |E - E_{dG}| \] \hspace{1cm} (3.4)

where, \( \vartheta_f \) is the graphene Fermi velocity.

The Dirac point in the channel, \( E_{dG} \), is self-consistently computed with \( n \) and \( p \) through plane capacitor model given by

\[ q(n - p) = C_{ox}\left(\frac{-\mu_S}{q} + V_G + \frac{E_{dG}}{q}\right) \] \hspace{1cm} (3.5)

where \( C_{ox} \) is the gate oxide capacitance, and a zero work function difference between gate and graphene is assumed.

By choosing \( \mu_S = 0 \) as a reference point, and using Eqs. (3.3), (3.4), and (3.5) we compute the Dirac point in the channel, \( E_{dG} \), piecewise in six different regimes as shown below. These six regimes encompass the device characteristics in all possible biasing configurations.

\[ E_{dG} = \frac{1}{2} \left[ - (b - \mu_D) + \sqrt{(b - \mu_D)^2 - 2(aV_G + \mu_D^2)} \right] \] \hspace{1cm} \text{for } E_{dG} > \mu_D > \mu_S \hspace{1cm} (3.6)

\[ E_{dG} = \frac{1}{2} \left[ - (b - \mu_D) + \sqrt{(b - \mu_D)^2 - 2(aV_G + \mu_D^2)} \right] \] \hspace{1cm} \text{for } E_{dG} > \mu_S > \mu_D \hspace{1cm} (3.6)

\[ E_{dG} = \frac{1}{2} \left[ (b + \mu_D) - \sqrt{(b + \mu_D)^2 - 2(\mu_D^2 - aV_G)} \right] \] \hspace{1cm} \text{for } \mu_S > \mu_D > E_{dG} \hspace{1cm} (3.6)

\[ E_{dG} = \frac{1}{2} \left[ (b + \mu_D) - \sqrt{(b + \mu_D)^2 - 2(\mu_D^2 - aV_G)} \right] \] \hspace{1cm} \text{for } \mu_D > \mu_S > E_{dG} \hspace{1cm} (3.6)

\[ E_{dG} = \frac{\mu_D^2 - aV_G}{2(b + \mu_D)} \] \hspace{1cm} \text{for } \mu_D > E_{dG} > \mu_S \hspace{1cm} (3.6)

\[ E_{dG} = \frac{\mu_D^2 + aV_G}{2(\mu_D - b)} \] \hspace{1cm} \text{for } \mu_S > E_{dG} > \mu_D \hspace{1cm} (3.6)
Here we have used the notations

\[ a = \frac{2\alpha C_{ox}}{q}, \quad b = \frac{\alpha C_{ox}}{q^2}, \quad \text{and} \quad \alpha = \pi (\hbar \theta_f)^2 \]

Now the number of modes that participate in conduction is given by

\[ M(E) = \min [M_S(E), M_D(E), M_G(E)] \quad (3.7) \]

where

\[ M_{S/D/G}(E) = \frac{2W}{\pi \hbar \theta_f} |E - E_{d,S/D/G}| \]

and \( W \) is the width of the channel.

We use a numerical code, developed using Mathematica, to calculate the minimum value of the above relation at each energy level and integrate using Eq. (3.1) to get the current in the device as a function of the drain bias. We consider \( p \)-type doped source and drain electrode regions, and assume the value \( \Delta E_{con} = 0.3 \ eV \).

So far we have assumed that the source and drain regions are described by the same linear dispersion relation as the channel. This is not true in real experimental situations, since the DOS in the contacted region is broadened due to metal-graphene coupling.[105] This broadening induces a finite DOS at the Dirac point. Therefore, we introduce DOS broadening of contacts (\( \Delta = 162 \ meV \)) in our model in order to better fit the model to our experimentally obtained I-V characteristics. Finally, we add a resistance of \( R_c = 200 \ \Omega \) in series to the simulated device in order to account for the contact resistance of the device. Further increase in \( V_{SD} \) leads to rise in current and the disappearance of the quasi-saturation effect.
3.4.2 Results

Figure 3.6: (a) Experimental I-V data for the single layer graphene device at various negative gate voltages. (b) Simulated I-V data for the same range of $V_{SD}$ and gate voltages as in (a). (c) Experimental I-V data for the single layer graphene device at various positive gate voltages. (d) Simulated I-V data for the same range of $V_{SD}$ and gate voltages as in (c).

Using the numerical code, we obtain the I-V characteristics for a simulated device in the same range of $V_{SD}$ and gate voltages as the experiment. We observe a quasi-saturation of current as shown in Figs. 3.6b and 3.6d. This quasi-saturation occurs when $\mu_D$, controlled by $V_{SD}$, crosses the Dirac point of the channel, $E_{dG}$, for $V_G < 0$, and when $\mu_S$ crosses $E_{dG}$ for $V_G > 0$. At the Dirac point, the DOS in the graphene channel is at a minimum, resulting in a bottleneck in the number of available modes for conduction. This causes a minimum in the differential conductance.
3.5 Conclusions

We have demonstrated a novel method of fabricating stable ultra-short channel graphene field effect device. Electromigration of the metal contacts is used to achieve the channel length control. The devices thus fabricated are electrically tested and the I-V characteristics studied. Both single layer and bilayer graphene device show a non-linear current behavior with the applied bias voltages. The single layer graphene device shows quasi-saturation in current as well.

A semi-analytical model, within the ballistic charge transport regime, is developed to explain the observed behavior of the single layer graphene device. This model addresses the device’s I-V characteristics in the low bias ($V_{SD}$) region.

During high $V_{SD}$ stressing cycles, and with constant $V_G$, a negative differential conductance effect is observed for our single layer device. A hysteresis in the current is also observed after such stressing cycles which affect the low bias gate sweep (transconductance data) of the device. A controllable and reversible resistance value of the device at low $V_{SD}$, and $V_G = -60$ V is achieved by electrically stressing the device. Thus the device shows potential use in multi-bit storage applications.
Chapter 4 Electrical Breakdown of Graphene

4.1 Introduction

Graphene is a fascinating two-dimensional material that has shown immense potential for future nanoelectronic devices. Its high charge carrier mobility\(^{[123]}\) and superior heat conduction\(^{[124]}\) has potential use in constructing high speed interconnects.\(^{[125]-[127]}\) It is likely that interconnects containing graphene are stressed with large currents over extended periods of time. Also, practical applications require graphene to be on a substrate, which increases charge carrier scattering, resulting in heating/stressing of the graphene channel and altering its electrical properties. Thus designing graphene nanoelectronic structures that maintain the electrical and structural integrity of devices under large current densities presents a challenge. Previous studies on electrical breakdown of graphene\(^{[128]-[130]}\) and carbon nanotube\(^{[131]}\) devices have observed an upper limit of current densities that can be maintained. Higher current densities have resulted in the breakdown of the devices, but the evolution of the electrical properties of graphene during the breakdown process itself has not been explored. Understanding the electrical breakdown process would benefit the design and monitoring of graphene based devices where high current densities are expected.

In this study we report evolution of electrical properties of few-layer graphene (FLG - layer number \(\geq 3\)) devices at intermediate stages of breakdown. We observe a \(p\)-type doping of graphene during the breakdown process along with a concomitant decrease in the electrical conductance. Earlier studies on the electrical breakdown of graphene have either used a single ramp of voltage\(^{[132]}\) where they see an abrupt break in the junction, or have used some form of feedback method to form a narrow junction device.\(^{[133]}\) In such studies the time scale for breakdown is short and there is no opportunity to study the evolution of graphene as the breakdown occurs. In this report we use a feedback controlled method which monitors the change in four-probe conductance closely and increases the time scale of the breakdown process allowing us to unambiguously observe the evolution of the FLG junction near the breakdown region. It is achieved by controlling the current density in the FLG channel close to breakdown causing a reproducible slow breakdown process. This type of feedback controlled method has been successfully used in electromigration of metallic nanowires to produce nanogaps\(^{[102]}\) and to fabricate FLG nanogap electrodes.\(^{[134]}\)

4.2 Experimental Details

4.2.1 Sample Preparation

The test structures used in these experiments are constructed by mechanically exfoliating graphene on 300 nm thick thermally grown \(SiO_2\) supported on a highly \(p\)-doped silicon substrate. FLG films are identified using an optical microscope and thickness confirmed by atomic force microscopy and Raman microscopy using 633 nm wavelength incident laser.\(^{[104]}\) A bowtie geometry is carved out of graphene flakes using electron beam lithog-
raphy (EBL) followed by reactive ion etching in oxygen plasma. The graphene channel is shaped in a bowtie like geometry in order to control the location of break junction formation, by increasing the current density at the narrow region. Four probe non-invasive\cite{135} electrical contacts are defined with electron beam lithography (see Appendix A) followed by electron beam evaporation of Cr/Au (4/40 nm) metals. All electrical tests are carried out at room temperature and under vacuum of $1 \times 10^{-5}$ Torr or lower, using a Lakeshore probe station.

Figure 4.1: (a) A schematic of the feedback control method used to study electrical breakdown of graphene devices. The applied bias voltage is controlled by monitoring the current flow in real time. (b) Scanning electron microscope image of a typical device structure used which shows the bowtie geometry that is carved out in the graphene channel to facilitate higher current densities.

Residue cleaning is performed by annealing the devices in a tube furnace heated at 350°C with $Ar/H_2$ forming gas. A total of 12 devices were electrically tested, out of which 6 were FLG, 3 single layer, and 3 bilayer graphene. Previously we have seen that lithographic residues, from device fabrication practices, can cause unintentional doping and this effect can be minimized by eliminating the solvents in such residues.\cite{103} In the present study, feedback controlled electrical stressing (ES) cycles were carried out on both bare and residue cleaned FLG devices. We observed reproducible slow breakdown process in all our FLG devices and residue cleaning did not affect the overall behavior of our devices during ES cycling. Furthermore, in both cleaned and bare samples, single layer and bi-layer graphene devices proved to be difficult to control and would break abruptly within the first ES cycle with no reproducible slow evolution. However, break junctions were formed on all of our devices using the feedback control method.
4.2.2 Electrical Stressing Using Feedback Controlled Method

Figure 4.2 is a flow-chart that explains the core process by which the feedback control method works. During each individual ES cycle the FLG device undergoes a controlled reduction in its conductivity at the high bias region. In each ES cycle, the voltage across the source-drain ($V_{SD}$) electrode is increased in succession at a rate of 30 mV/s and the 4-probe conductance of the device is monitored, using non-invasive voltage probes close to the narrow junction. As the conductivity decreases by a manually preset value (typically 1-3%), the $V_{SD}$ is ramped down about 500 mV at a rate of 300 mV/s to prevent abrupt breaking of device. The voltage ramping process is repeated to further reduce the conductivity controllably. After decreasing the conductivity by a desired value, the $V_{SD}$ is ramped back to zero. This procedure constitutes one ES cycle. The transfer curve of the device is measured after each ES cycle, and the whole process is repeated until the FLG device breaks down. All ES cycles are carried out at zero gate voltage. This procedure for electrical stressing using this feedback control mechanism is adopted from [102].
4.3 Results

4.3.1 Breakdown Process

Figure 4.3 represents all transfer curves of the same device after each ES cycle. As the applied bias voltage reaches $V_{SD} \approx 1.5$V in the first ES cycle, shown as red squares in Fig. 4.3a, the current in the FLG device starts to deviate from a linear trend due to resistive heating of junction. With further increases in $V_{SD}$, the current starts to decrease and reaches the preset value. At this stage $V_{SD}$ is ramped back to zero volts and the transfer curve of
the device is measured at low-bias $V_{SD}$. A shift in the charge neutrality point (CNP) from a positive $V_{CNP} \approx +9.6\,\text{V}$ towards negative $V_{CNP} \approx -8.4\,\text{V}$ is observed (Red squares Fig. 4.3b). A maximum sheet current density of $2.7 \times 10^8 \,\text{A/cm}^2$ is observed during the onset of breakdown process. With further ES cycles, the device shows a decrease in overall low-bias transconductance, in addition, the CNP shifts to higher positive gate voltages indicating $p$–type doping of the FLG channel as shown in Fig. 4.3b. There is a reduction of hole mobility from $2886 \,\text{cm}^2/\text{V}\,\text{s}$ to $797 \,\text{cm}^2/\text{V}\,\text{s}$ within the first two ES cycles. It is seen that with multiple ES cycling the high-bias channel conduction decreases indicating a decrease in channel width, and further ES cycling by increasing the $V_{SD}$, leads to breakdown of the junction. Figures 4.4a and 4.4b show SEM images of nanogap formation after final ES cycle: Shown as orange spheres in Fig. 4.3a.

![SEM image of FLG device after breakdown. The large bright regions on either sides correspond to the metal source-drain electrodes, and the dark region is FLG. The two metal voltage probes are also seen.](image1)

![Zoomed in SEM image of the narrow central region of the same device as highlighted by yellow box in (a). The bright region is graphene and the dark region is substrate. The arrows show the break junction formed at the narrowest region.](image2)

**Figure 4.4**: (a) SEM image of FLG device after breakdown. The large bright regions on either sides correspond to the metal source-drain electrodes, and the dark region is FLG. The two metal voltage probes are also seen. (b) Zoomed in SEM image of the narrow central region of the same device as highlighted by yellow box in (a). The bright region is graphene and the dark region is substrate. The arrows show the break junction formed at the narrowest region.

In most of our devices, after the initial ES cycle, the CNP moves closer to zero gate voltage. This behavior can be explained due to current induced cleaning of the device at high current densities. Occasionally we also observe secondary dips in transfer curve measurements after initial ES cycles. Similar effects have been observed while stressing graphene devices under high bias and at finite non-zero gate voltages. In such cases charge injection into the gate-oxide layer that are trapped provide local doping, causing shifts in CNP. However, the overall $p$–type doping observed in our case for all devices after each ES cycles cannot be explained just by an oxide charge trap model. The observed effect can be explained by doping of graphene with oxygen. Since our graphene devices are supported on $\text{SiO}_2$, there could be interaction between graphene and oxygen in the silanol ($\text{SiOH}$) groups of $\text{SiO}_2$ at elevated temperatures generated at high current densities. This further indicates that the $p$–type doping may be unique to the choice of
substrate and, although graphene-$SiO_2$ substrate interactions$^{[37, 139]}$ have been studied, their behavior at high current densities remains to be explored.

In addition to the CNP shift indicating $p-$type doping, we also observe an overall decrease in channel conductivity after each ES cycle. This decrease in conductivity could be explained as constriction of channel width due to reconstruction of the FLG edges caused by joule heating$^{[140, 141]}$. This in turn causes higher current densities at the narrow junction and more joule heating. The threshold voltage at which the sheet conductivity starts to decrease also decreases with every cycle. The high-bias induced changes in the FLG channel affects its low-bias transfer properties as seen in Fig 4.3b. Our low-bias transfer curve results bears similarity to earlier reports where graphene devices have been exposed to oxygen plasma,$^{[142]}$ ozone,$^{[143]}$ and $He^+/Ne^+$ irradiation.$^{[144]}$ In such cases, structural defect formation due to chemical treatment is reasoned to be the cause for the decrease in graphene’s conductivity. In comparison, our results indicate that electrical stressing at high current densities cause localized heating. Since there is a thermal mismatch between graphene and the $SiO_2$ substrate, localized heating could result in strain build up in the FLG channel, which further leads to a decrease in conductivity and eventually the breakdown of the graphene device.

### 4.3.2 Joule Heating

![AFM height image of a graphene device after initial ES cycle](image)

Figure 4.5: AFM height image of a graphene device after initial ES cycle. The top portion is a contour plot of height, where the region enclosed by blue dashed line is graphene and the rest is $SiO_2$ substrate. The bottom portion is a line profile of height for the region highlighted in the top image by a horizontal red dashed line.

We now focus on Joule heating of the FLG channel in order to better understand the observed results. Previous experimental work have shown suspended graphene to sustain
high current densities in order of $\approx 10^{10} \text{ A/cm}^2$. However, in the present case our FLG devices are supported on a substrate which limits the maximum current density to an order of $\approx 10^8 \text{ A/cm}^2$. At these current densities the graphene channel experiences joule heating. The AFM height profile across a graphene junction, shown in Fig. 4.5 after an initial ES cycle further indicates that heating is confined to a localized region close to the narrow junction. As the junction is heated, the heat is carried away towards the metal leads and to the substrate. The joule heating effect combined with the bowtie like geometry, creates a temperature gradient within the graphene channel. Although an analytical model for joule heating in metal nanowires have been calculated, here we utilize a finite element simulation method (COMSOL) to obtain both heating and thermally induced stresses in our graphene device.

Figure 4.6: (a) Finite Element Simulation of the Joule heating in a graphene channel. The bowtie geometry of the device causes the narrowest region of the channel to heat the most, as expected. (b) A line cross section of the data showing temperature versus channel length. The cross section is taken across the length of the device (from left metal contact to right metal contact), at the middle of the narrow constriction, and along the top surface of the channel.

In our simulation, we construct a test structure which comprises of a graphene channel of length $2 \mu m$ shaped like a bowtie. This graphene channel is electrically contacted by gold metal electrodes on either sides and the whole structure is resting on a 300 nm SiO$_2$ substrate. The structure is initially set to room temperature ($300 \text{ K}$). The test device is then voltage biased, such that, the same maximum current flows in the test device as in our actual device, shown in Fig. 4.3a.

Figure 4.6a shows the simulated Joule heating in our test structure. As expected, the heating is confined to the narrow junction in the graphene channel. A line profile taken using the simulated data along the length of the channel, see Fig 4.6b, reveals a temperature of about 1000 K at the center of the channel. This corresponds to a temperature rise of 700 °C. The metal leads being large in comparison to the graphene channel act as heat sinks.
Figure 4.7: (a) SEM image of a FLG device after breakdown showing the residual effects of heating profile. The lithographic resist residues has not been cleaned in this device. (b) Even with residue cleaned device, the remnant heating profile is observed after the device undergoes breakdown. In both figures, the graphene channel is enclosed within the dotted box and the rest is SiO$_2$ substrate.

Although the heating in the graphene channel occurs during the passage of high current, its remnant effects are observed in most of our devices. The temperature profile shown in Fig. 4.6a has striking similarity with SEM images of devices taken well after breakdown. Figure 4.7 shows two devices in which the Joule heating has left a mark on the graphene channel. The shape of the remnant heating residue and that of our simulations have similar curvature, within some scaling factor. The remnant heating residue is observed regardless of whether the cleaning procedure to remove lithographic resist residues is undertaken.

Graphene is known to have a negative thermal expansion coefficient ($\alpha_{TEC}$) in the temperature range of 0 – 700 K.\[148] In our simulations, for graphene, we have used a value $\alpha_{TEC} = -8 \times 10^{-6} \text{K}^{-1}$, which is consistent with previously reported values.\[149, 150] The SiO$_2$ substrate on the other hand has a positive thermal expansion coefficient value, and we use a value $\alpha_{TEC} = +8.5 \times 10^{-6} \text{K}^{-1}$ in our simulations.

The SiO$_2$ layer expands (contracts) whereas the graphene sheet contracts (expands) as the temperature rises (falls). This TEC mismatch induces a biaxial tensile or compressive strain on the graphene channel as temperature deviates from room temperature. When the temperature rises further, graphene may slip on the surface of the substrate because the tensile strain increases significantly over the weak van der Waals force which pin the graphene on the substrate. Since our graphene channel is also held down at the ends with metal contacts, such slipping action over the surface of the substrate is restricted. This further increases the stress in the graphene sheet.
Figure 4.8 (a) Surface stress component in the direction along the length of the graphene channel (parallel to current flow) induced due to thermal mismatch between graphene and SiO$_2$ substrate. (b) Surface stress component in the direction perpendicular to the length of graphene channel due to the same thermal mismatch. (c) Cross section data of both parallel and perpendicular stress components of the channel as a function of channel length. Stress values are in $10^9$ Nm$^{-2}$ scale.

We have calculated the surface stress values in our graphene channel due to Joule heating. Figures 4.8a and 4.8b show surface stress component along the direction parallel and perpendicular to length of the channel respectively. Cross sectional line profiles (as shown in Fig. 4.8c), for both the stress values, across the length of the graphene channel, show the variation more clearly. The perpendicular stress component is higher than the parallel stress component in the narrow portion of the channel. Both components have a positive value near the narrow junction and a negative value close to the contacts. Here a positive stress value indicates a tensile stress, and a negative value, a compressive stress. Thus the graphene channel experiences maximum tensile stress at the narrow junction, thereby causing breakdown in this region.
4.4 Conclusions

In conclusion we have demonstrated that we can study the evolution of the electrical properties of graphene junctions close to breakdown by employing a feedback control method. This feedback control method allows slow evolution of resistances, thereby increasing the time scale of the breakdown process. Precise control over the resistance increase is achieved, after which the gate response of the device can be measured. A decrease in overall conduction of the FLG channel is observed in addition to substrate induced $p$-type doping close to breakdown. Addition of structural defects due to thermally induced stress is proposed to be the cause of the observed evolution. Monitoring the electrical properties of graphene devices that carry large current densities, could thus avert any changes in its electrical properties and could prevent breakdown of device. Furthermore, our simulation model can be extended to study heat transport in graphene structures at high current densities, close to electrical breakdown.
Chapter 5 Doping and Environmental Effects

5.1 Introduction

Graphene has tremendous potential use as a component in future nanoelectronics and sensors due to its high electrical mobility and the fact that all the mobile charge carriers reside completely on its surface. In an effort to improve such nanoelectronic devices, considerable effort has been made to remove residual contaminants on graphene resulting from the nanolithography. Poly (methyl methacrylate) (PMMA) is ubiquitously used to prepare graphene devices and has been known to leave such residue\[99–101\] which can affect the electrical properties of the graphene. This PMMA residue is generally understood to $p$–dope the underlying graphene,\[151,152\] though reports of graphene devices placed on highly-cross-linked PMMA seem to contradict this view.\[153\] Moreover, there has recently been tremendous interest in doping graphene surfaces,\[30–33,38\] particularly in specific localized regions in order to controllably form $p$–$n$ interfaces within the material.\[112,154,155\]

Here we show that variable doping levels of the graphene and few-layer-graphene devices result from the different methods of thermally processing the PMMA, pointing to a potential way of localized doping with this polymer coating. The low-temperature thermal dependence of the doping level suggests that residual solvent contained within the PMMA plays an important role in controlling the doping of few-layer graphene (FLG) devices. The importance of the solvent is determined through in situ measurements performed in a glove bag environment that allows for the application, annealing, and electrical measurement without the need for intervening ambient exposure steps which could potentially complicate the interpretation of results.\[80,151\] These measurements show that an applied PMMA coating in $N_2$ environment $p$–dopes the graphene devices. However, after a relatively short ($\approx$ one hour) and low-temperature ($< 200$ °C) annealing process of PMMA encapsulated graphene devices we observe significant $n$–doping. For multi-layer graphene devices (with layer number $\geq 2$) we even observe an overall net $n$–doping. We also show that this $n$–doping persists after exposure to ambient conditions for more than a month. The dependence of the PMMA doping of graphene on annealing suggests that it is due to the variable amount of residual solvent contained within the polymer layer. This solvent-effect is corroborated by reapplication of solvent after annealing, showing a dramatic increase in hysteretic switching of the device between the $p$–doped and $n$–doped states upon gate voltage cycling. A final annealing step removes the solvent again and returns the device to the $n$–doped state having minimal hysteresis. The common use of PMMA in nanolithography processing makes it a potentially useful localized doping agent for few-layer graphene and other two-dimensional materials.
5.2 Experimental Setup

To construct the few-layer graphene test devices used in these experiments we start with a highly $p$-doped silicon substrates with 300 nm of thermally grown $SiO_2$ which are cleaned in an one inch diameter tube furnace for approximately an hour at 400°C with $Ar/H_2$ (flow rates 340:380 Standard Cubic Centimeter per Minute (SCCM)) forming gas to minimize the hydrophilic silanol (SiOH) groups.[37] The substrates are then heated at 400°C for between 45 minutes to 1.5 hours on a hotplate inside a glove bag (Sigma Aldrich AtmosBag-Z118354) with dry Nitrogen ($N_2$) flowing to maintain relative humidity (RH) at 0.0% (monitored by a Lufft C200 humidity meter). After heating, the substrates are allowed to cool to room temperature and few-layer graphene is mechanically exfoliated on $SiO_2$ substrates in the $N_2$ environment before venting the glove bag in order to reduce potential contamination trapped between the graphene and the substrate. The substrates with few-layer graphene are then processed in the furnace with forming gas ($Ar/H_2$ at 400°C) (flow rates 340:380 SCCM) to remove tape residue. Graphene flakes are then optically identified and thickness confirmed by Raman microscopy using a 633 nm wavelength incident laser.[104] Four probe non-invasive[135] electrical contacts are constructed with electron-beam lithography (see Appendix A) followed by electron-beam evaporation of Ti/Au (10/50 nm) electrodes. The graphene channel is cut using oxygen plasma by reactive-ion etching (Oxford instruments Plasmalab80plus). The devices are further cleaned in a furnace (under $Ar/H_2$ at 250°C with a flow rate 340:380 SCCM). Prior to initial testing the devices undergo vacuum annealing at 120°C for 24 hours at a pressure below $10^{-4}$ Torr. It is noted that the lab relative-humidity (RH) varied from 17% to 61% over the course of several months in which it took to complete all the measurements reported here.

5.2.1 Environmental Control

Controlled environment is achieved by continuously flowing $N_2$ into the glove bag and sealing off any large areas to avoid air flow into the bag. A small opening is maintained to let the excess $N_2$ out of the bag, in this way a slight overpressure is created inside the bag, thereby maintaining the relative humidity at 0.0%. All the required electrical testing equipment is incorporated inside the glove bag to ensure in situ measurements of our devices. Figure 5.1a shows a schematic of the experimental set-up. Figure 5.1b is an image of in-house built probe station.

5.2.2 Electrical Testing

For a given applied gate voltage, the electrical measurements are performed by alternating the direction of a low-bias voltage (between 5 and 20 mV) with square-wave form at 0.91 Hz and measuring the resulting current and voltage drop across the non-intrusive side-electrodes in order to null-out contact resistances and offsets. In all of the experiments reported here the gate voltage is swept at the rate of 0.6 V/s. It is noted that the device response remains unchanged while the sample is kept under $N_2$ atmosphere for extended periods of time (for at least the experimentally determined minimum of 16 hours).
5.3 Results

5.3.1 Environmental effects on bare device

Figure 5.2a shows the variation in the electrical sheet conductivity of a single-layer four-terminal graphene device subjected to various environments. After long term exposure to ambient for about 30 days the charge-neutrality-point (CNP), the point of minimum conductivity, is located at the high positive back-gate-voltage ($V_g$) of about 37 V, indicating the graphene is $p$-doped[138] as seen by the black squares in Fig. 5.2a A slight hysteresis in the device is also observed which is commonly attributed to adsorbed molecules like water on graphene or the charging and discharging of oxide traps.[156–158]

The $N_2$ environment in itself does not seem to effectively regenerate the devices after exposure to ambient air and there is negligible change to the estimated electron and hole mobilities. After an hour of the device being in the $N_2$ environment it shows negligible change in its behavior as shown by the green circles in Fig. 5.2a However, after the sample is thermally annealed at 180°C for 1.5 hours in $N_2$ within the glove bag environment there are significant improvements to the device’s CNP, hysteresis, and electron mobility. The
Figure 5.2  (a) Conductivity of a single-layer graphene device under various environmental conditions. Inset: AFM image of a typical device showing four-probe geometry. (b) Result of ambient air exposure on conductivity of same device in figure 5.2a at three different stages. Inset: Decrease in hole mobilities as device is exposed to ambient air. (c) Hysteresis in conductivity as device is exposed to ambient air.

CNP moves significantly closer to zero while the hysteresis is reduced by a factor of two, and the hole mobility has increased by a factor of 1.55 to a value of $4100 \text{ cm}^2/\text{Vs}$. After heat-treatment, the sample properties are maintained while located in the glove-bag under the $N_2$ environment (as determined by tests up to 66 hours in duration). Similar results have been confirmed through regeneration experiments we have performed on 9 different samples comprising single, bi-layer, and multi-layer graphene channels.

Upon re-exposure to ambient conditions single-layer graphene devices quickly return to their behavior prior to thermal annealing within the glove bag. Figure 5.2b shows four-probe conductance measurements of the same single-layer graphene sample in Fig. 5.2a at three different times after it is exposed to ambient laboratory air by venting the glove bag. These measurements demonstrate a fast return to the transport properties of the graphene just prior to regeneration upon exposure to ambient, i.e., a rapid rise in the CNP, increase in hysteresis, 5.2c and decrease in charge carrier mobility (Inset Fig. 5.2b).
Here are the definitions to key words used in the current text

- **Hysteresis** The gate voltage is swept from $0 \rightarrow +V_g \rightarrow -V_g \rightarrow 0$. The conductivity of the graphene device need not retrace itself as the $V_g$ is swept, this leads to ambiguity in its value which depends on the direction of gate sweep.

- **CNP-R** The position of the CNP in Volts when sweeping $V_g$ from high positive voltage is denoted by CNP-R

- **CNP-L** The position of the CNP in Volts when sweeping $V_g$ from high negative voltage is denoted by CNP-L

### 5.3.2 Polymer Encapsulation

![Figure 5.3](image)

Figure 5.3 (a) A Schematic and optical image of device covered with polymer droplet. Scale bar $500 \mu m$. (b) Variation in sheet conductivity of single-layer graphene device in ambient, after thermal regeneration in $N_2$, with a PMMA capping layer in $N_2$ prior to annealing, and with a PMMA capping layer after annealing in $N_2$. (c) Contact conductivity variations of same device in 5.3b under same processing conditions.

We now investigate the device response to the addition of a PMMA encapsulation layer. For these tests, the samples are initially regenerated in the $N_2$ environment as performed above (see Fig. 5.2a) and allowed to cool to room temperature within the glove bag. While the device is contained within the $N_2$ environment, a small drop of PMMA (molecular weight 950) at 2% concentration dissolved in anisole solvent (prepared by Microchem) is applied to the device covering all of the graphene and adjacent metallic electrodes using a
micropipette inside the glove bag. Figure 5.3a show respectively a schematic illustration and an image of an actual few-layer graphene device with PMMA encapsulation. The typical thickness of a dried PMMA droplet is verified by a profilometer to be \( \approx 1\mu m \). After application of the PMMA, the device is allowed to dry within the \( N_2 \) atmosphere for approximately 30 minutes and then electrically measured while it is still contained within the glove bag environment. These electrical measurements (the green diamonds in Fig. 5.3b) show that the CNP has increased slightly compared to the bare-regenerated behavior represented by the red triangles. For all 4 few-layer graphene samples we have measured the CNP point shifts to higher gate voltage after application of a PMMA drop. This increase in the CNP is consistent with \( p^- \) doping of the graphene induced by the PMMA layer in agreement with the general consensus.[151, 152]

However, when these same PMMA encapsulated graphene devices are annealed under \( N_2 \) the CNP moves in the opposite \((n^-\)doped) direction in relation to the regenerated state. For the sample shown in Fig. 5.3, annealing the PMMA encapsulated device for 120 minutes at 180°C under \( N_2 \) atmosphere decreases the CNP by approximately 9 volts with a corresponding increase in the mobility by a factor of 1.23 and a reduction in hysteresis (blue circles in Fig. 5.3b). Since the dielectric constant of PMMA is known not to vary significantly upon annealing,[159] we can estimate the change in the doping level of the device as \(-8.54 \times 10^{11} \text{ cm}^{-2}\).

Conductivity of the metal-graphene contacts is found by taking the difference between the overall 2-probe conductivity and the 4-probe conductivity of the device and is termed as **Contact Conductivity**. With the same polymer processing conditions, changes in the contact conductivity is observed as shown in Fig. 5.3c. This indicates that the metal-graphene contacts are sensitive to their local environments.

When estimating changes in the doping level and charge carrier mobilities, it is important to take into account the alteration in the electrical coupling to the back-gate due to a changed dielectric environment. Despite the fact that the PMMA encapsulation is on top of the graphene, it can still influence the gate coupling due to fringing field lines from the top of the channel to the back-gate. We have estimated this change in coupling through finite-element simulations of \( 2000 \times 322 \text{ nm} \) graphene sheets placed on \( 300 \text{ nm SiO}_2 \) substrate (see Fig. 5.4). We find that modeling with a 1.5\( \mu \text{m} \) thick encapsulation layer having a dielectric constant of \( \kappa = 3.1 \) (a value consistent with previous reports [159]) results in an increase in gate coupling by a factor of about 1.3 – a factor which is incorporated in the above doping level estimate, and is too small to account for the observed changes in the CNP.
Figure 5.4 Finite element analysis of gate-capacitance variation with polymer capping.

This negative shift in the CNP of annealed-encapsulated single-layer graphene is even more pronounced for few-layer graphene devices consisting of two or more layers. In fact, of the 4 few-layer devices we have measured, 3 have shown a negative CNP after encapsulation with an annealed PMMA drop. Figure 5.5a shows transport measurements of a bare-regenerated bi-layer graphene device having a CNP of roughly 6 volts (red triangles). After a PMMA drop is allowed to dry on this sample without breaking to ambient, the CNP shifts in the positive direction to 20 volts, implying a change in charge doping of $1.46 \times 10^{12} \text{ cm}^{-2}$. When this same sample is annealed in $N_2$ at 180°C for 2 hours the CNP is reduced to approximately -20 volts, corresponding to an approximate doping change of $-3.80 \times 10^{12} \text{ cm}^{-2}$, or a net doping level of $-1.90 \times 10^{12} \text{ cm}^{-2}$ (relative to zero). This $n$–type doping persists after the sample is exposed to ambient for 42 days as seen in Fig. 5.5b. These measurements in Fig. 5.5b show that the ambient atmosphere still tends to slightly $p$–dope the graphene device even when encapsulated with PMMA, but the evolution is much slower and the overall position of the CNP remains on the negative $V_g$ side.
Figure 5.5  (a) PMMA encapsulation-process dependent doping for a bi-layer graphene device.  (b) Doping stability in bi-layer graphene device after exposing to ambient air for 42 days.

5.3.3 Role of Solvent

The likely cause of the change in doping for few-layer graphene devices upon annealing of PMMA is due to the removal of remnant anisole solvent. This is supported by experiments we performed in which a droplet of anisole was placed on the same bi-layer PMMA annealed device. The blue circles in Fig. 5.6b is the initial response under dry N\textsubscript{2} of the device encapsulated with annealed PMMA, showing very little hysteresis and a CNP of about −20V. Without breaking the device to ambient, we placed a single small (< 0.1\(\mu\)l) drop of anisole on the annealed drop of PMMA. Immediately after application of the anisole drop the PMMA encapsulation layer developed a network of cracks (Fig. 5.6a) and the device’s electrical response became extremely hysteretic (red pentagons in Fig. 5.6b). This hysteretic behavior suggests that the solvent behaves as a negatively charged impurity contained within the PMMA, inducing shifts in the CNP of ≈ 35V upon cycling the gate. The large hysteretic behavior is seen in Fig. 5.6c to be relatively stable for seven gate sweep cycles lasting over a period of 45 minutes.

This hysteretic response has a CNP-R which is very close to +20V CNP for non-annealed PMMA encapsulation (see Fig. 5.5a) while the CNP-L has a value very close to the annealed PMMA value. This suggests that a positive \(V_g\) attracts the negatively charged solvent towards the gate and closer to the bi-layer graphene surface, resulting in \(p\)-doping. A negative \(V_g\) would thus repel the solvent away from the bi-layer graphene surface and result in \(n\)-doping, as is seen in Fig. 5.6b and 5.6c. Moreover, the CNP-R is seen to be slowly shifting towards zero \(V_g\) while (in contrast) the CNP-L stays pegged (close to the value of pre-annealed PMMA). This slow evolution of CNP-R suggests a gradual evaporation of the anisole from the PMMA. Further evidence that the large hysteresis and doping variation is due to the anisole solvent is obtained by performing a final anneal in \(N_2\) at 180°C for an hour. This final anneal restores the annealed PMMA state with a CNP ≈ −20V and minimal hysteresis, as shown by the green triangles in Fig. 5.6b which indicates that the anisole solvent has been driven completely out of the PMMA. In addition to providing insight into
the effects that remnant solvent can play in the induced doping of graphene devices, the above measurements demonstrate a method of significantly increasing the gate hysteretic response of graphene devices by about an order of magnitude through the use of a PMMA encapsulation layer, which may have utility in memory storage applications.[160] [161]

5.3.4 Humidity and Oxygen Tests

Figure 5.7a shows that the onset of hysteresis is slowed down by polymer capping in contrast to bare devices (Fig. 5.2c) exposed to ambient air. The amount of CNP shift and hysteresis is further reduced by annealing the polymer in \( N_2 \) (Fig. 5.7b). In few-layer graphene devices, we have already observed that the doping remains fairly stable (5.5b) even with the device being exposed to ambient air for more than a month. These results indicate that we are able to reduce the degrading effects of ambient exposure on graphene devices by encapsulating them in a polymer matrix. Although the polymer provides a bar-
Figure 5.7: (a) The onset of hysteresis is observed to decrease with PMMA applied in N₂. (b) Onset of hysteresis is further suppressed with annealing the PMMA capping in N₂.

Carrier to the $p$–doping effects of air, it is not completely protecting the underlying device. Moreover, since a non-zero hysteresis evolves as the encapsulated device is exposed to air, the polymer capping is thus assumed to be a semi-permeable barrier. To further investigate this onset of hysteresis, polymer encapsulated graphene devices are subjected to water vapor and oxygen environments.

Water vapor tests were performed by first purging N₂ through the glove bag and then bubbling N₂ through de-ionized water in another gas line with a flow rate control valve. Electrical transport data was taken continuously in dry N₂ as the valve was opened to allow N₂ to flow through the bubbler after the first full gate sweep. Initially we set low N₂ flow through the bubbler, and we measured the humidity rise in the glove bag, but after a few minutes we observed the humidity to saturate so we increased the flow in order to increase the humidity as shown in Fig. 5.8c. We wanted a time-measure on humidity so we took a note of the value every time we were at $-50\text{V}$ on the gate voltage sweep cycle (since this is time stamped– the automated Labview program allows us to keep track of the exact time between gate sweeps). We chose $-50\text{V}$ since we start from 0 and go positive and then negative, and by the time we are at the maximum negative voltage, the device has undergone one full sweep in both directions.

The above set up was maintained and the gas flow to the bubbler was turned off. A third gas line with a flow control valve and a flow rate controller was used to flow oxygen for the tests. After purging the glove bag with N₂ for 22 hours to eliminate water vapor, and with humidity meter reading 0%, electrical transport measurements were taken continuously. After the first full gate sweep the O₂ and N₂ gas flow is adjusted to 16:80 SCFH (Standard Cubic Feet per Hour) so that the gases are in the same ratio as in ambient air. Measurements for PMMA encapsulated device is first taken to see the evolution of hysteresis. Measurements on a bare device is taken before and after the data for the encapsulated device is completed. Humidity was continuously monitored to be 0%.
Figure 5.8: (a) Evolution of hysteresis in PMMA annealed device and bare device as they are subjected to variation in relative humidity. (b) Hysteresis evolution is diminished in PMMA annealed device when exposed to oxygen environment at 0% relative humidity. (c) Relative humidity variations during humidity test performed in 5.8a. (d) Hysteresis increase with increase in relative humidity levels in correspondence to 5.8c.

Figure 5.8a shows the evolution of hysteresis when both bare and PMMA annealed devices are exposed to relative humidity in a controlled environment. As the humidity level increases, we observe an increase in the amount of hysteresis which is clear from Fig. 5.8d. This hysteresis increase is due to rapid motion of CNP-R, whereas CNP-L remains relatively pegged to its initial value. This behavior of CNP-R is present even in bare devices, where CNP-R moves more towards high positive $V_g$ in comparison to CNP-L. This onset of hysteresis is observed to be faster in comparison to the onset observed when devices are exposed to an oxygen environment. In the latter case both CNP-R and CNP-L start moving but at a different rate thereby producing lower hysteresis as evident from Fig. 5.8b.

From these tests we can infer that the onset of hysteresis, and doping of the graphene channel by moving the CNP, can be decoupled. When a graphene device is exposed to ambient air conditions, the observed hysteresis evolves mainly due to water vapor interactions, and the oxygen in air helps promote doping by shifting both CNP-L and CNP-R.
5.4 Conclusions

In summary, we have shown that the effects of ambient air on graphene field effect devices can be reversed under $N_2$ annealing in near-ambient conditions. After regenerating few-layer graphene devices in $N_2$ environments, PMMA is applied to their surfaces. This is shown to $p-$dope the few-layer graphene devices as is generally accepted in the field. However, in situ annealing of the PMMA encapsulated few-layer devices shows an overall doping level less than the initial regenerated devices. Annealing PMMA in $N_2$ leads to a change from $p-$type to $n-$type doping for bi-layer and few-layer graphene devices. Furthermore, polymer capping acts as a protective layer and minimizes the process of atmospheric doping. Water vapor is shown to be mainly responsible for the immediate onset of hysteresis when the devices are exposed to ambient air. Annealing polymer in $N_2$ leads to significant changes in the doping level of few layer graphene devices. Annealing PMMA in $N_2$ leads to a change from $p-$type to $n-$type doping for bi-layer and few-layer graphene devices. In situ application of solvent onto PMMA encapsulated devices demonstrates significantly enhanced hysteretic switching between the $p-$doped and $n-$doped states. This indicates that residual solvent levels contained within the polymer play a significant role in the $p-$doping caused by the PMMA layer. Graphene devices can be covered partially with polymer and solvents can be used to dope the covered region, thereby creating differentially doped graphene devices. Such process-dependent, polymer encapsulation induced doping variations, allows controlling the type of external doping present in graphene devices. Finally, the fact that these doping variations are determined by relatively low-temperature thermal processing of the ubiquitous nanolithography polymer resist makes this work of importance for potential future nanoscale graphene device applications.

Copyright © Abhishek Sundararajan, 2015.
Appendix A

Substrate Preparation

The substrates on which graphene devices are fabricated need to be specially prepared. In this study all the devices are fabricated on highly $p^+$ doped silicon which has a thermally grown 300 nm oxide ($SiO_2$) layer grown on top. One side of the oxide is polished and the other is left unpolished, and we use the polished side as the surface on which graphene devices are constructed.

**Materials Required:**

1. Silicon wafer
2. Diamond scribe
3. Pair of flat head tweezers
4. Clean work bench
5. A few clean glass slides
6. Fresh Kim-wipes
7. Access to clean compressed air or $N_2$ gun
8. Wear comfortable powder-free nitrile gloves during the entire procedure

**Procedure:**

1. Place a clean sheet of Kim-wipe on the clean work bench
2. Using flat head tweezers transfer the silicon wafer on the Kim-wipe.
3. Using the diamond scribe, make scratch about half a centimeter long near the edge of the wafer. The scratch has to be made in one attempt keeping the wafer steady and has to be made from inside the wafer towards the edge of wafer. Care should be taken when scribing the wafer since too much pressure tends to shatter the wafer completely. Choose the size of the wafer required before attempting the cut, as the wafer tends to break along the line where the scratch is made.
4. Gently blow away any debris caused by scratching the surface of wafer using a $N_2$ gun.
5. Align the glass slides and transfer the scribed wafer on top using tweezers. Place the wafer such that the scratch mark lines with the edge of the glass slide, and the required size of substrate is overhanging to the side.
Now using a few folded Kim-wipes to protect the top (polished) surface of substrate, gently press on either side of the scribe so that the wafer breaks along the scratched line. Note that a clean break should occur when doing this, since the scribe line is made to facilitate the wafer to break along a preferred crystallographic direction. If the wafer breaks unevenly or shatters, then either the scribe line was not made properly or too much pressure is applied while pressing the overhanging side of the wafer. It is a good practice to hold the opposite side (not overhanging) down firmly while pushing gently on the other side. The glass slide is there to facilitate in orienting the slide and also provides a ledge on which the wafer can break.

Once the required size substrate is cut, gently blow any debris off the surface of wafer with $N_2$. The as cleaved substrates may be used for exfoliating graphene, but for electrical device applications further cleaning of substrates before graphene transfer is required. This cleaning procedure ensures a clean surface of the substrate and also minimizes the hydrophilic silanol (SiOH) groups.[37]

**Cleaning Procedure:**

1. Substrates prepared as above are immersed in Acetone and sonicated for 5 minutes, followed by sonication in Isopropyl alcohol and deionized water for 5 minutes each.

2. Using flat tweezers, and ensuring not to damage the central area of the substrate, the substrates are blow dried in dry $N_2$.

3. The dried substrates are then loaded into the quartz tube furnace (max of 5 at once) mounted on a quartz holder.

4. Annealing of the substrates is carried out at 400°C with $Ar/H_2$ (flow rates 340:380 Standard Cubic Centimeter per Minute (SCCM)) forming gas for one hour.

5. After the furnace is cooled down, the samples are carefully transferred into a sample holder and stored in a desiccant box.

6. For some of the samples used in this study an additional cleaning procedure is undertaken. The substrates are heated at 400°C for between 45 minutes to 1.5 hours on a hotplate inside a glove bag (Sigma Aldrich AtmosBag-Z118354) with dry $N_2$ flowing to maintain relative humidity (RH) at 0.0% (monitored by a Lufft C200 humidity meter). After the heating procedure is complete, the substrates are allowed to cool to room temperature before graphene is mechanically exfoliated inside the glove bag environment.
Graphene Isolation

Graphene can be obtained in several ways, but the two main routes are exfoliation and growth of graphene layers. In exfoliation single layer graphene flakes are isolated from bulk graphite and is achieved commonly by either mechanical cleavage or liquid-phase exfoliation. Graphene can be grown by Chemical Vapor Deposition (CVD), by using precursor gases at elevated temperatures in the presence of a metal catalyst. We focus on mechanical exfoliation technique since all graphene samples in this study are derived from this method.

Mechanical Exfoliation:
In this method we cleave layers of graphene sheets from bulk graphite using mechanical force. There is a certain methodology that need to be used in order to get right amount of graphene (both area and layer thickness) distributed randomly across the area of desired sample surface. In previous the section we discussed the cleaning procedure involved in preparing the substrates on which graphene is placed. Here we give a stepwise procedure to obtain graphene flakes transferred onto the pre-cleaned substrates.

Materials Required:
1 Graphite flakes or HOPG slab. (see Fig. )
2 Scotch tape
3 A pair of tweezers
4 Clean work bench
5 Fresh Kim-wipes
6 IPA (Isopropyl Alcohol) in a squirt bottle
7 Wear comfortable powder-free nitrile gloves during the entire procedure

Procedure:
1 Clean the tweezers and workbench with IPA and dry with Kim-wipes.
2 Cut approximately 5 to 6 inches of tape and place it on the work bench such that the adhesive side is facing up.
3 Anchor down the ends of the tape by taping it (with additional smaller pieces of tape) to the work bench, making sure there is enough length of the original tape still usable.
4 Take a couple of small graphite flakes (If using HOPG go to next step) with tweezers and place them near the center of tape with adhesive side up. Care should be taken here since if too much or too little graphite is chosen, then it is possible to end up with thick graphite layers or scantily dispersed flakes of graphite on the substrate.
5 Hold the HOPG with tweezers and stamp it near the center of tape so that the broad side of HOPG slab is in contact with the tape. Care should be taken here, since it is possible that a large amount of graphite can get adhered to the tape when stamping, thus use light pressure only when stamping the slab on the tape.

6 Cut another piece of tape of the same length as before and fold the ends on itself so they won’t stick when held between fingers.

7 Carefully place this tape on top of tape with graphite/HOPG flakes such that adhesive sides of both tapes face each other.

8 Keeping one end fixed, peel off other end of the top tape away from the fixed tape. Note that the graphite is now transferred on both tapes.

9 Repeat the above two steps several times (Usually takes \( \approx \) 10 to 12 trials), taking note that the entire top tape should be evenly covered with graphite flakes.

10 Once the top tape is covered evenly with graphite flakes, gently peel it off the fixed tape and place over the cleaned substrate such that the adhesive + graphite side is facing the substrate. Care should be taken to avoid any air bubbles or wrinkles in tape.

11 With the tape now on top of substrate, light pressure can be applied to facilitate further adhesion between tape and substrate. The light pressure can be achieved either by using back of a finger nail or by using the broad side of the tweezer wrapped in Kim-wipe. Care should be taken not to put too much pressure as this may cause too much material to be transferred onto substrate surface. Also, gentle unidirectional motion should be used to avoid the tearing of tape.

12 Gently peel off the tape from the substrate in one attempt, avoiding the tape to re-adhere to substrate.

Once graphene sheets are exfoliated onto the substrate, we locate and characterize them. Although graphene is a single atomic layer thick, it can be seen optically. The identification of single layer graphene sheets with optical microscopy is possible with the color contrast caused by the light interference effect on the SiO\(_2\) which is modulated by the graphene layer.\([162, 163]\) Atomic force microscopy (AFM) can be used to confirm the thickness of the graphene piece of interest. The thickness can also be characterized by Raman spectrum analysis of the 2D−peak of graphene.\([104]\)
**Graphene Device Fabrication**

In order to study the electrical properties of graphene, the as exfoliated flakes need to be further processed. In this study, graphene devices are fabricated using the following general procedure.

*Materials/ Tools Required:*

1. Graphene sheets exfoliated on clean substrates. The sheets need to be optically identified and characterized for thickness prior to this procedure.

2. Polymer resists for E-Beam lithography. This includes Poly (methyl methacrylate) (PMMA) of molecular weight 950 (or 495) dissolved in Anisole solvent to make 2% solution labelled PMMA A-2 (a 4% solution labelled PMMA A-4 is also prepared), and MMA (monomer of PMMA: also called co-polymer) dissolved in ethyl lactate to make \( \sim 7\% \) solution.

3. Spin Coater

4. Scanning Electron Microscope with lithographic patterning capabilities (Precision movable stage + beam raster)

5. Thin film metal deposition instrument. In this study an electron-beam evaporator was used.

6. Reactive ion etcher with oxygen and argon gas line inserts.

7. Necessary glass wares, tweezers, chemicals/solvents like Methyl isobutyl ketone (MIBK), N-methyl-2-pyrrolidone (NMP), Acetone, IPA, deionized (DI) water, and compressed air/ \( \textit{N}_2 \). Prepare a solution of MIBK and IPA in ratio 1:3 and store in tight lid container. This solution is used as developer after e-beam lithography.

8. Wear comfortable powder-free nitrile gloves when handling substrate and chemicals.

**Preparing Alignment Marks**

The exfoliated graphene sheets on substrate need to be found both optically and in SEM in order to pattern leads to electrically contact them. For this purpose, we design alignment marks on the substrate that help to locally address the position of graphene sheets. The alignment marks are also used to orient the e-beam lithography stage and electron beam as well.

*Procedure:*

1. Spin coat co-polymer (\( \sim 7\% \) solution) on substrate at 4000 RPM for 45 seconds, followed by soft-baking substrate at 150°C for 90 seconds on a hot plate.

2. Spin coat PMMA A-2 on substrate at 4000 RPM for 45 seconds, followed by soft-baking substrate at 180°C for 90 seconds on a hot plate.
3 Using the bottom left corner of the substrate and the bottom edge as references for origin and angle of orientation respectively, write (expose e-beam) the alignment marks pattern that has been pre-designed earlier using e-beam lithography. This design consists of an array of equally spaced $100 \times 100 \ \mu m$ sized cross marks with individual numerical labels for co-ordinates and covers the majority area of the substrate.

4 Develop the pattern written using MIBK:IPA solution. Immerse the substrate into the solution for exactly 60 seconds, followed by rinsing in IPA, DI water and gently blow dry with $N_2$.

5 The developed polymer must be loaded into the vacuum chamber of e-beam evaporator immediately to avoid continuing development by residual solvents. Ti/Au metal of thickness 5/30 nm is evaporated using e-beam evaporator.

6 After metal deposition, the excess metal and unexposed polymer is removed by immersing the substrate in warm NMP ($\sim 70^\circ C$) heated on hotplate. The substrate is left in the solvent until all excess metal has peeled off of the surface of the substrate which can be verified upon visual inspection. The substrate is then immersed in warm acetone ($70^\circ C$), warm IPA ($70^\circ C$), water and blow dried with $N_2$.

Note: The spin coating parameters of polymer resists reported here are choices made after careful calibration of resist thickness, e-beam dose and deposited metal thickness, and are unique to the process used in this study.

Pattern Design

1 Using the alignment marks written on the substrate, we locate several sheets of graphene flakes using optical microscope. The graphene flakes are labeled accordingly with numerical labels that correspond to the nearest alignment mark to each of the graphene sheet.

2 The substrate is then loaded back into the SEM, and the alignment marks are used to align the stage of the SEM to the coordinates on the substrate.

3 The same graphene sheets found by optical methods is then found in the SEM and saved with the coordinates that correspond to the alignment marks design.

4 These images are used to design patterns using the software specific to the e-beam lithography system. The pattern is then written on the substrate as previously described, and metal is deposited to form leads to graphene. (Steps 1, 2, 4-6 in previous section)

5 Finally another lithography procedure is used to define the shape of the graphene device using PMMA A-4 as the polymer resist for lithography as well as the etch mask (Spin coat PMMA A-4 at 4000 RPM for 45 seconds, followed by soft-baking at 180$^\circ C$ for 90 seconds). The excess graphene is etched away using $O_2$ plasma in a Reactive Ion Etch. (Etch time is calibrated prior to etching of graphene device structures)

A schematic of the lithography steps involved in fabrication of a graphene field effect device is shown in Fig. [I]
Figure 1. A schematic of lithographic steps involved in fabricating graphene field effect device.
Bibliography


EG Steward, BP Cook, and EA Kellett. “Dependence on temperature of the interlayer spacing in carbons of different graphitic perfection”. In: (1960).


[160] Yi Zheng et al. “Gate-controlled nonvolatile graphene-ferroelectric memory”. In: 

[161] Augustin J Hong et al. “Graphene flash memory”. In: *ACS nano* 5.10 (2011), 
pp. 7812–7817.

p. 063124.

graphite on SiO2”. In: *Nano letters* 7.9 (2007), pp. 2707–2710.
Vita

Abhishek Sundararajan was born in Chengalpattu, India and grew up in Mysore, India. He obtained his BS and MS in Physics from University of Mysore, India in 2001 and 2003, respectively. He worked as a Junior Research Fellow at the Indian Space Research Organization (ISRO), Bangalore, India for over a year. He joined the Physics and Astronomy department at University of Kentucky (UK) as a PhD student in Spring 2008. He obtained the MS degree in Physics in Fall 2009 and is currently a PhD candidate in Physics at UK. He is a student body member of the American Physical Society and Materials Research Society.

Publications


**Contributed Talks**

- American Physical Society (APS) Conference, Dallas, TX, 2011

**Poster Presentation**

- 9th Kentucky Innovation Entrepreneurship Conference, Lexington, KY, 2013