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ABSTRACT OF THESIS

PHOTOVOLTAIC CELLS BASED ON COPPER PHTHALOCYANINE AND CADMIUM SULFIDE HETEROJUNCTION

This work focuses on the solar cell based on the heterostructure formed between Copper Phthalocyanine (CuPc) and Cadmium Sulfide (CdS). Two different fabrication techniques were used for depositing the organic and inorganic layers of CuPc and CdS layers respectively. CuPc was deposited by electrodeposition while CdS was deposited by chemical bath deposition. Hybrid CdS/CuPc thin films were obtained from CdS films grown on Glass/ITO by chemical bath deposition followed by electrodeposition of CuPc onto these films and annealing at 250°C after the deposition of each layer. The maximum open circuit voltage (V_{oc}) and the short circuit current density (J_{sc}) obtained for this heterojunction solar cell are 0.59v and 0.7mA/cm² respectively and these are the highest values achieved in literature till date. The materials characteristics and electrical performances of the device were analyzed. The effect of increasing the thickness of CuPc and CdS on the short circuit current density and open circuit voltage were also investigated.

KEYWORDS: Heterojunction solar cell, Copper Phthalocyanine (CuPc), Cadmium Sulfide (CdS), electrochemical deposition, Chemical bath deposition

Sandeep Kumar Marda

10/27/2008

PHOTOVOLTAIC CELLS BASED ON COPPER PHTHALOCYANINE AND
CADMIUM SULFIDE HETEROJUNCTION

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THESIS

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The Graduate School

University of Kentucky

2008

PHOTOVOLTAIC CELLS BASED ON COPPER PHTHALOCYANINE AND
CADMIUM SULFIDE HETEROJUNCTION

THESIS

A thesis submitted in partial fulfillment of the requirements for the degree of Master
of Science in Electrical Engineering in the College of Engineering at the
University of Kentucky

By

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Electrical and Computer Engineering

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2008

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DEDICATION

To my Family and God

ACKNOWLEDGEMENTS

I would like to express my sincere thanks and heartfelt gratitude for my academic advisor and thesis chair Dr Vijay Singh for his guidance and support throughout my thesis. I am very thankful for his constant encouragement and motivation during the thesis. I would like to extend my thanks to Dr Todd Hastings and Dr Janet Lumpp for serving on my thesis committee and providing me with invaluable comments and suggestions for improving this thesis.

I am very thankful to Dr.Suresh Rajaputra and Dr.Sova without whom the thesis would have never successfully completed. I am greatly indebted for their technical support throughout my thesis. I also like to thank people in the group for their technical assistance and support.

My parents and my friends have been great sources of support throughout my studies in the USA. My wife supported me a lot without which this work would not have been possible.

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1. Introduction

The Photovoltaic effect was discovered by Edmund Becquerel in 1839. The first solar cell with enough efficiency for commercial applications was a diffused silicon p-n junction, developed by Bell Labs researchers Chapin, Fuller, and Pearson in 1954 [1]. Earlier solar cells were mainly used in power supplies for satellites and space vehicles but now the focus is more on small-scale terrestrial applications. The continued improvements in the research area will make the solar energy economically viable.

The performance of Organic photovoltaic devices has been improving steadily but these devices still faces some fundamental limitations in terms of efficiency and stability that needs to be overcome. Innovative designs of the photovoltaic cells such as multi-layered Organic/Inorganic heterojunctions may enhance their overall performance. Such a design can increase the light absorption efficiency through complementary absorption of separate portions of the solar spectrum by different layers with specific band-gaps and this might help in minimizing the thermal losses and increasing the overall photon conversion efficiency. We can optimize the performance of these cells by maximizing the desirable processes (light absorption, exciton diffusion, forward electron transfer, charge transport) and eliminating the undesirable recombination processes. This can be achieved by improved charge carrier mobility and slowing down the rate of back electron transfer so that the photo-generated charge carriers can escape from the film before recombination occurs, while maintaining thick enough film to allow most of the light to be absorbed.

Organic photovoltaic devices based on donor-acceptor heterojunctions have been the major focus and areas of improvement in the past. The difference in electron affinity and ionization potential at the interface results in electrostatic forces. If both electron affinity and ionization potential are greater in one material (the electron acceptor) than the other (the electron donor) then the interfacial electric field drives charge separation [2]. The strong electric fields may break up photo-generated excitons if the differences in potential energy are larger than the exciton binding energy. In a planar heterojunction, or 'bilayer' device, the organic donor-acceptor interface separates excitons much more efficiently than the organic-metal interfaces in a single layer device and with very high purity materials efficient photovoltaic devices may be made [2]. Organic-Inorganic hybrid materials not only represent a creative alternative to design new materials and

compounds for academic research, but their improved or unusual features allow the development of innovative industrial applications [3].

1.1 Organic/Inorganic Solar cells

Organic semiconductors are of great interest because of the possibility of large area devices and possibility of producing optoelectronic features of these materials. Organic photovoltaic devices have the advantage of being light weight and low cost. Lot of research has been done in past couple of years on organic semiconductor-semiconductor and semiconductor-metal junctions [4]. Inorganic–Organic photovoltaic devices are promising candidates for renewable sources of electrical energy because of ease in fabrication and low production cost as well as lightweight and flexibility [5]. Inorganic layers have high electron mobility and physical strength, while, organic layers have high luminescence efficiency [6].

1.2 CdS/CuPc solar cell

Thin films of Copper Phthalocyanine (CuPc) and their heterostructures with a number of organic/inorganic materials have shown interesting electronic properties that can be used in photovoltaic applications [7]. CdS thin films have often been used in photovoltaic applications when its surface is doped with Cu atoms. Therefore formation of a complex interface layer was expected during the deposition of CuPc layer on CdS layer [8]. The structure of the device fabricated in this work is as shown below in Figure 1.1.

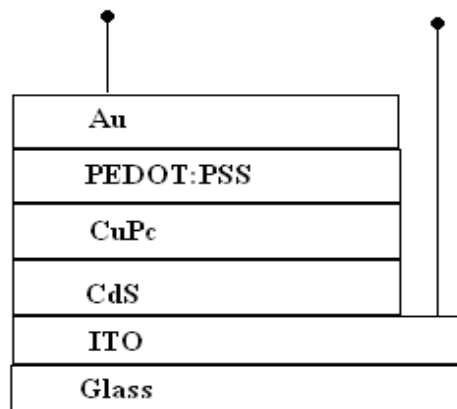


Figure 1.1: The structure of the device fabricated

Disappointing results in single layer organic materials made the researchers to look at two layered structures of Organic/Organic and Organic/Inorganic materials to obtain higher energy conversion efficiency [2]. Organic electronics materials are conjugated solids where both optical absorption and charge transport is dominated by the π and π^* orbital's [2]. Organic materials are very attractive for photovoltaic primarily because of the prospect of high throughput manufacturing. They are of interest for future applications in solar cells [9].

In the above structure CuPc acts as a donor material. Phthalocyanines are a class of semiconductors that are generally p-type, chemically and thermally stable and they exist commonly in two forms, α and β forms. Copper Phthalocyanine (CuPc) is p-type organic semiconductor having the hole equilibrium concentration $P_0=2.3 \times 10^{13} \text{cm}^{-3}$, the mobility $\mu_p=1.1 \times 10^{-2} \text{cm}^2/\text{Vs}$, the dark electrical conductivity $\sigma_p=4 \times 10^{-8} \Omega^{-1} \text{cm}^{-1}$ and the equilibrium Fermi level located at 0.5eV above the valence band [10]. The chemical structure of CuPc is as shown below in Figure 1.2. It is a conjugated molecule characterized by 2-dimensional π electrons delocalized.

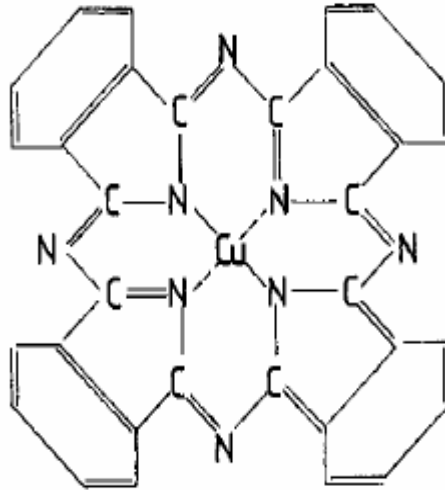


Figure 1.2: The chemical structure of CuPc Ref [10]

PEDOT:PSS layer acts as buffer layer and thus makes the top surface more uniform[12]. PEDOT (Poly 3, 4-ethylenedioxythiophene) has excellent transparency in visible region, good conductivity and insolubility in anything and can be electrically or chemically doped [13]. PEDOT:PSS is the most common form used comprising of

poly(styrene sulfonate) abbreviated as PSS. The synthesis of PEDOT:PSS involves polymerization of EDOT monomers in a polyelectrolyte solution of PSS. Polymerization is initiated by removal of charges from EDOT monomers formed in this way and thus promoting polymerization of EDOT units while PSS acts as a counter ion balancing charge residing on PSS [11]. The chemical structure of PEDOT:PSS is as shown in the Figure 1.3.

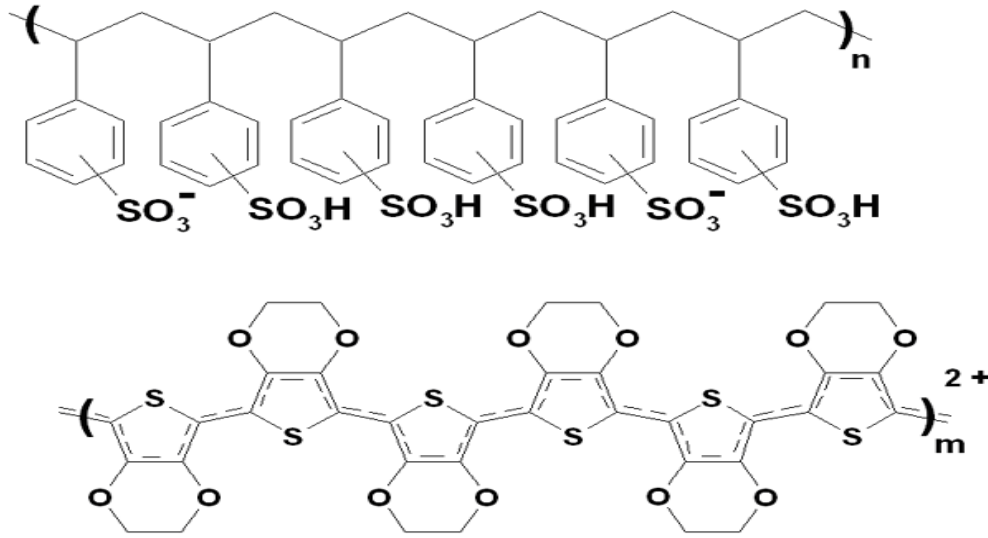


Figure 1.3: Structure of PEDOT:PSS Ref [11]

Cadmium Sulfide (CdS) acts as an acceptor in the device fabricated. It is an n-type semiconductor with a band gap of 2.42eV [14]. In the above structure CdS acts as a window layer allowing most of the light incident on it to pass through it and reach the CuPc layer which is acting as a donor and absorbs the light reaching it. Thus overall the light absorption spectrum is increased which allows more light energy to be absorbed and thus resulting in higher energy conversion efficiency.

In this thesis, Open circuit voltage of 0.59V and Short circuit current density of 0.7mA/cm² has been achieved for the CdS/CuPc based photovoltaic cell. The document focuses on explaining the theory, experimental procedures and the results on the CdS/CuPc based solar cell fabricated. Chapter 2 gives the theory behind the photovoltaic cells, Schottky barriers and heterojunctions. The third chapter describes the experimental procedures and preparation of the samples for characterization of the device. The fourth

chapter deals with the results and discussions on the device fabricated. Chapter 5 provides the conclusion and the future scope for further research.

2. Photovoltaic Cell

A Photovoltaic (PV) cell also known as solar cell is a semiconductor device that converts optical energy to electricity. The first Silicon solar cell was invented by Russell Ohl in 1941, but these early solar cells had energy conversion efficiency of less than one percent. In 1954 a solar cell with an energy conversion efficiency of six percent was developed by Gerald Pearson, Calvin Fuller and Daryl Chapin by creating an array of several strips of Silicon [12]. More than 90% of all the solar cells produced worldwide are composed of the semiconductor material Silicon (Si). As the second most abundant element in earth's crust, silicon has the advantage, of being available in sufficient quantities, and adding to its advantage processing the material does not burden the environment. At some point of time solar cells made of other semiconductor devices are expected to surpass silicon based PV cells in cost and performance.

In addition to optimizing the production processes, work is being done to increase the level of efficiency, in order to lower the costs of solar cells. However, different loss mechanisms set limits on these plans. Different types of losses that limit the performance of solar cells include optical losses, heat losses, material contamination, surface effects and crystal defects, electrical resistance losses [15].

To overcome these limitations, researchers are finding directions to enhance the performance of solar cells and exploring different types of organic and inorganic materials to attain more efficient and cost effective solar cells [15].

Solar energy is natural and solar cells are long lasting sources of energy which can be used almost at any place. It has wide range of applications and it is viewed as the best source for electricity supply, since there are no fuel costs or fuel supply problems, the equipment can usually operate unattended and thus are very reliable and require no maintenance. Photovoltaic solar power is one of the most promising renewable energy sources in the world [15].

2.1 Principle of Photovoltaic cells

Solar cells are essentially semiconductor junctions under illumination. Light generates electron-hole pairs on both sides of the junction, in the n-type side and the p-

type side. The generated electrons (from the p-type side) and holes (from the n-type side) then diffuse to the junction and are swept away by the electric field, thus producing electric current across the device. The electric currents of the electrons and holes reinforce each other since these particles carry opposite charges. The p-n junction therefore separates the carriers with opposite charge, and transforms the generation current between the bands into an electric current across the p-n junction [12]. Practically photocurrent and photo voltage deteriorates in a solar cell because of their carrier losses. Thus to attain a high-energy conversion efficiency, prevention of recombination becomes a very important aspect of the design of solar cell. When the incident photon energy is less than the band gap of the semiconductor, the light is transmitted through the material, that is, the semiconductor is transparent to the light. Thus when the incident photon energy has higher energy than the band gap and is absorbed by the semiconductor, the energy of the photon is transferred to the electrons in the atoms of the cell. With more energy, the excited electron escape from its normal position and thus this movement of electron results in electricity. Thus the cutoff wavelength is also an important parameter to choose the solar cell material because the light with wavelength longer than the cutoff wavelength cannot be used for solar energy conversion [12].

2.2 Types of Photovoltaic materials

The semiconductor materials used in photovoltaic cells can be classified as crystalline and thin film materials. They vary from each other in terms of light absorption, energy conversion efficiency, fabrication process and cost [12].

Crystalline materials (considering single crystal) have very uniform molecular structure which results in high energy conversion efficiency. In case of polycrystalline materials which consist of small grains of single crystal, the energy conversion efficiency is lower when compared to monocrystalline or single crystal materials. A Polycrystalline material have slightly less manufacturing cost but is offset by the energy conversion efficiency when compared to single crystal materials [12].

2.3 Schottky barriers

When a piece of metal is in contact with a semiconductor resulting in either an ohmic contact or a Schottky barrier depending on the interface formed between the metal and semiconductor. Assuming an n-type semiconductor, an ohmic contact is formed with

an n-type semiconductor when a metal having a lower work function than that of the semiconductor (i.e. $\Phi_M < \Phi_S$) is deposited as a contact on the semiconductor surface. When a metal with work function $q\Phi_M$ is brought in contact with a semiconductor having a work function $q\Phi_S$, charge transfer occurs until the Fermi levels align at equilibrium. To align the two Fermi levels, the electrostatic potential of the semiconductor is changed relative to that of the metal. Depletion region W is formed near the junction and the positive charge due to uncompressed donor ions within W matches the negative charge on the metal. The equilibrium potential V_o which prevents further net electron diffusion from the semiconductor conduction band into the metal, is the difference in work function $\Phi_M - \Phi_S$ [16]. As shown in the figure 2.1 the barrier height Φ_B , is defined as the potential difference between the Fermi energy of the metal and the band edge where the majority carriers reside, Φ_M is the work function of the metal and Φ is the electron affinity. A metal-semiconductor junction will therefore form a barrier for electrons and holes if the Fermi energy of the metal as drawn on the flat band diagram is somewhere between the conduction and valence band edge. In addition, the built-in potential, Φ_I , is defined as the difference between the Fermi energy of the metal and that of the semiconductor [16].

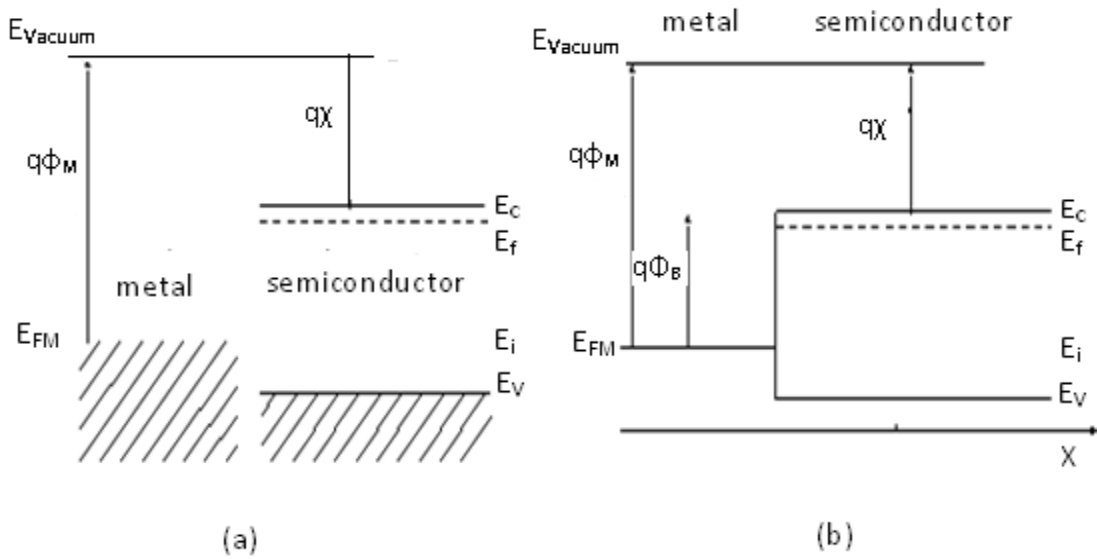


Figure 2.1 Energy Band Diagram of the metal and semiconductor. Ref [17]

The flat band diagram, shown in Figure 2.1 is not a thermal equilibrium diagram, since the Fermi energy in the metal differs from that in the semiconductor. Electrons in the n-type semiconductor can lower their energy by traversing the junction. As the electrons leave the semiconductor, a positive charge, due to the ionized donor atoms, stays behind. This charge creates a negative field and lowers the band edges of the semiconductor. Electrons flow into the metal until equilibrium is reached between the diffusion of electrons from the semiconductor into the metal and the drift of electrons caused by the field created by the ionized impurity atoms. This equilibrium is characterized by a constant Fermi energy throughout the structure as shown in figure 2.2. The notations used in the figures here are as follows: $q\Phi_M$ -work function of metal, $q\Phi_B$ -work function of semiconductor, $q\chi$ -electron affinity of semiconductor, E_{vacuum} -vacuum level, E_{FM} -metal fermi energy level, E_F -semiconductor fermi energy level, E_C -conduction band level, E_V -valence band level [18].

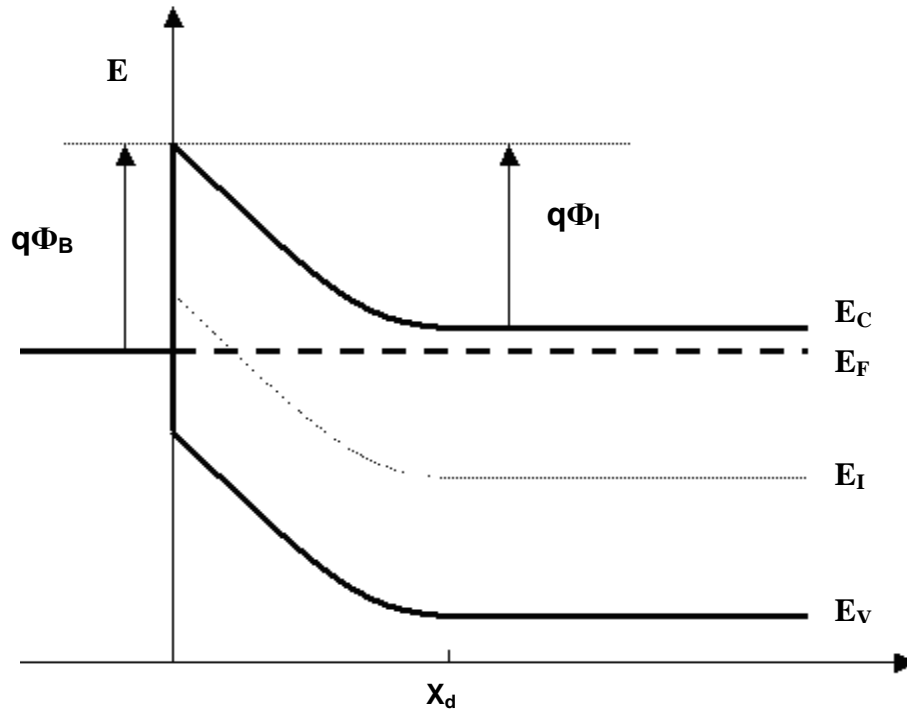


Figure 2.2: Energy band diagram of the metal and semiconductor in thermal equilibrium. Ref [17]

Operation of a metal-semiconductor junction under forward and reverse bias is illustrated with Figure 2.3. As a positive bias is applied to the metal (Figure 2.3 (a)), the

fermi energy of the metal is lowered with respect to the Fermi energy in the semiconductor. This results in a smaller potential drop across the semiconductor. The balance between diffusion and drift is disturbed and more electrons will diffuse towards the metal than the number drifting into the semiconductor [18]. This leads to a positive current through the junction at a voltage comparable to the built-in potential [16].

As a negative voltage is applied (Figure 2.3 (b)), the Fermi energy of the metal is raised with respect to the Fermi energy in the semiconductor. The potential across the semiconductor now increases, yielding a larger depletion region and a larger electric field at the interface. The barrier, which restricts the electrons to the metal, is unchanged so that the flow of electrons is limited by that barrier independent of the applied voltage. The metal-semiconductor junction with positive barrier height has therefore a pronounced rectifying behavior [18]. A large current exists under forward bias, while almost no current exists under reverse bias. The potential across the semiconductor therefore equals the built-in potential, Φ_i , minus the applied voltage, V_a as shown in Figure 2.3 below [16].

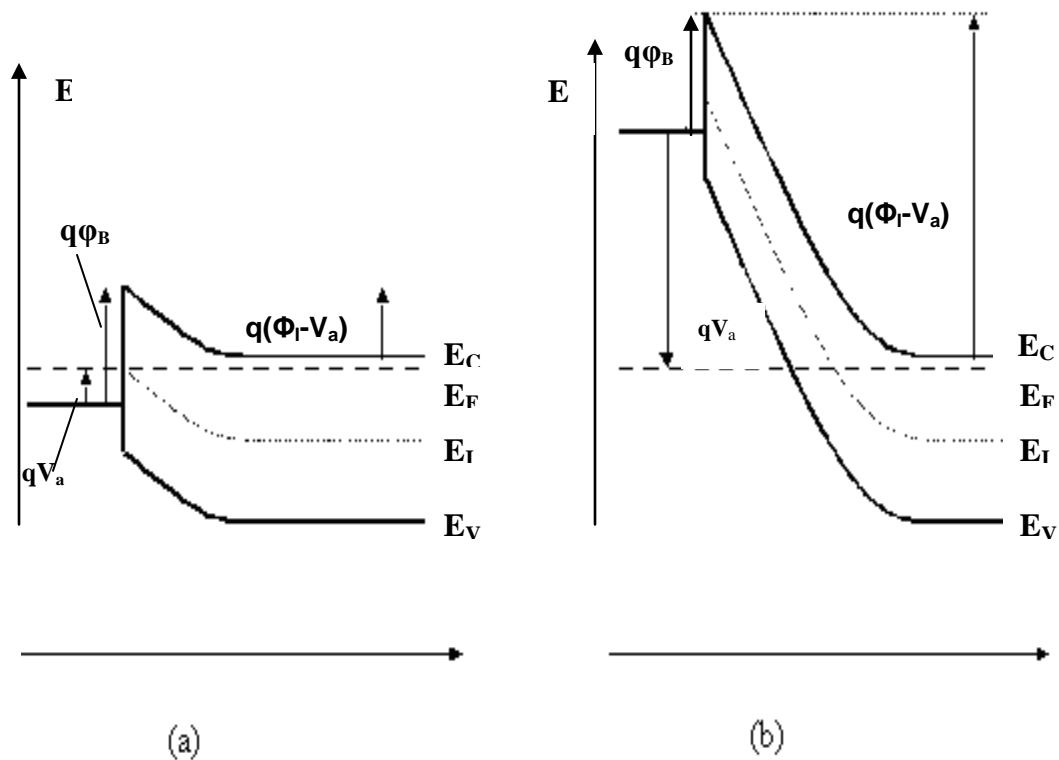


Figure 2.3: Energy Band diagram of a metal- semiconductor junction under (a) forward bias and (b) reverse bias. Ref [17]

2.4 Heterojunction

A junction formed between two semiconductors with different band gaps is called as a heterojunction. Along with band gap another important difference between the semiconductors forming the junction is the refractive index. For fabricating a good quality heterojunction, lattice matching of the two semiconductors plays a very an important role [19]. The energy band diagram before and after the formation of the junction between p and n type semiconductors are shown in Figure 2.4 and Figure 2.5 respectively. When semiconductors of different band gaps, different work functions and electron affinities are brought together to form s junction, discontinuity is expected in the energy bands as the Fermi level lines up in equilibrium. The discontinuities in conduction band ΔE_c and the valence band ΔE_v accommodate the difference in the band gap between two semiconductors. Ideally $\Delta E_c = \chi_n - \chi_p$, $\Delta E_v = \Delta E_c + E_{gn} - E_{gp}$. This is referred to as Anderson's affinity rule [20].

When a junction is formed between semiconductors with different band gaps, the electrons flow from n-type to p-type semiconductor and the holes flow from p-type to n-type semiconductor. This leads to a charge builds up near the junction and thus electric field is built. This electric field extends from the n- side to the p-side of the junction. The photons from the sunlight which have energy between E_{g2} and E_{g1} pass through the n-type semiconductor and will be absorbed by the p-type material. These photons create carriers which are collected at the p-type material. The photons with energy greater than E_{g2} are absorbed by the n-type material leading to the generation of charge carriers in the depletion region and in the bulk of the material. These separated carriers at the junction result in the light generated current.

Heterojunction devices have the advantage over the homojunction devices which require the materials that are doped both n-type and p-type. Many photovoltaic devices (single layer devices) can be doped with only either p-type or n-type but heterojunctions do not have any such constraint and thus many promising photovoltaic devices can be investigated to produce optimal solar cells.

In case of the CdS/CuPc heterojunction based solar cell fabricated in this work, the top and bottom layers in the ITO/CdS/CuPc/PEDOT:PSS/Au structure have different roles to play. The bottom layer or the window layer, CdS in this case is the material with

higher bandgap and selected for its transparency to light. This window layer allows almost all of the light to pass through it and reach the bottom layer. The top layer (CuPc) acts as absorber with lower bandgap that readily absorbs light. This light generates electron very near to the junction which helps to separate electrons and holes before they recombine.

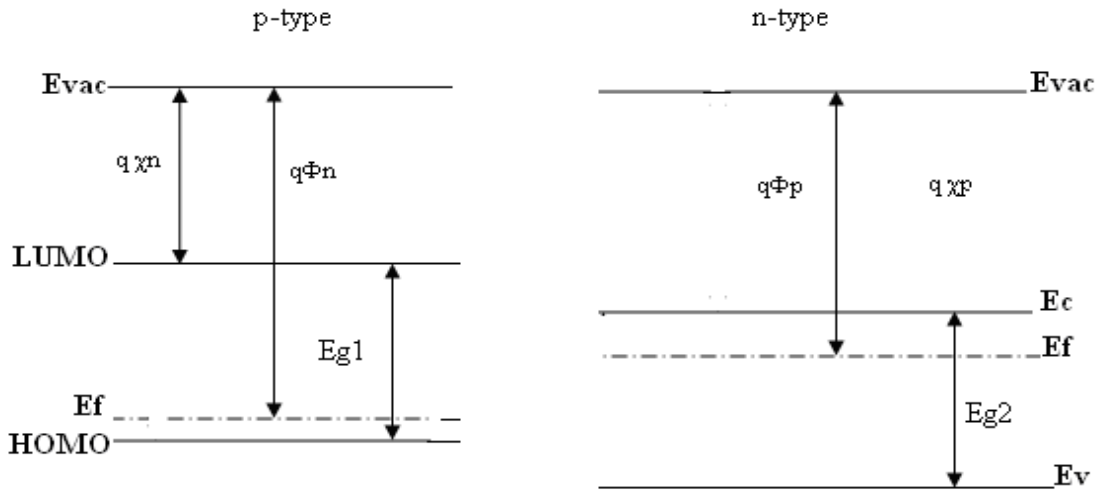


Figure 2.4: Energy band diagram of n-type and p-type semiconductors before the contact.

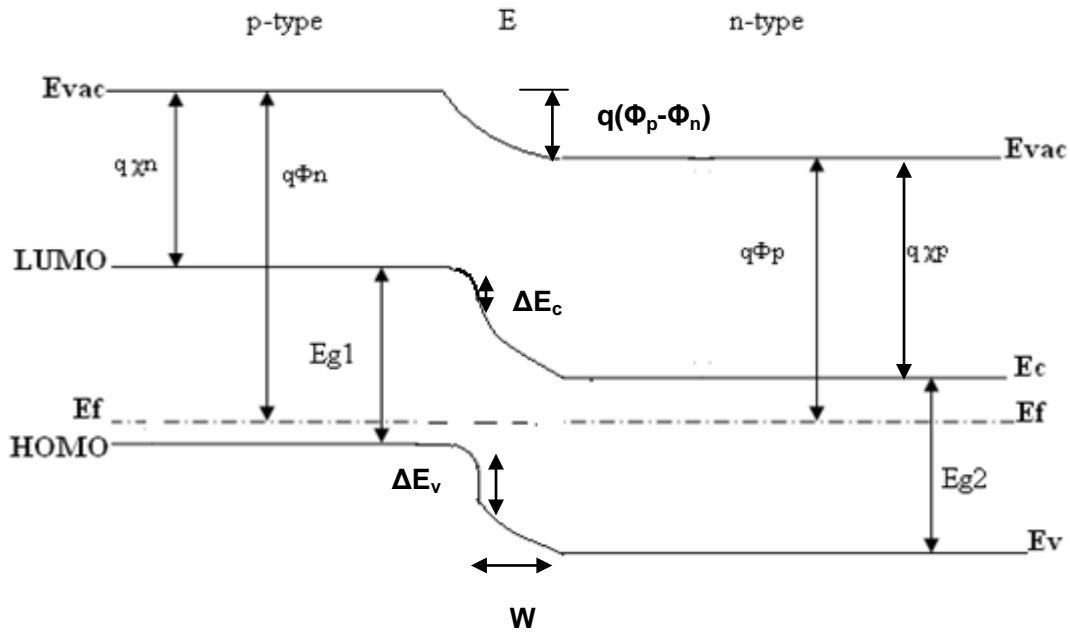


Figure 2.5: Energy band diagram of n-type and p-type semiconductors after the contact.

3. Experimental Procedure

3.1 Fabrication Procedure

The fabrication of the Organic/Inorganic heterojunction involved a sequential procedure of Glass/ITO sample cleaning, Chemical bath deposition of Cadmium Sulfide(CdS), Vacuum annealing, Electrodeposition of Copper Phthalocyanine(CuPc), Vacuum annealing, Spin coating of PEDOT:PSS, Vacuum annealing and finally e-beam evaporation of metal contact. The fabricated cells were characterized using a J-V tester and solar simulator. Samples were also characterized by Electron beam microscopy, X-Ray diffraction and Optical absorption. The structure of the device is as shown in figure 3.1 and the fabrication process is explained below in detail. The top view of the sample is as shown in the figure 3.2. The J-V measurements shown in the next chapter are taken for a typical dot on the sample.

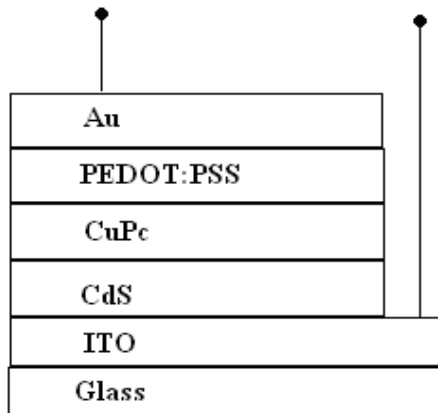


Figure 3.1: The structure of CdS/CuPc Heterojunction solar cell

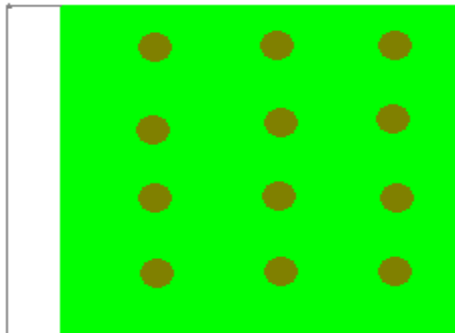


Figure 3.2: The top view of the structure fabricated

3.1.1 Substrate Cleaning

The PV cells based on Organic/Inorganic heterojunction were fabricated on glass substrates precoated with a 10nm thick transparent, conducting ITO anode with a sheet resistance of 4-8 Ω /square. The ITO glass samples were 1 inch x 1 inch in size obtained from delta technologies. Before any deposition, these substrates were cleaned with de-ionized and dried with nitrogen gas. Then the samples were sonicated using ultrasonic bath with acetone and rinsed with de-ionized water. The samples were then again cleaned with de-ionized water and then dried with nitrogen gas. To identify the ITO side of the glass, multimeter was used to measure the resistance on both sides of the glass sample. The surface which showed some resistance had ITO sputtered on it. During this entire process, all the glass samples were handled using tweezers to avoid any contamination of the glass substrates.

3.1.2(A) Chemical Bath Deposition of Cadmium Sulfide (CdS)

The Inorganic layer of CdS was deposited first by chemical bath deposition. A solution of 0.7g of Cadmium Chloride (CdCl_2), 0.72g of Ammonium Chloride (NH_4Cl), 2.3g of thiourea and 200ml of de-ionized water was prepared and heated to 110 $^\circ\text{C}$ with continuous stirring (using a 1 inch magnetic stirrer) till all the particles are dissolved in the solution. 15ml of the solution is taken in a separate beaker and then the sample on which the CdS is to be deposited is dipped in it and then 0.2ml of NH_4OH is added to the 15ml solution. Depending on the required thickness, the sample is kept in the 15ml solution. The whole deposition process is done at 110 $^\circ\text{C}$. During this work the thickness was varied from 50nm to 150nm to see the effect on open circuit voltage and short circuit current density.

3.1.2(B) Electrochemical deposition of Cadmium Sulfide (CdS)

The Inorganic layer of CdS can also be deposited by electrochemical deposition. A solution of 0.5g of Cadmium Chloride (CdCl_2), 0.5g of Sulphur, 60ml of Dimethyl Sulfoxide (DMSO), was prepared and heated to 110 $^\circ\text{C}$ with continuous stirring (using a 1 inch magnetic stirrer) till all the particles are dissolved in the solution. The sample and the electrode were arranged parallel to each other using the sample holder. The size of the platinum electrode was 1x1 inch. The platinum electrode was connected to the positive

terminal of the supply voltage and the sample was connected to the negative terminal. The sample was connected in such a way that the ITO side of the glass faced the platinum electrode. The distance between the electrode and the sample was maintained to obtain a uniform deposition of the inorganic material. The electrodeposition process was done at 110°C, with maximum stirring using a magnetic stirrer, with a DC Voltage of 50V and constant current at 5mA and varying the duration (2min, 5min, 8min 10min) of deposition to get different thicknesses. The thickness of CdS was estimated from the images obtained through spectroscopy.

3.1.3 Vacuum Annealing of Inorganic layer (CdS)

After the deposition of CdS layer on glass/ITO substrate, the sample is vacuum annealed at 250°C for 5 hours in the vacuum chamber at 30 inches of Hg. After annealing for 5 hours the vacuum was allowed to cool down for about 5 hours till the vacuum furnace reached 25°C and then the samples were removed for deposition of the organic layer (CuPc).

3.1.4 Electrochemical Deposition of Copper Phthalocyanine (CuPc)

The organic layer was deposited by electrochemical deposition. A solution of 2ml of Trifluoroacetic acid (TFA), 55ml of chloroform (CHCl₃) and 0.0018gm of Copper Phthalocyanine were taken in a beaker and stirred until all the CuPc was completely dissolved in the solution. First the weight of CuPc was measured using Fisher Scientific. Then the CuPc was taken in a 80ml size beaker. 2ml of TFA was taken in the same beaker and stirred properly to mix all the CuPc. After the CuPc was completely mixed in TFA giving the solution a dark green color, 5 to 6ml of chloroform was added to the solution and stirred. After 1 min of stirring, the beaker was filled with chloroform till the solution reached 60ml. The solution was stirred for 2 minutes using a magnetic stirrer. The sample and the electrode were arranged parallel to each other using the sample holder. The size of the platinum electrode was 1x1 inch. The platinum electrode was connected to the positive terminal of the supply voltage and the sample was connected to the negative terminal. The sample was connected in such a way that the ITO side of the glass faced the platinum electrode. The distance between the electrode and the sample was maintained to obtain a uniform deposition of the organic material. The

electrodeposition process was done at room temperature, with maximum stirring using a magnetic stirrer, with a DC step voltage (120v for 2sec and 0v for 4sec) and varying the duration (4min, 6min, 8min, 10min, 12min, 13min, 15min, 17min, 18min, 20min, 23min, 25min) of deposition to get different thicknesses. The thickness of the CuPc is estimated using the images obtained through microscopy.

During the deposition there were many variables which needed to be taken care of, in order to obtain a uniform deposition and plane surface morphology. To obtain uniform deposition, maximum stirring was used, and the distance between the electrode and sample was at about 1-2cm. The concentration of the solution was also one of the factors to be considered. Another hindrance encountered was the formation of pin holes on the sample. This was reduced by using high stirring rates.

3.1.5 Vacuum Annealing of CuPc

After the deposition of CuPc layer on glass/ITO/CdS, the sample is annealed at 200°C for 5 hours in a Vacuum furnace at 30cm of Hg. After this is done, the furnace is allowed to cool down for 4 to 5 hours till the temperature in the furnace reaches 25°C. Then the samples are removed and the PEDOT:PSS layer is deposited.

3.1.6 Spin coating of PEDOT: PSS

PEDOT: PSS was spin coated on the glass/CdS/CuPc sample. Chemat technology spin coater was used to spin coat PEDOT: PSS at 4000rpm for 40 seconds on the CuPc layer. This layer of PEDOT:PSS helps in smoothening surface of the CuPc layer. The spin coated samples were then annealed in vacuum at 100°C for 2 hours using Fisher-Scientific furnace. Annealing removes the excess water molecules in the PEDOT:PSS layer on the sample and also increases the adhesion between the PEDOT:PSS and CuPc. The samples were left for about 2 hours to cool down to room temperature.

3.1.7 E-Beam Evaporation of Electrode

The metal cathode was deposited via high-vacuum at a base pressure of 8.8×10^{-6} Torr using Torr International E-Beam Evaporator. The density (10.9 g/cm^3) and Z-ratio (0.529) of Aluminum were programmed in the system prior to the deposition. The source had a graphite crucible filled with Gold pallets. The samples were at distance of about

15cm from the source and a maximum of four samples could be placed for a single batch. The samples were covered with a shadow mask of circular holes made from an aluminum foil. The shutter was moved to a position so that the source was covered completely till the melting of Aluminum started. A supply voltage of 8KV was applied and the supply of current to the source was incremented slowly till the Au started melting (at RMS current value of 0.05Amps). Now the shutter was moved to uncover the boat and this allowed Gold deposition on the samples. 65nm-thick Au cathode was deposited with a deposition rate of 0.2Å/sec on the sample resulting in active cell area of 0.07 cm².

3.2 Characterization Procedures

As a part of the thesis, the devices and the structures fabricated were characterized using the following procedures: Optical Absorption Spectroscopy, Scanning Beam Microscopy, X-Ray Diffraction and Electrical characterization.

3.2.1 Optical Absorption Spectroscopy

Most materials absorb some light and the degree to which they absorb light is the function of the wavelength of the light. Optical absorption in the visible and near UV portions of the spectrum is generally the result of the absorption of the light by electrons, ions or molecules and thus the absorption characteristics can yield a lot of information about the electronic structure.

The absorption spectrum obtained from this procedure is used to determine the band gap energy of the material being studied. Optical spectroscopy helps in understanding the optical properties of materials used in fabricating the device. The background used in understanding the optical properties of CdS/CuPc Heterojunction device fabricated is ITO Coated glass conducting surface. Optical spectroscopy helps in understanding the amount of light that is incident on this fabricated device and how much of it is absorbed by the device.

The experimental procedure was carried out using a cray-50 v3.0 UV-visual spectrometer. The plane ITO coated glass substrate was first scanned to use it as a background source. Then the samples fabricated were scanned in the similar fashion against the Glass substrate background between the wavelengths 200nm to 800nm. The

optical absorption is in the units of optical absorbance which is a dimensionless quantity defined as the negative of the base-10 logarithm of the transmission.

3.2.2 X-ray Diffraction

X-ray Diffraction is a technique used to identify the materials, determine the degree of crystallinity, and know the composition of different materials in case of a mixture of different materials. It provides the researchers with a fast and very reliable tool to determine the material composition; however, it does not provide the qualitative compositional data as obtained from Scanning beam microscopy. The pattern of the X-rays diffracted is mathematically related to the structural arrangement of the atoms causing the scattering. The intensity of the diffracted beam also depends on the arrangement of the atoms in the repeated motif called unit cell [21].

When an X-ray beam hits the sample and is Diffracted, the distance between the planes of the atoms can be measured using the Braggs law which states that $n\lambda=2d\sin\theta$ where n is the order of the Diffracted beam, d is the distance between the adjacent planes of the atoms and θ is the angle of incidence of the X-ray beam. The Diffraction pattern is a plot of Intensity versus 2-THETA [22].

The sample was placed on the sample holder and a filter was placed in front of one of the X-ray beam source. The Commander program which was pre-written was run to observe the alignment of the sample in the z-plane. After the sample was properly aligned, the filter was removed and the program was run for 2-THETA values from 3° to 120° . The peaks and their respective intensities were observed from the resulting curve of the program. Thereafter, the spectrum was cross checked with the diffraction spectrum of CuPc and CdS and all the peaks along with their corresponding 2-THETA values were compared.

3.2.3 Electrical Characterization of the solar cell

The electrical characterization helps in knowing the current flowing in the device as a function of voltage applied. It helps in determining the open circuit voltage and short circuit current density for the solar cell and thus helps in further analysis of the device fabricated and determining other important parameters of the solar cell. The electrical characterization was done using a solar simulator. The sample was illuminated in light

with a bulb of 1 sun. A DC voltage using a kepcos supply was given to the ITO of the sample as cathode and the metal contact as anode. In this analysis two Keithley 2000 digital multimeters were used to measure the voltage across the device and the voltage across the resistor. A program written using LabVIEW software is used in recording the voltages and currents. The whole data is recorded as an Excel file. After plotting the J-V curve from the data obtained, the open circuit voltage and short circuit current can be estimated. This data helps in evaluating other parameters required for the analysis of solar cell like the Ideality factor, Efficiency of the designed solar cell.

3.2.4 Field Emission scanning electron microscopy

A Hitachi FESEM (Model S-900) with a maximum magnification power of 800kX at an accelerating potential of 3k Volts was used for characterization purposes for this thesis work. This microscope uses beam of electrons instead of light to image the specimen and to gain information about its structure and composition. The SEM has a large depth of field, which allows large amount of sample to be in focus at a time. It produces images of very high resolution, which means that closely spaced features can also be examined at high magnification. SEM is one of the heavily used instruments in the research field because it gives higher magnification, greater resolution, and large depth of focus with ease of sample observation. Cleaned copper stubs are used to SEM imaging. A 2 mm x 5 mm graphite tape was cut and pasted on copper stub. Small pieces of sample of the dimension less than the graphite tape were cut and mounted on the stub. The edges of the sample are covered with graphite paste. The sample was then coated with gold and placed in the sample holder. The sample holder was then placed in the chamber and then focused to the desired magnification of the top of the sample and the cross-sectional view of the sample. This was repeated for different samples fabricated with different thicknesses of CuPc and thus the cross-sectional view for all of the samples was obtained.

4. Results and Discussion

4.1 Characterization of CdS/CuPc Heterojunction using SEM (Scanning Electron Microscopy)

The SEM images of the sample ITO/CdS/CuPc/PEDOT:PSS are as shown below. Figure 4.1 shows the SEM image (top view) of the sample ITO/CdS/CuPc showing how the CuPc layer is deposited. CuPc was electrodeposited applying a pulse voltage 0V for 4 sec and 120V for 2 sec. This image shows uniform deposition of CuPc on the CdS layer.

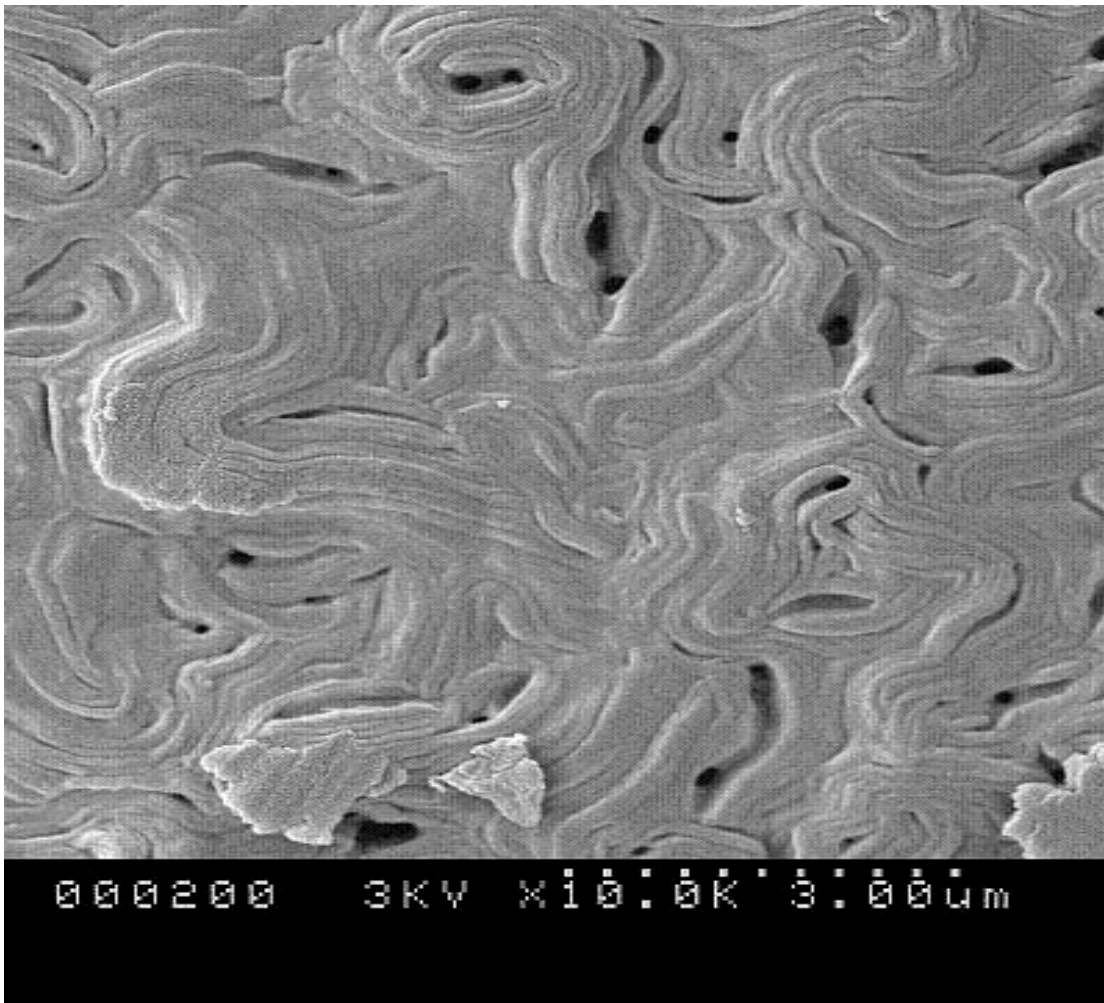


Figure 4.1: Top view of the sample ITO/CdS/CuPc

Figure 4.2 shows the top view of the sample ITO/CdS/CuPc/PEDOT:PSS. The SEM image shows the smooth and Uniform deposition of PEDOT:PSS layer on top acting as a buffer layer for the sample. Fig 4.2 shows the top view of the structure

ITO/CdS/CuPc/PEDOT:PSS. A smooth uniform layer of the PEDOT:PSS can be seen over the CuPc layer.

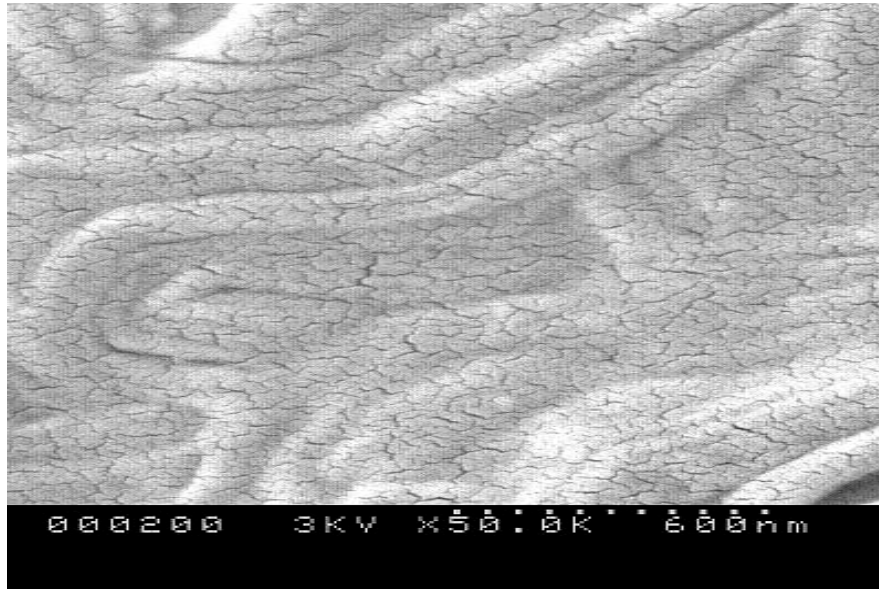


Figure 4.2: Top view of the sample ITO/CdS/CuPc/PEDOT:PSS

Figure 4.3 shows the cross-sectional view of the Structure ITO/CdS/CuPc/PEDOT:PSS. We can see the junction formed between the CdS layer and the CuPc layer in the figure below. The thickness of CdS is 100nm and that of the CuPc layer is 100nm.

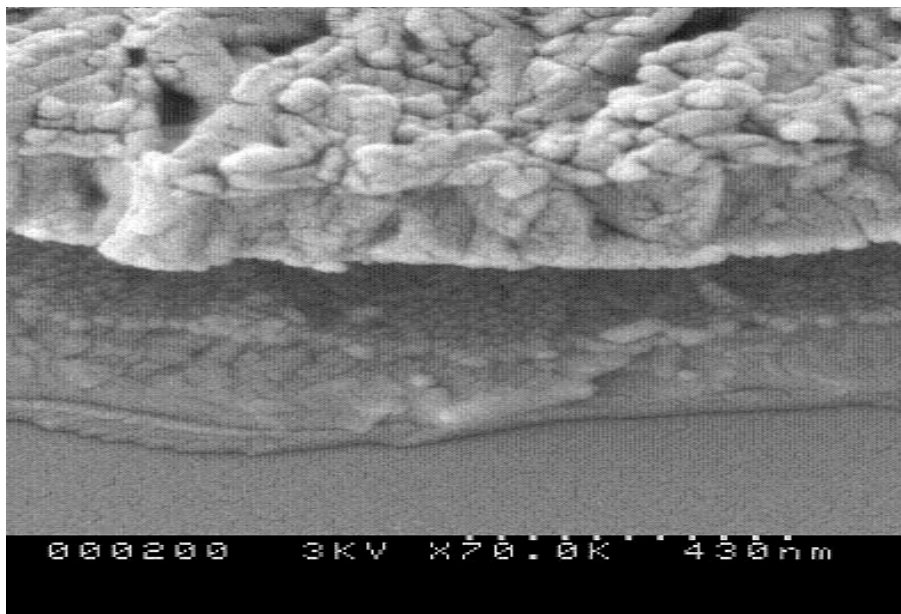


Figure 4.3: Cross sectional view of the sample ITO/CdS/CuPc/PEDOT:PSS

In the Figure 4.4, the thickness of CuPc layer is 300nm and the thickness of CdS layer is 100nm. Thickness of ITO is 150nm. The junction formed between the CdS layer and the CuPc layer can be seen from the SEM image in the Figure 4.4. Also the top and bottom layers of PEDOT:PSS and ITO respectively can also be observed.

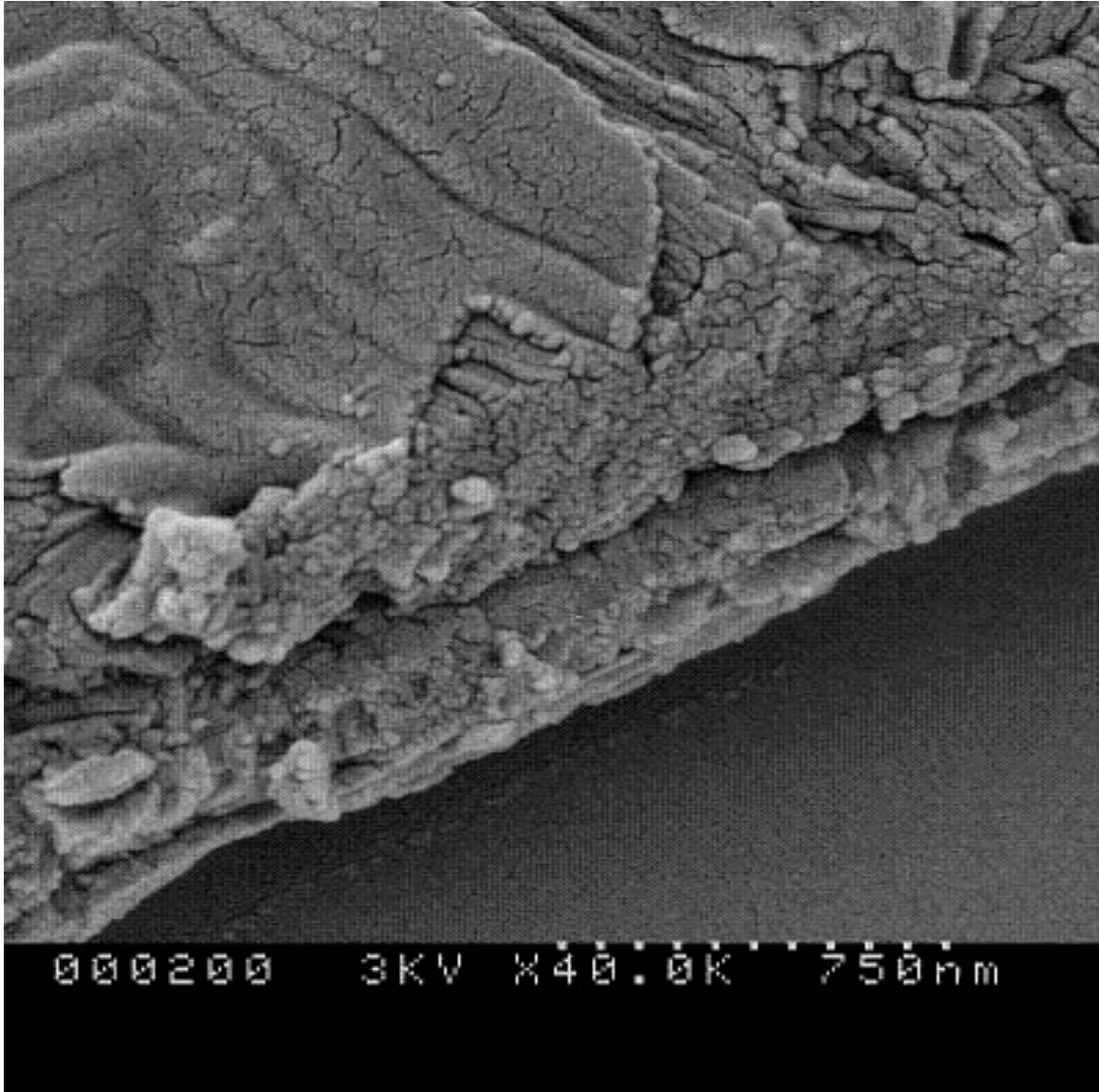


Figure 4.4: Cross sectional view of the sample ITO/CdS/CuPc/PEDOT:PSS

Figure 4.5 shows the image of the CdS/CuPc formed and also the top layer of PEDOT:PSS and the bottom layer of ITO can also be seen. The thickness of CuPc in this case is 700nm and the thickness of CdS is 100nm. The thickness of PEDOT:PSS layer is 200nm and that of ITO is 150nm.

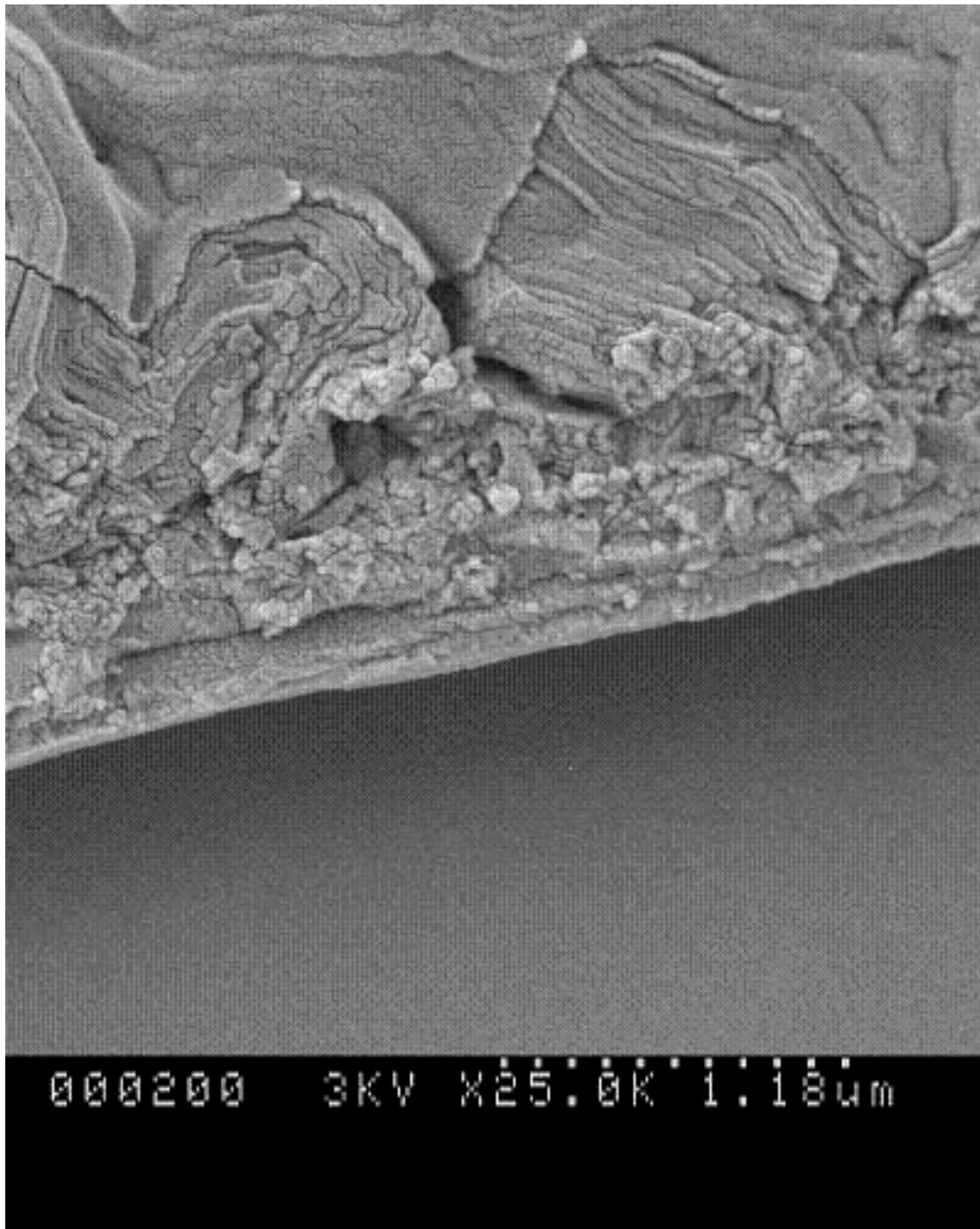


Figure 4.5: Cross sectional view of the sample ITO/CdS/CuPc/PEDOT:PSS

Figure 4.6 shows the cross-sectional view of the sample and we can see the junction formed between CdS/CuPc layers. And the ITO and PEDOT:PSS which are the bottom and top layers respectively can also be seen in the image. Thickness of ITO is 150nm, thickness of CdS is 100nm, and thickness of CuPc is 500nm.

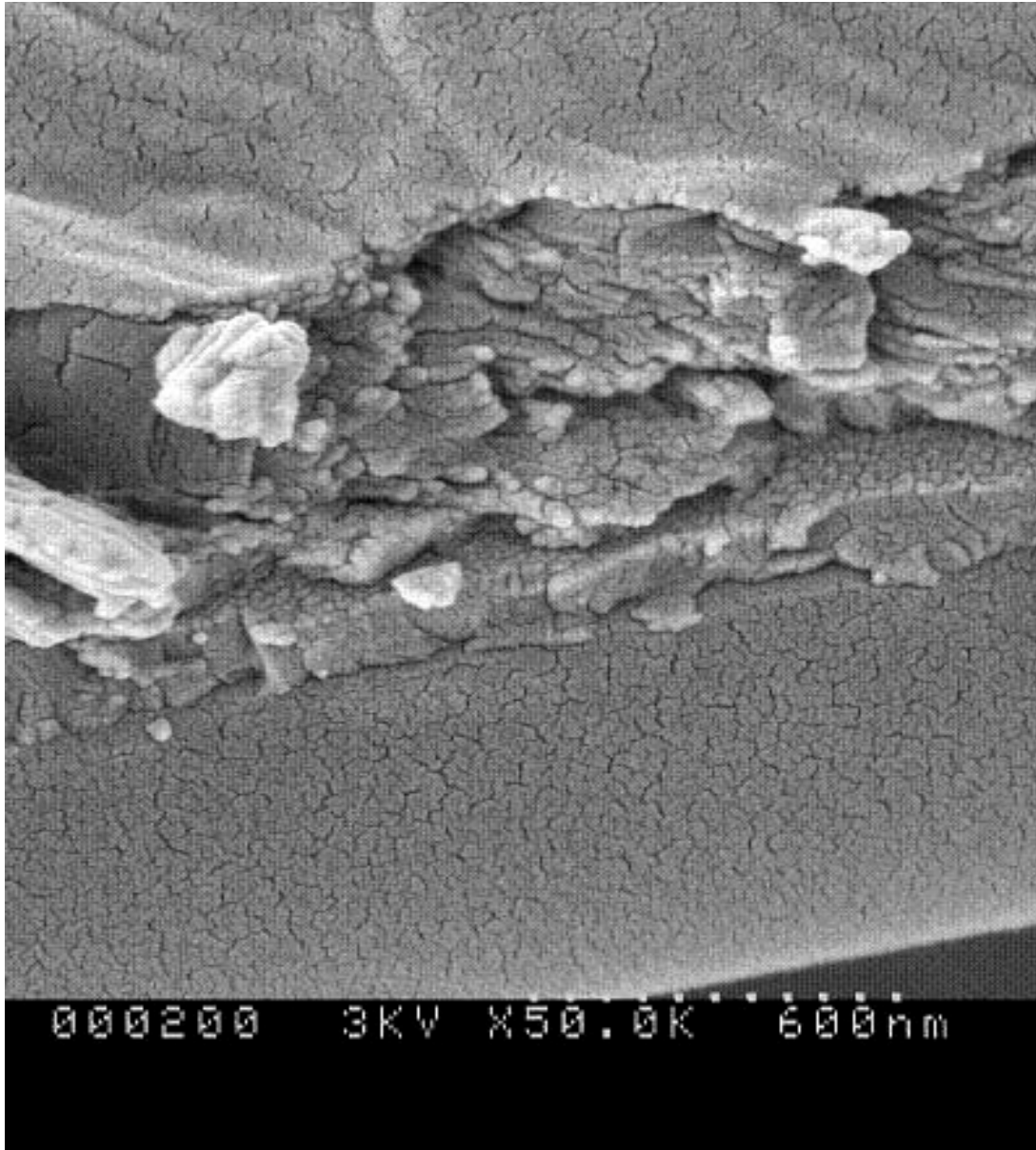


Figure 4.6: Cross sectional view of the sample ITO/CdS/CuPc/PEDOT:PSS

4.2 Characterization of CdS/CuPc Heterojunction using X-Ray Diffraction

The X-ray diffraction patterns obtained for the structure ITO/CdS and ITO/CdS/CuPc are as shown in Figure 4.7 and Figure 4.8 respectively. The intensities and 2-THETA peak values are observed for different thicknesses of CuPc and CdS. The X-ray diffraction pattern both before deposition of CuPc and after the deposition of CuPc on CdS was observed. The Intensity peaks for CdS can be seen at 26.5° and those for ITO

can be seen at 30° , 35° , 37° , 45° , 51° and 60° . The 2-THETA peak for CdS can be ascribed to (002) hexagonal structure of CdS.

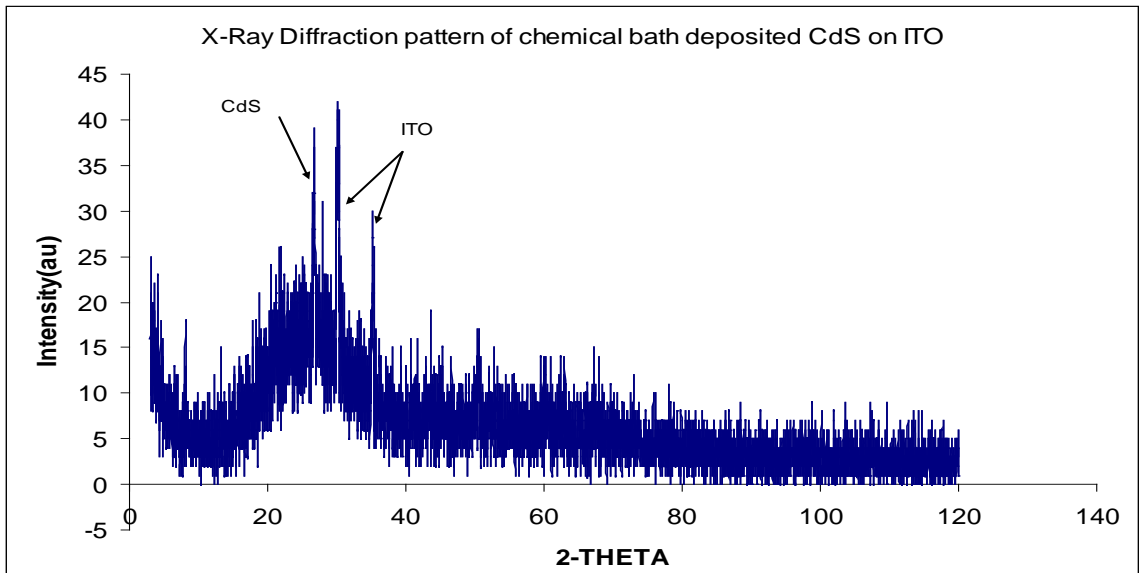


Figure 4.7: X-Ray Diffraction pattern for CdS Deposited on glass/ITO substrate

The maximum Intensity peaks for the ITO/CdS/CuPc structure were found at 26.8° for CdS and for CuPc at 6.8° which also suggests that the CuPc deposited is in alpha-phase. The maximum intensity peak for ITO is observed at 30° .

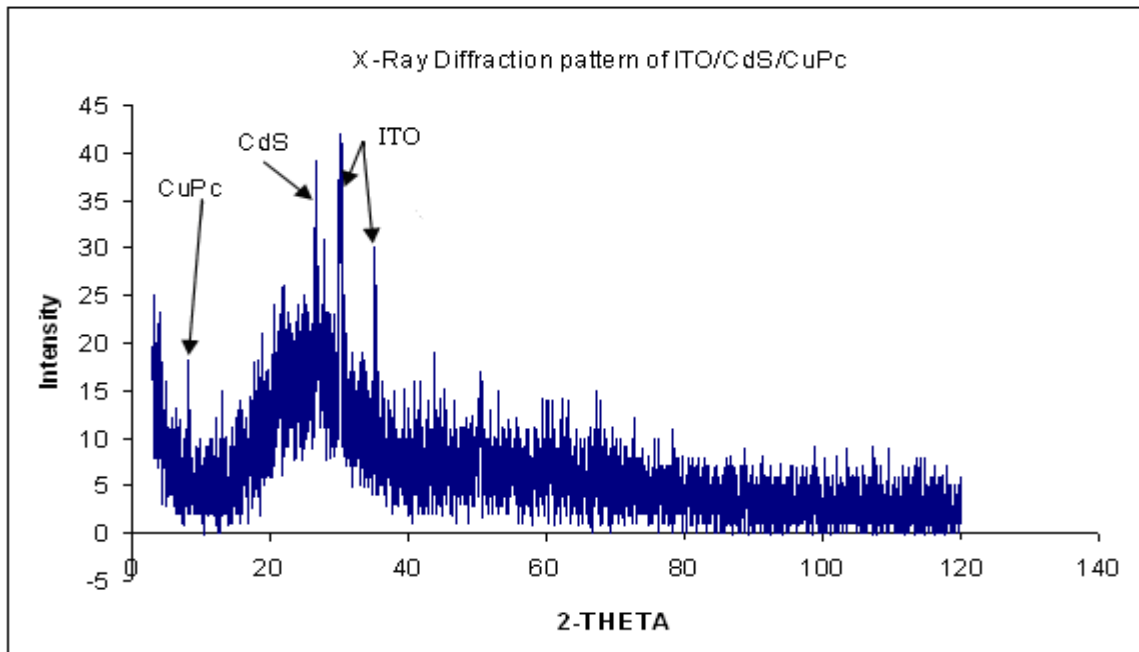


Figure 4.8: X-Ray Diffraction pattern for glass/ITO/CdS/CuPc structure

The 2-THETA values at which the maximum intensity peaks obtained show electrochemically deposited CuPc in α -phase and Chemical bath deposited hexagonal CdS [14]. The difference in both forms is in the tilt angle of the axis of the stack (b axis of unit cell) with respect to the normal of the Phthalocyanine molecular plane and the stacking density of the crystal [18]. The α -phase of the CuPc absorbs more oxygen than the β -phase, and the orientation of CuPc is different in both the phases obtained from both the methods. The peaks of the ITO are observed at 2-Theta values of 30° , 35° , 37° , 45° , 51° and 60° .

4.3 Characterization of CdS/CuPc Heterojunction based on Optical Absorption Spectroscopy

The optical absorption curves for the device fabricated are as shown in figure 4.9. The thickness of CuPc was varied, keeping the thickness of CdS constant and the variation in the optical absorption curves is as shown in the Figure 4.9. Two peaks of absorption as observed in the figure 4.9 correspond to the absorption of electrochemically deposited CuPc. This is because CuPc is acting as the absorber layer in the heterojunction fabricated and the CdS layer acts just like a window layer allowing light to pass through it. The two peak value at 614nm and 692nm correspond to chott Phthalocyanine and monomer Phthalocyanine respectively [22] [19]. As the thickness of CuPc is increased the intensity of the two peaks also increases. The intensity of the peak value at 614nm is more compared to the peak value at 692nm. This indicates that the percentage of Phthalocyanine increases as the thickness of the CuPc increases.

The cutoff wavelength's for CdS and CuPc are approximately around 512nm and 730nm. Thus CdS absorbs the light with wavelength below 512nm and allows the light beyond the cutoff wavelength. CuPc absorbs the light below the 820nm wavelength and allows the light beyond the cutoff wavelength to pass through it. Thus by fabricating a heterojunctions solar cell, the absorption spectrum is increased based on the band gaps of each material. When compared with single layer structures, bilayer or multilayered cells prove to be more efficient in terms of energy conversion. Future work can be focused more on multilayered structures but fabricating these devices will be a challenge and especially with Organic materials since stability is an important criterion for these materials.

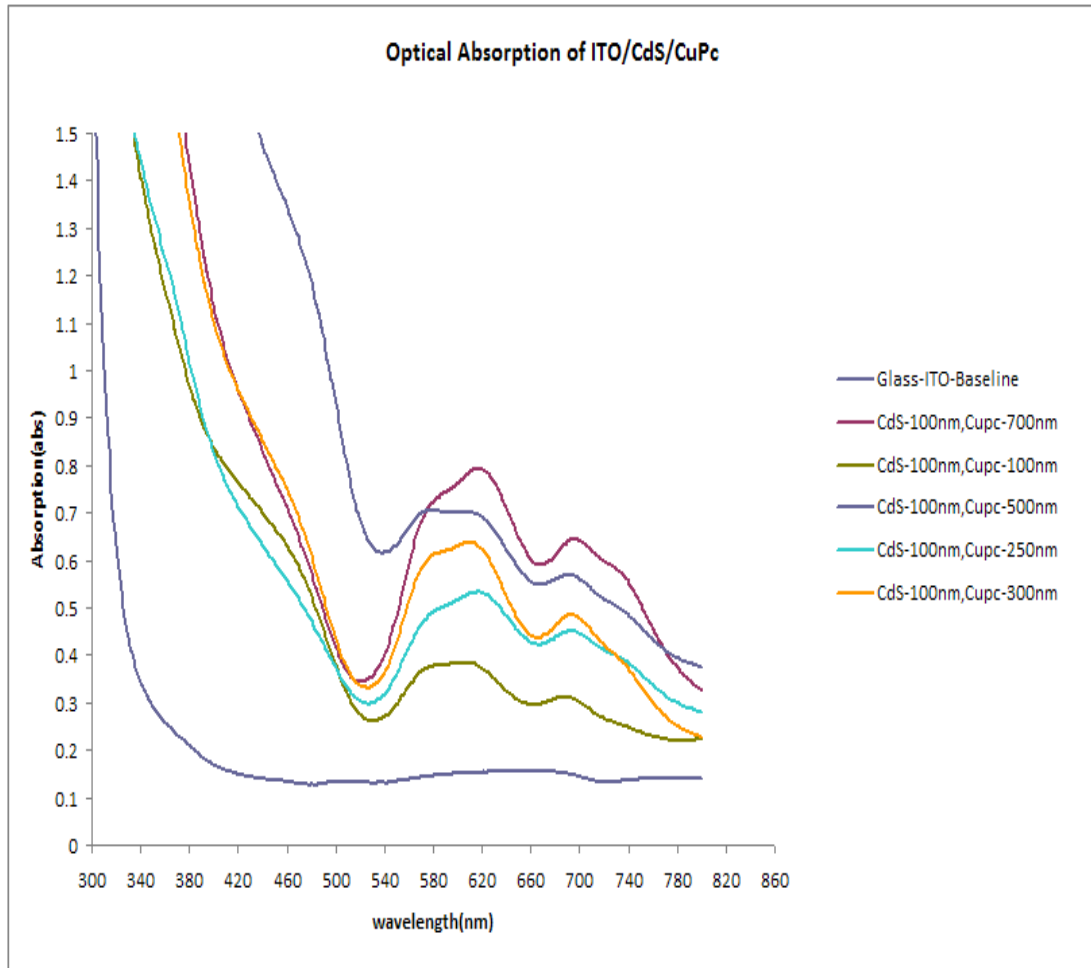


Figure 4.9: Optical absorption curves for different thickness of CuPc on the glass/ITO/CdS/CuPc structure

4.4 Electrical Characterization of CdS/CuPc heterojunction [18]

The diode ideality factor helps in characterizing the electrical properties of the solar cell. The ideal diode equation is given by the equation (1) as shown below,

$$I = I_0 (e^{(qv/kt)} - 1) - I_L \dots\dots\dots (1)$$

where I is the diode current, I_0 is the reverse saturation current, q is the electron charge ($1.6 \times 10^{-19}C$), v is the voltage, k is the Boltzman's constant ($k=1.38 \times 10^{-23} J.K^{-1}$), T is the absolute temperature in Kelvin.

But practically considering the leakage current and series resistance into account, equation (1) can be re-written as follows:

$$I = I_0(e^{(q(v-IR_s)/Akt)} - 1) - I_L \text{ -----(2)}$$

Where A is the diode ideality factor and Rs is the series resistance. The series resistance can be obtained by differentiating equation (2) thus resulting in equation (3) as given below.

$$dV/dI = (AkT/qI_0) e^{-q(V-IR_s)/AkT} + R_s \text{ -----(3)}$$

Neglecting the I₀ term we can write the equation (3) as,

$$dV/dI = AkT/qI + R_s \text{ -----(4)}$$

Using equation (4) we can calculate the series resistance from the J versus I curve when it is forward biased, and thus rising vertically.

$$R_s = dV/dI = (V_2 - V_1) / (I_2 - I_1)$$

After calculating the Series Resistance, we can find the diode ideality factor as follows:

$$\text{Junction voltage (V}_j\text{)} = V - I * R_s$$

$$\text{Current (I}_j\text{)} = I_0 \exp(qV_j / AKT) \text{ -----(5)}$$

Applying natural logarithm on both sides of equation (5) results in equation (6).

$$\ln(I_j) = \ln(I_0) + qV_j/AKT \text{ -----(6)}$$

Therefore slope = 1/AKT, and thus Ideality factor (A) = 1/ slope*KT. Reverse saturation current is given by the y-intercept of the Ln(J)-V curve. For an ideal diode the ideality factor is 1 but practically it is always one because of tunneling effect and the carrier injection between the states.

4.4.1 Electrical characterization of the [ITO / CdS / CuPc / PEDOT:PSS / Au] structure (CdS-Chemical bath deposited, CuPc-Electrochemically deposited)

The energy band diagram for the CuPc and CdS heterojunction is as shown in Figure 4.10. The curves in Figure 4.11 and Figure 4.12 show the plot of the Current density versus the voltage for the CdS/CuPc based heterojunction where CdS is chemical bath deposited and CuPc is electrodeposited. Fig 4.11 shows the maximum open circuit voltage (V_{oc}) and maximum short circuit current density (J_{sc}) obtained for the above structure. The thickness of both CuPc and CdS were varied and the maximum (V_{oc}) obtained was 0.59V and the maximum J_{sc} was 0.7mA/cm². The junction between CuPc (work function 4.3eV) and CdS (work function 4.7eV) is the heterojunction. ITO and CdS layers in the above structure form an ohmic contact and the CuPc and Au also (work

function 5.1eV) form an ohmic contact. A maximum open circuit voltage that can be obtained theoretically (0.59v) is achieved in this work.

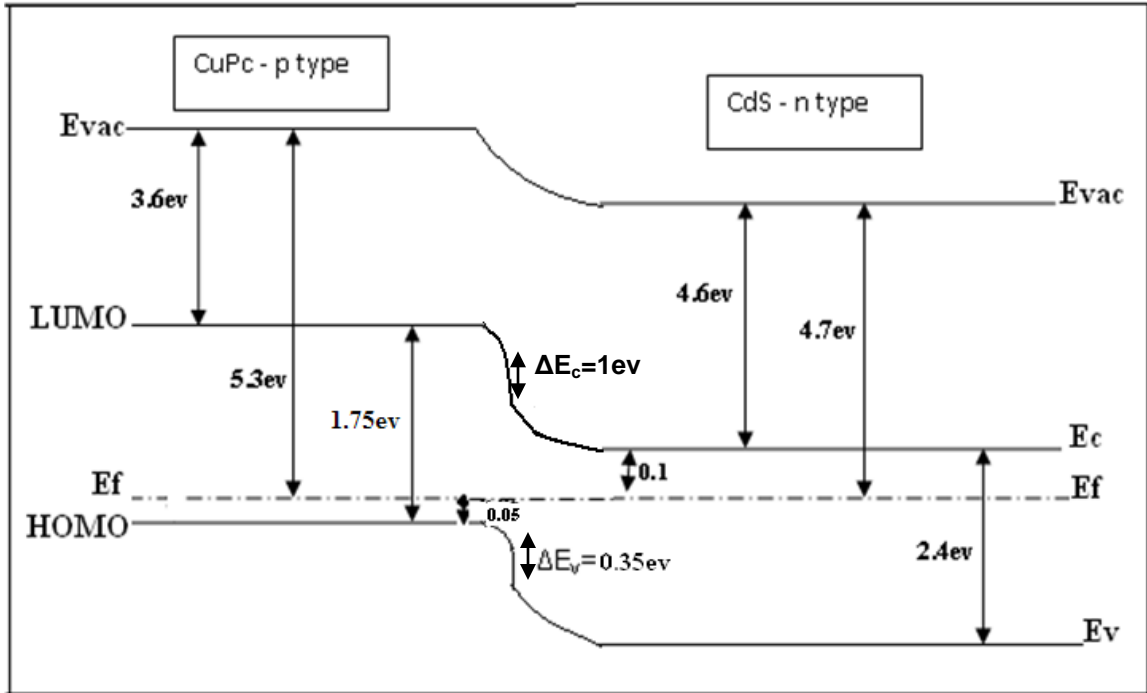


Figure 4.10: Energy band diagram in equilibrium after the junction formation between CdS/CuPc

The CuPc is p-type organic semiconductor with equilibrium Fermi level located at 0.05eV above the valence band (HOMO). CdS is an n-type Inorganic semiconductor with Fermi level located 0.1ev below the conduction band. In this device, the interface between the organic/Inorganic layers is crucial in determining the photovoltaic response. The absorption characteristics of the two layers enhance the utilization of wavelengths of the solar spectrum by the two layers as compared with most of the single layer based solar cells.

Experiments were performed to observe the effect on J-V characteristics of the solar cell by varying the thickness of both CdS and CuPc. Fig 4.13 shows the effect of varying the thicknesses of CuPc layer on open circuit voltage and short circuit current density. The variation of thickness of CdS layer was also experimented but since the CdS layer plays the role of just being the window layer, has a very little impact on open circuit

voltage and short circuit current density. Fig 4.14 shows the J-V curves in the dark conditions and the effect of variation of CuPc layer under the dark conditions.

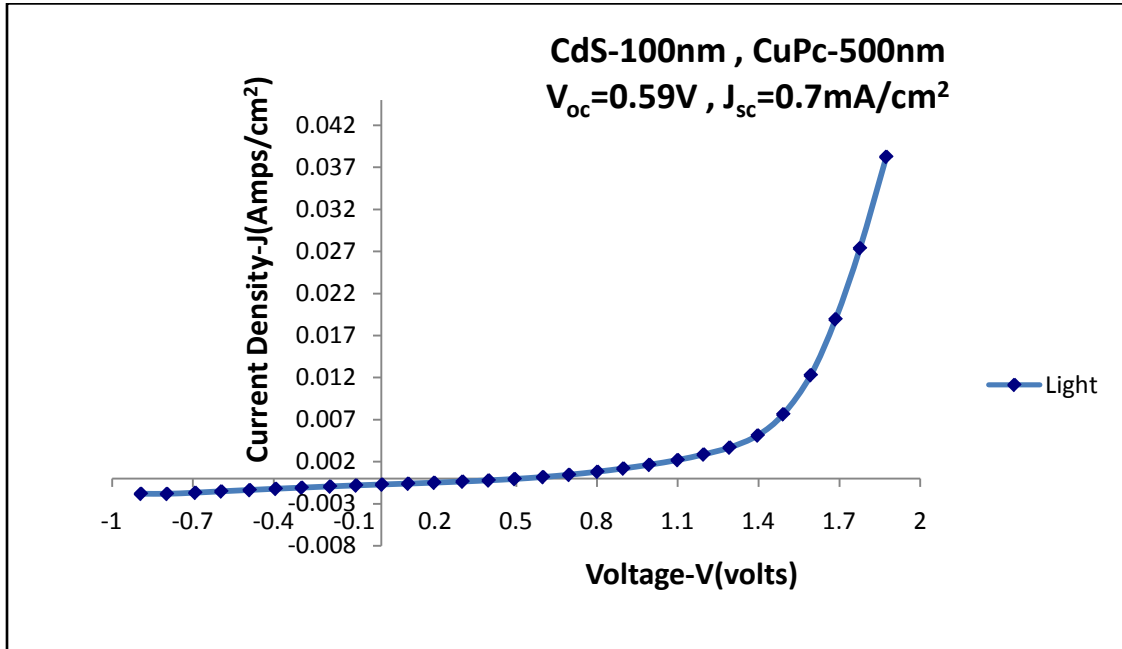


Figure 4.11: J-V curve showing the maximum open circuit voltage and maximum short circuit current density that was obtained for the device fabricated.

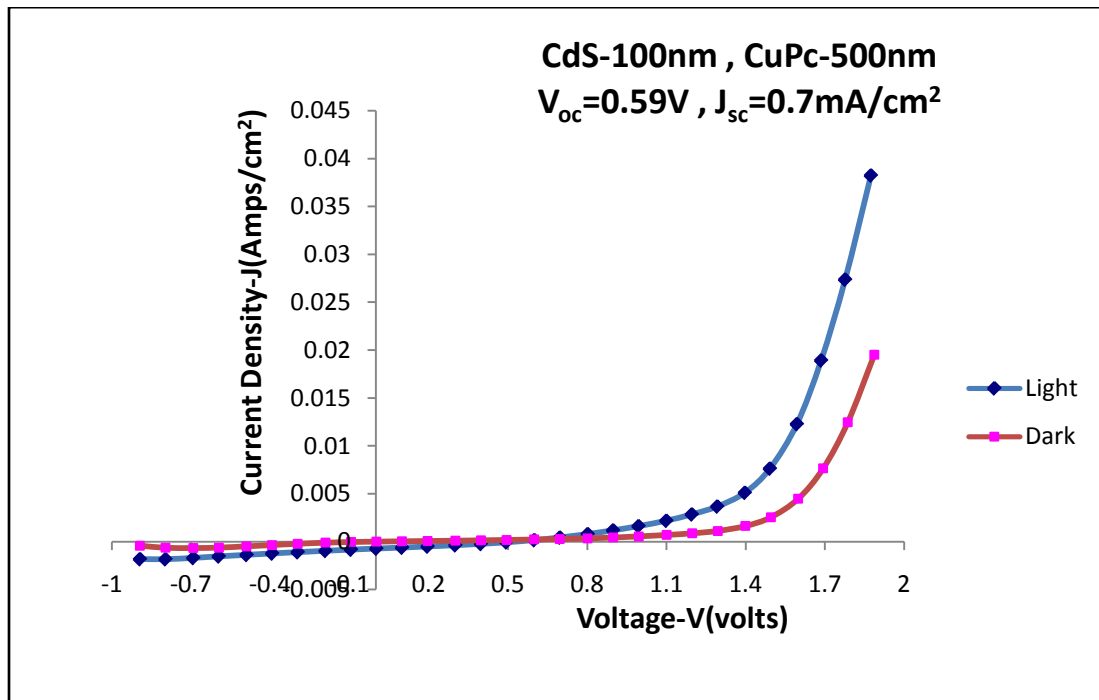


Figure 4.12: J-V curve showing the maximum open circuit voltage and maximum short circuit current density that was obtained along with the dark curve for the device fabricated.

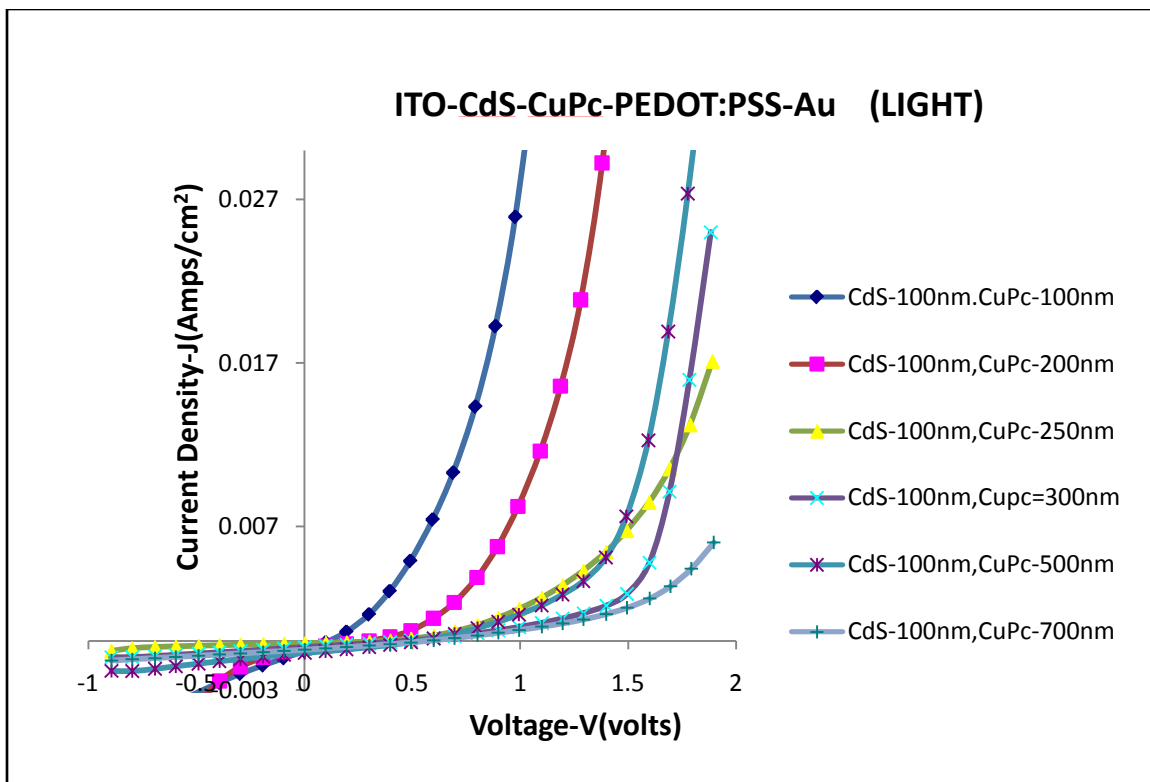


Figure 4.13: J-V curves (light) for different thicknesses of CuPc showing the effect on open circuit voltage and short circuit density

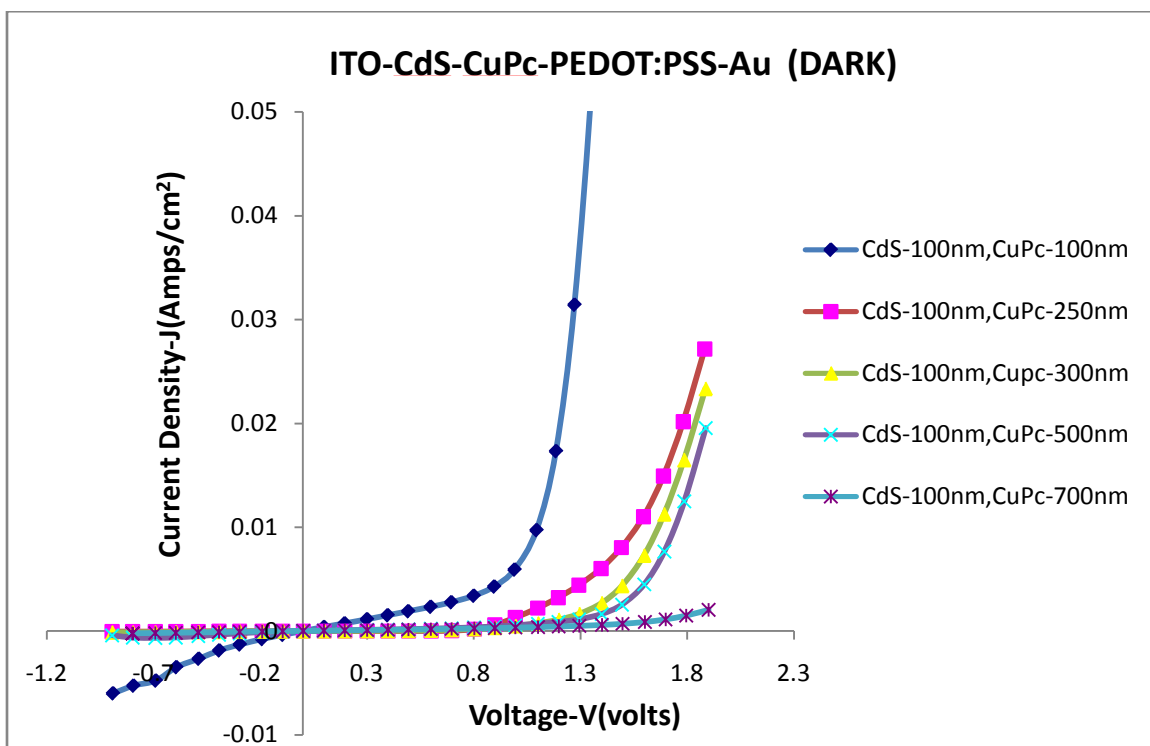


Figure 4.14: J-V curves (dark) for different thicknesses of CuPc

Figure 4.15 shows the short circuit current densities and open circuit voltages for different thicknesses of CuPc, keeping the thickness of CdS as 100nm. The maximum open circuit voltage that can be obtained for this structure was 0.59v and thus maximum theoretical value of the open circuit voltage has been obtained. Although the maximum short circuit current density obtained is $0.7\text{mA}/\text{cm}^2$, there is chance for improvement and higher values can be obtained by tailoring the deposition technique of CdS. The J-V curves from Figure 4.16 through Figure 4.27 show the various curves for different thicknesses of CuPc along with $\ln(J)$ Vs V plots.

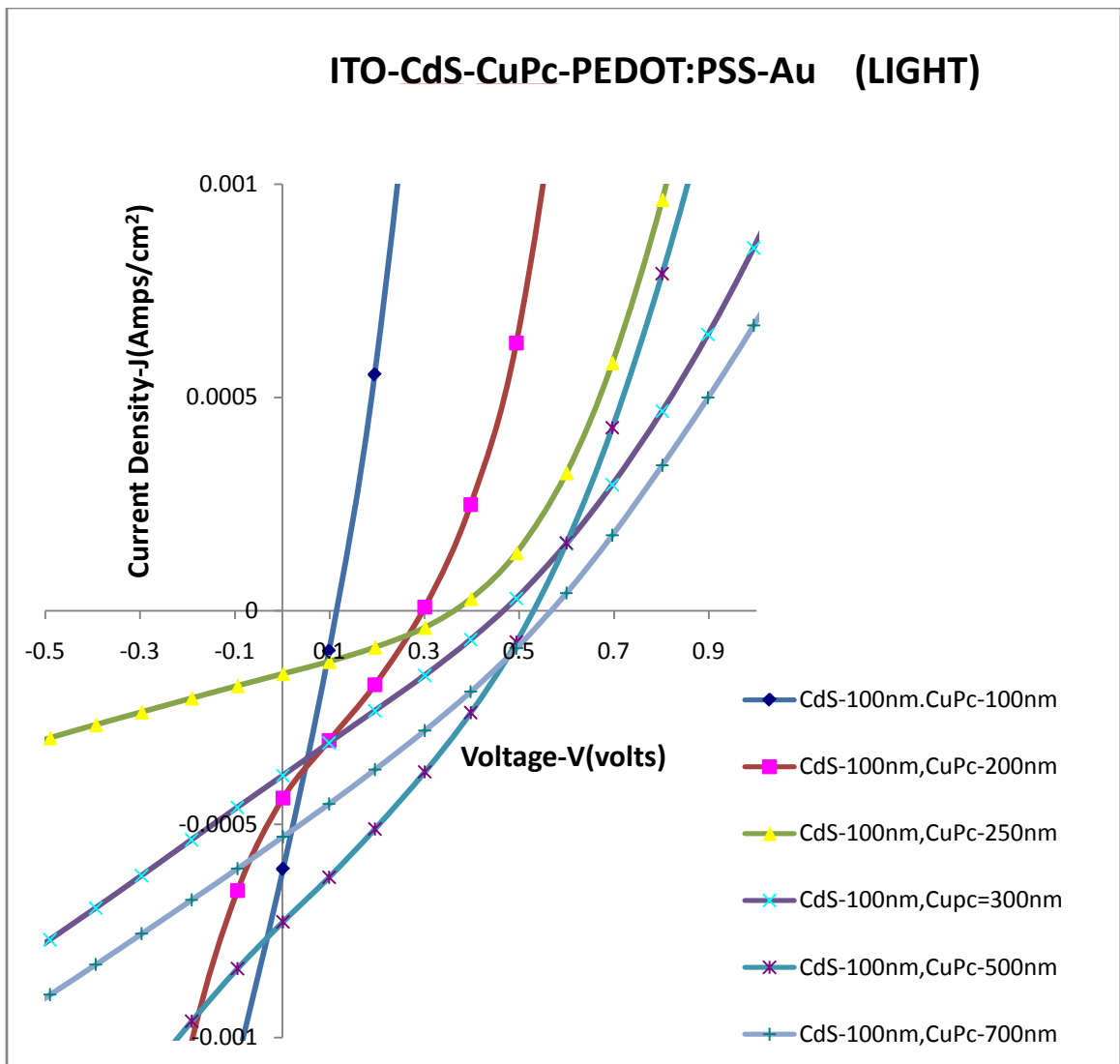


Figure 4.15: J-V curves (light) for different thicknesses of CuPc showing the open circuit voltage and short circuit density

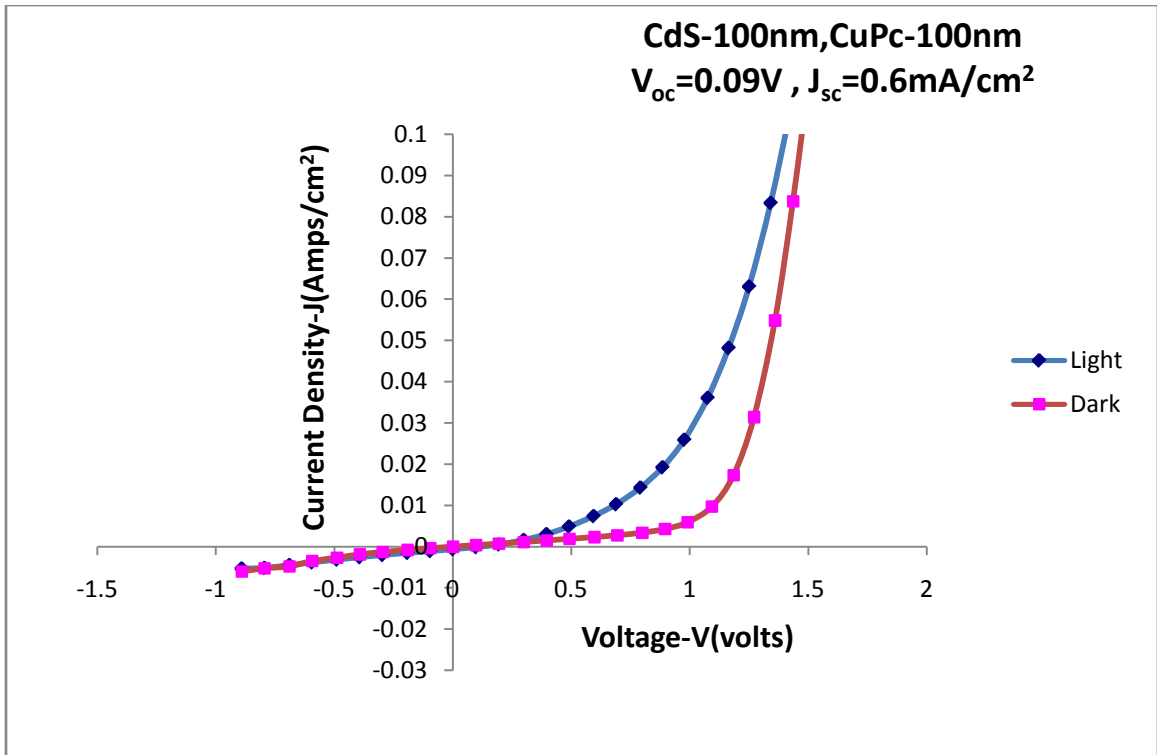


Figure 4.16: J-V curve (light and dark) when thickness of CuPc is 100nm and CdS is 100nm

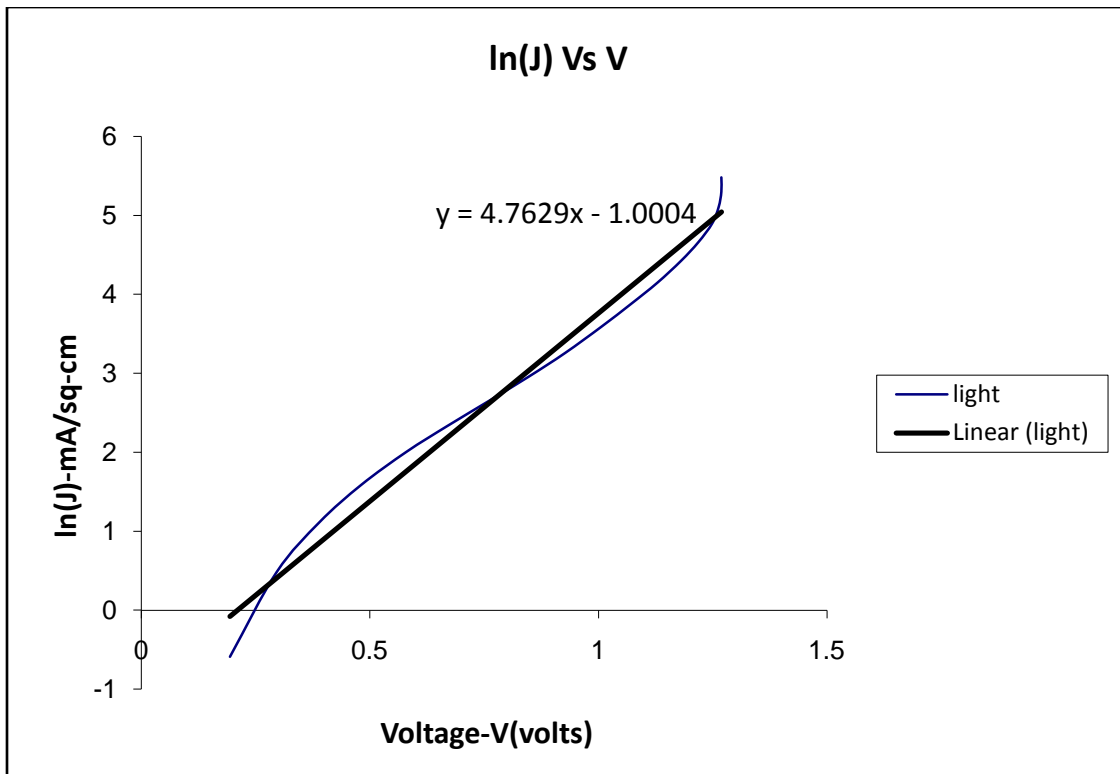


Figure 4.17: ln(J) Vs V curve in light (CuPc-100nm , CdS-100nm)

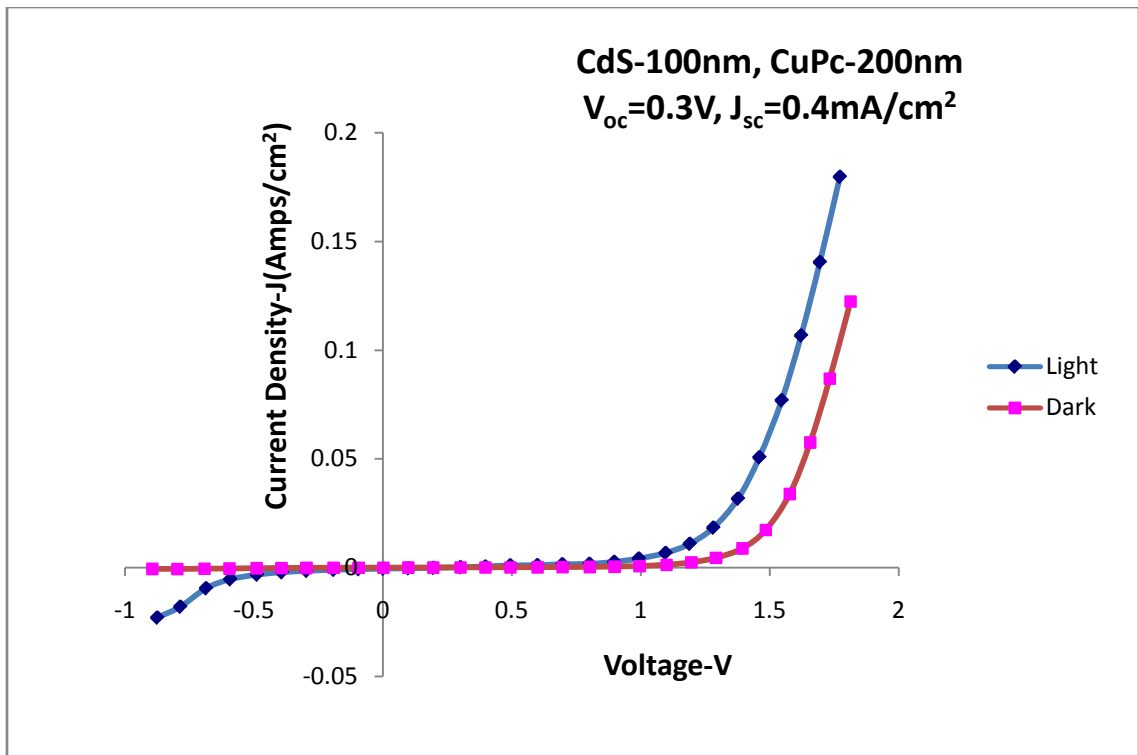


Figure 4.18: J-V curve (light and dark) when thickness of CuPc is 200nm and CdS is 100nm

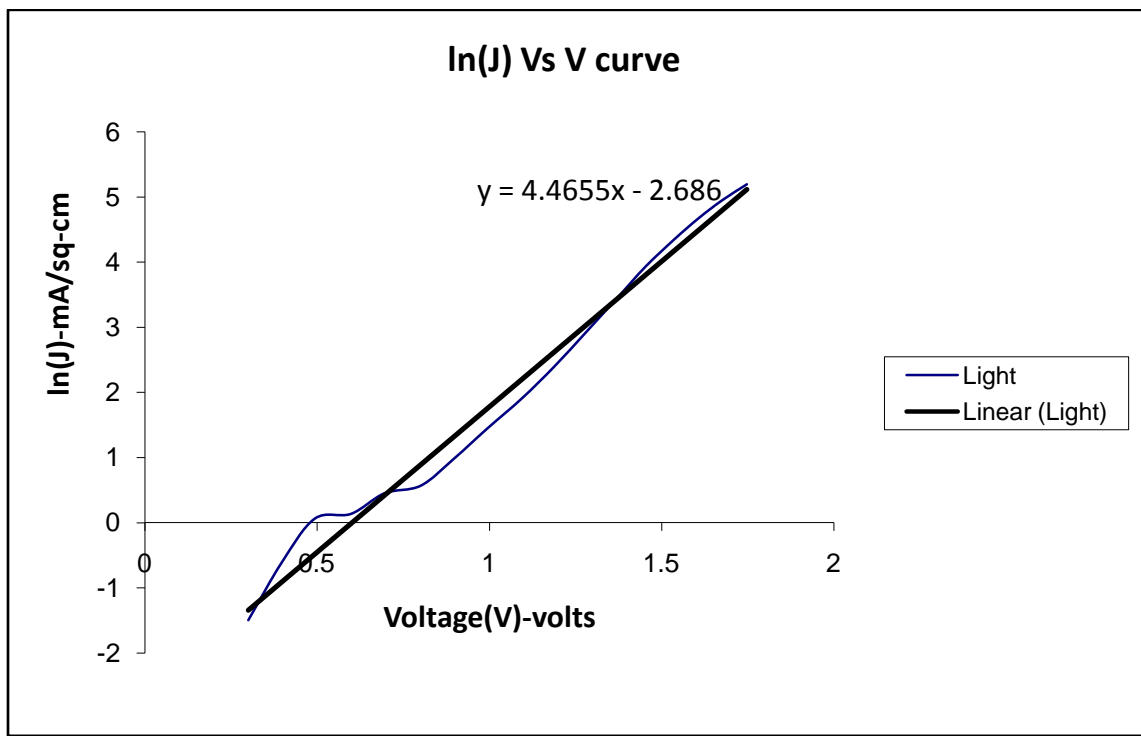


Figure 4.19: ln(J) Vs V curve in light (CuPc-200nm , CdS-100nm)

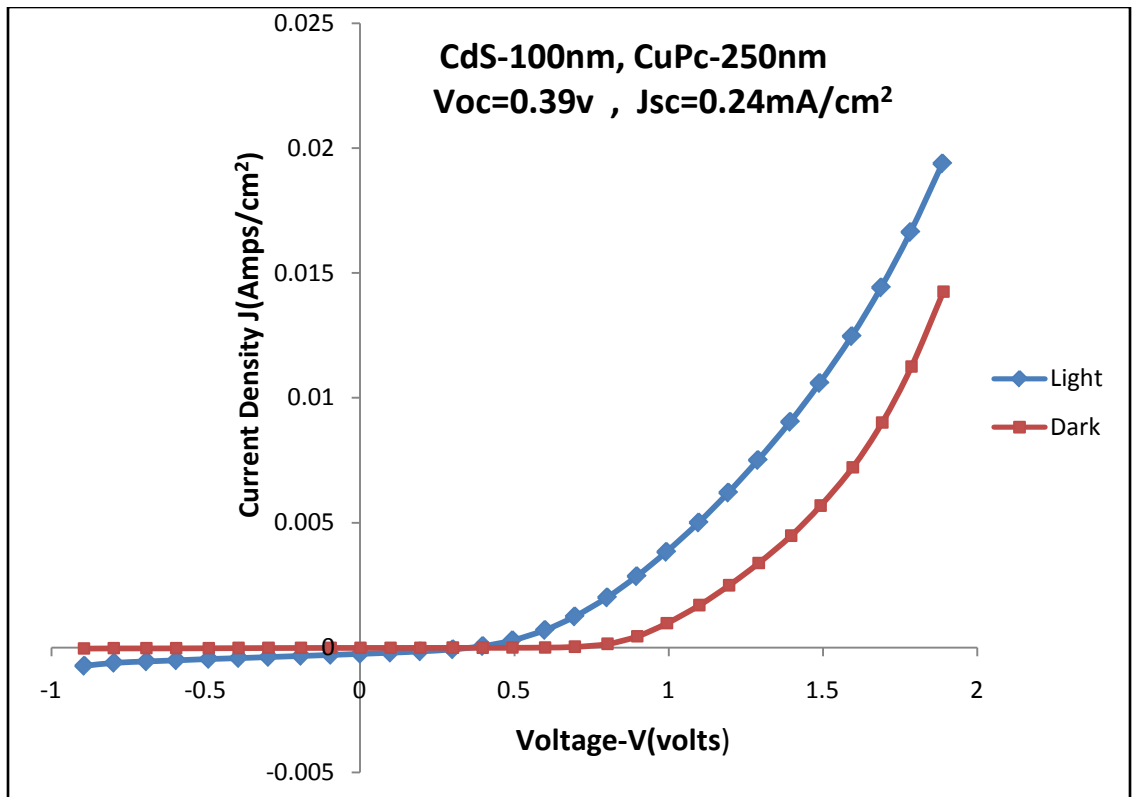


Figure 4.20: J-V curve (light and dark) when thickness of CuPc is 250nm and CdS is 100nm

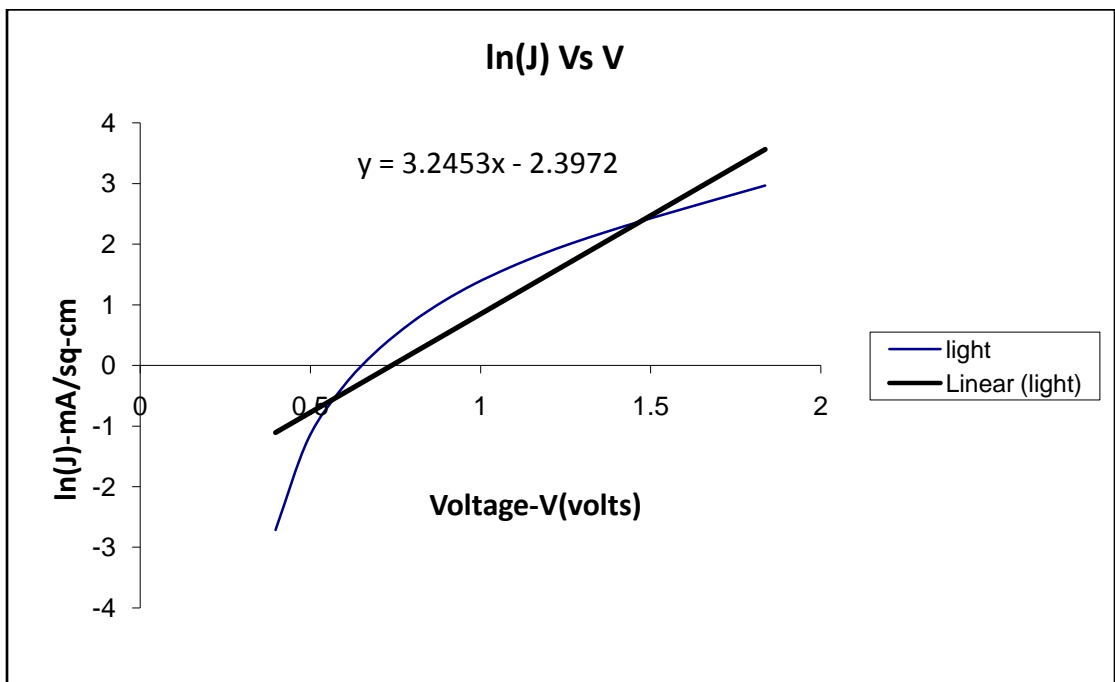


Figure 4.21: ln(J) Vs V curve in light (CuPc-250nm , CdS-100nm)

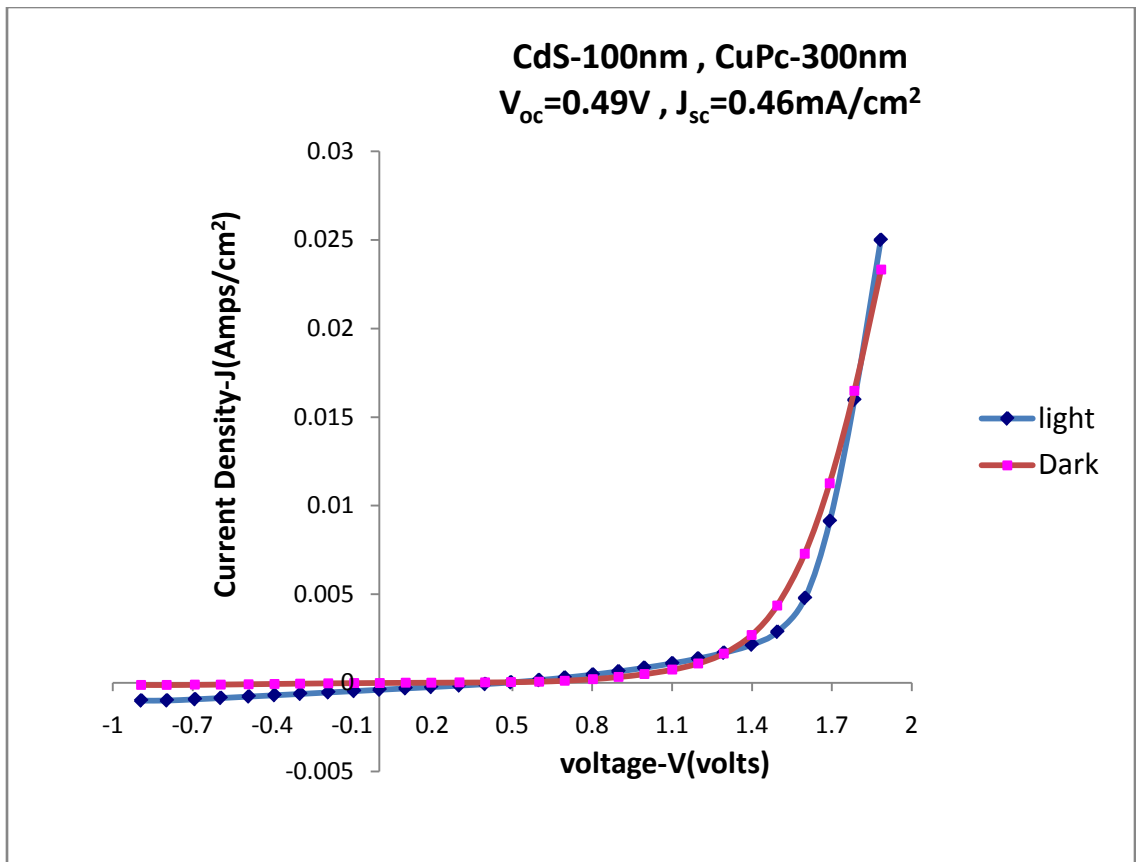


Figure 4.22: J-V curve (light and dark) when thickness of CuPc is 300nm and CdS is 100nm

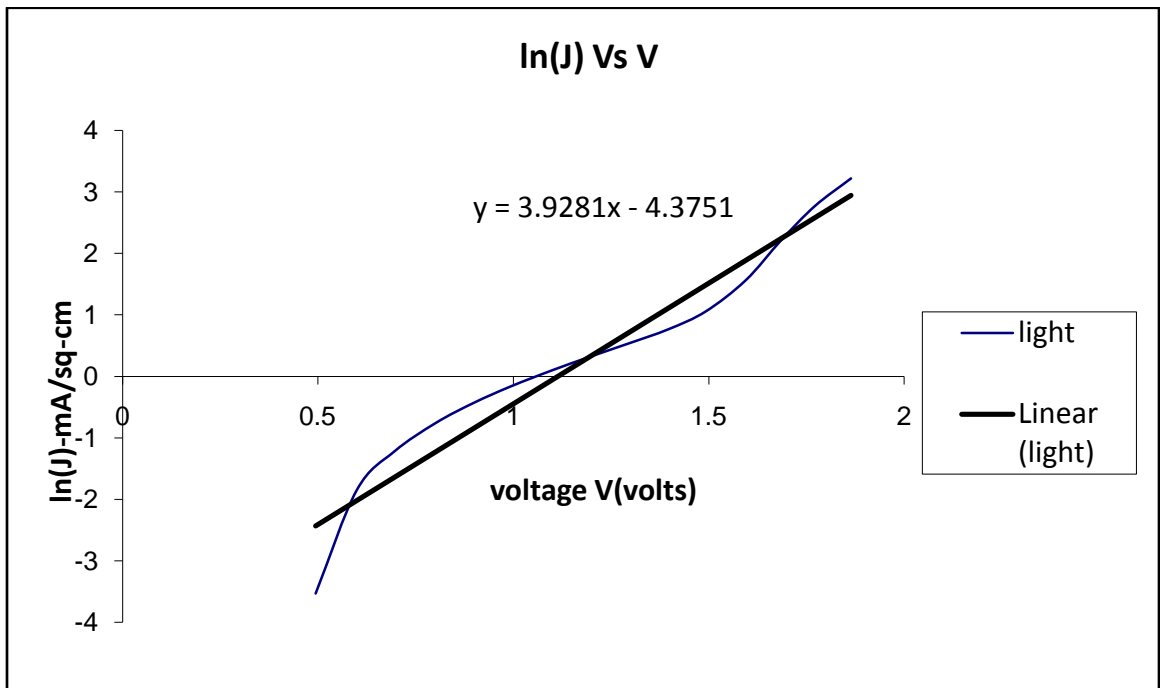


Figure 4.23: ln(J) Vs V curve in light (CuPc-300nm , CdS-100nm)

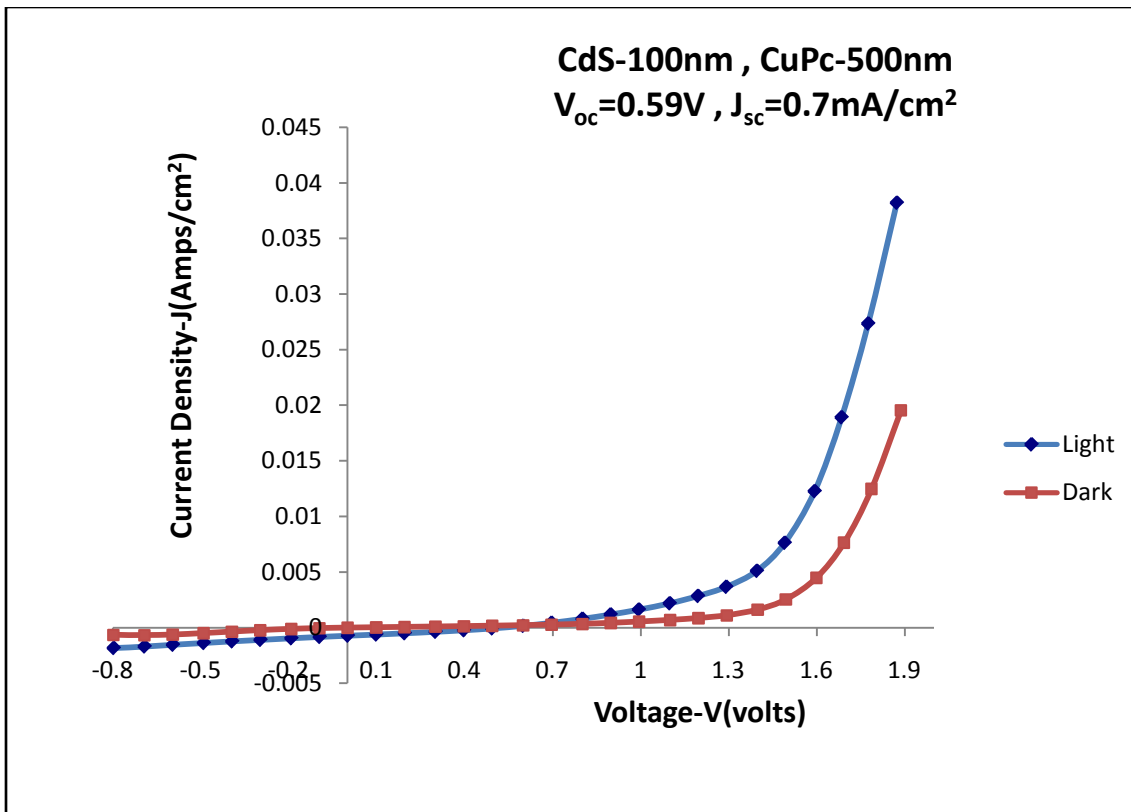


Figure 4.24: J-V curve (light and dark) when thickness of CuPc is 500nm and CdS is 100nm

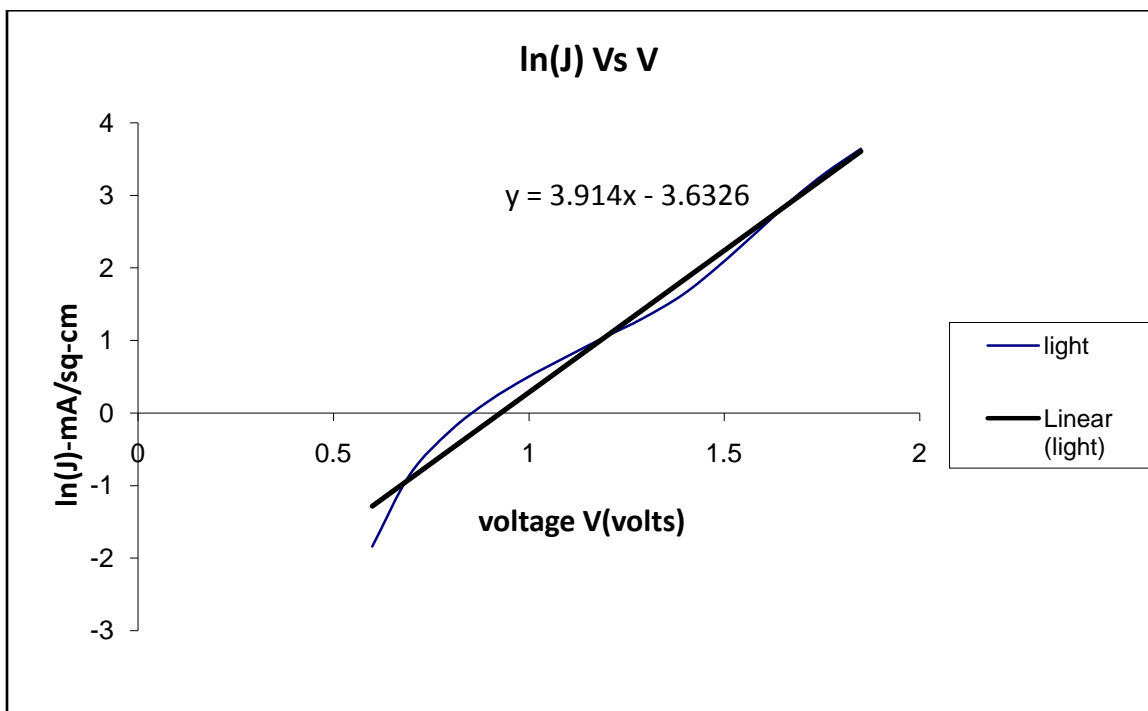


Figure 4.25: ln(J) Vs V curve in light (CuPc-500nm , CdS-100nm)

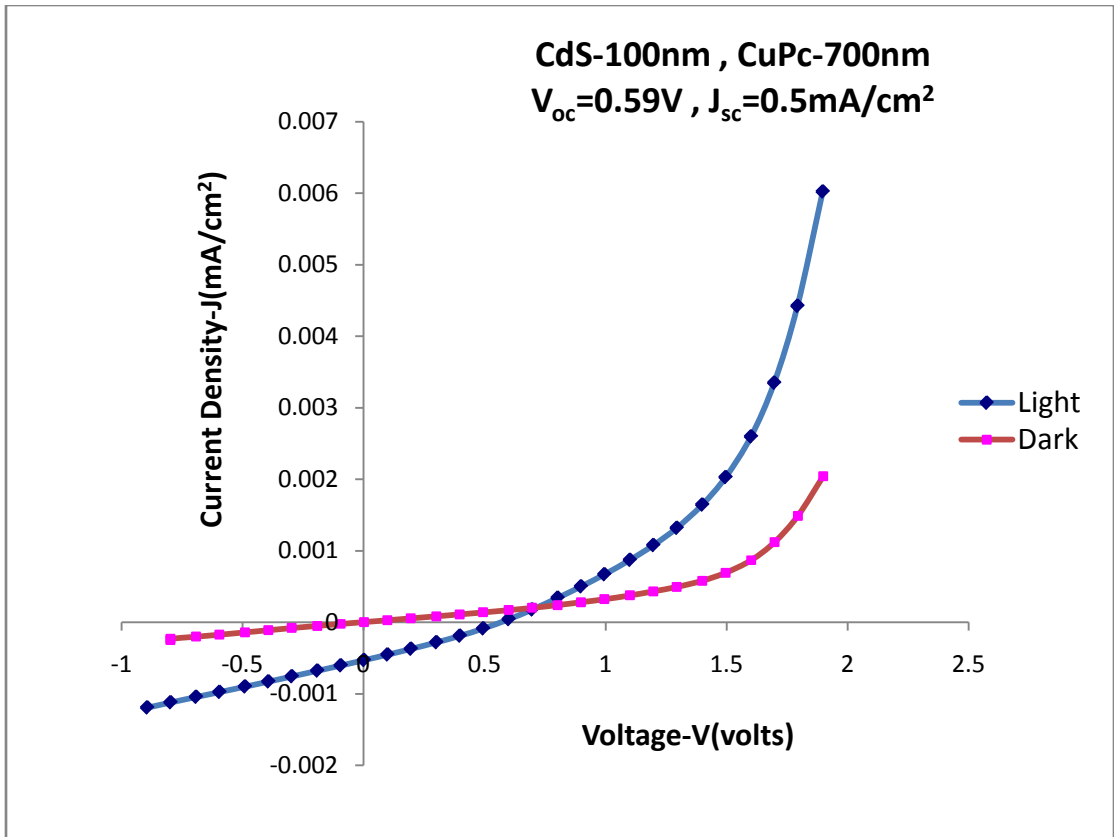


Figure 4.26: J-V curve (light and dark) when thickness of CuPc is 700nm and CdS is 100nm

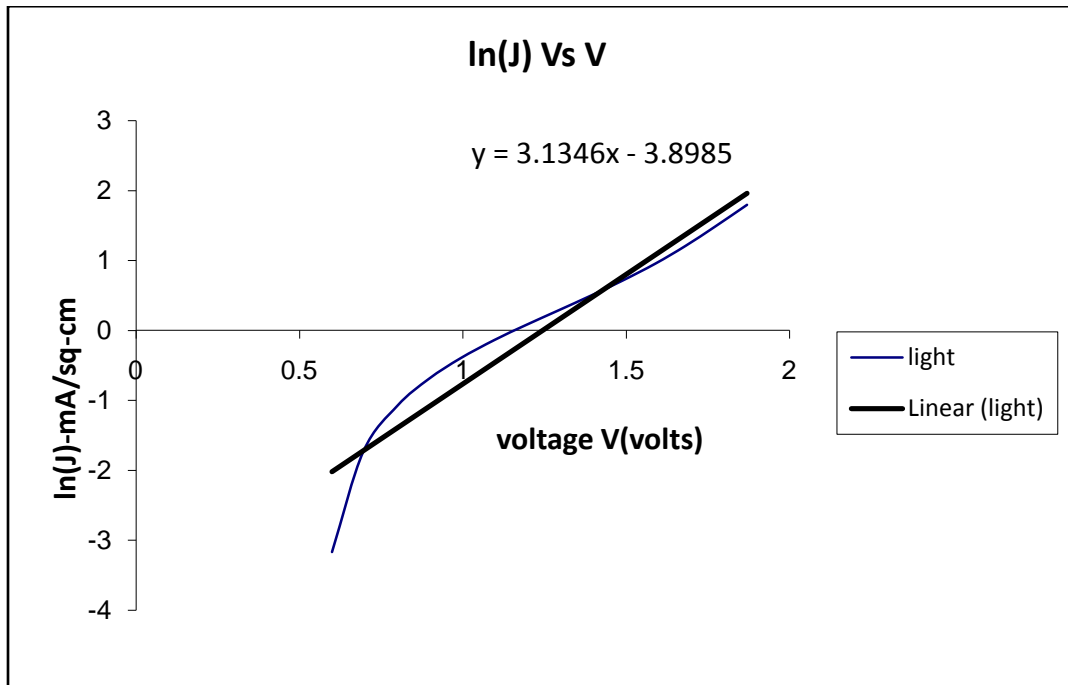


Figure 4.27: ln(J) Vs V curve in light (CuPc-700nm , CdS-100nm)

The various parameters to characterize the electrical properties of the fabricated heterojunction solar cell are as tabulated in the Table 1 and Table 2, for dark and light conditions respectively. The characterization is done for different thicknesses of CuPc, since CuPc is acting as the donor material and is majorly responsible for photoconductivity of the designed structure. The CdS layer acts as acceptor layer and is like a window layer allowing the light to pass through it and reach CuPc layer. Thus CdS helps in increasing the absorption spectrum and thus increasing the energy conversion efficiency. Thickness of CdS was also varied and experimented.

Table 1: The electrical characteristics of the ITO/CdS/CuPc/Au with varying CuPc thickness, for Light curves (CdS-Chemical bath deposition, CuPc-Electrodeposited)

Thickness of CdS(nm)	Thickness of CuPc(nm)	V_{oc} (mV)	J_{sc} (mA/cm ²)	Series Resistance R_s (Ω /cm ²)	J_o (mA/cm ²)	Ideality Factor
100	100	0.09	0.60	1.9249	0.367	8.1103
100	200	0.30	0.40	1.9756	0.068	8.6460
100	250	0.39	0.24	37.7159	0.090	11.8760
100	300	0.49	0.46	10.9794	0.012	9.8299
100	500	0.59	0.70	18.9698	0.026	9.8648
100	700	0.59	0.50	65.2250	0.033	12.3183

Table 2: The electrical characteristics of the ITO/CdS/CuPc/Au with varying CuPc thickness, for Dark curves (CdS-Chemical bath deposition, CuPc-Electrodeposited)

Thickness of CdS(nm)	Thickness of CuPc (nm)	Series Resistance R_s (Ω /cm ²)	J_o (mA/cm ²)	Ideality Factor
100	100	1.8006	0.096	8.2987
100	200	2.2720	0.010	7.8125
100	250	34.4450	0.002	7.3281
100	300	14.6792	0.003	8.0134
100	500	14.2241	0.018	10.9075
100	700	189.0850	0.025	16.2628

J_0 denotes the reverse saturation current in Table1 and Table2. Table 3 shows the comparison of the open circuit voltages and short circuit current densities for two different contacts gold and nickel respectively. As we can see from the table, there is much difference in the currents and voltages when the two contacts are used separately on the device fabricated because the work function of the two metals compared is almost the same. The work functions of Gold and Nickel being 5.15 and 5.1 respectively. Thus not making a much difference on the results obtained from the structure fabricated. The performance of the device with Gold and Nickel contacts was compared for different thicknesses of CuPc and CdS as shown in Table3.

Table 3: Comparison of Gold and Nickel on ITO/CdS/CuPc/PEDOT:PSS structure

CdS deposition (Chemical Bath Deposition)	CuPc deposition (Electrochemical Deposition)	Contact(Gold)		Contact(nickel)	
		V_{oc} (V)	J_{sc} (mA/cm ²)	V_{oc} (V)	J_{sc} (mA/cm ²)
60nm	300nm Pulse (0V-120V)	0.39	0.33	0.39	0.27
60nm	300nm Pulse (0V-120V)	0.39	0.32	0.39	0.29
100nm	300nm 120V	0.49	0.18	0.39	0.31
100nm	300nm 120V	0.49	0.34	0.39	0.29

The difference on the performance of the device when using these two contacts Gold and Nickel can be observed from the J-V curves in Figure 4.28 and Figure 4.29 respectively. The difference can be observed when negative bias is applied to the device. We can see that there is more shunt resistance when Nickel is used when compared with that of Gold. This could be because Gold has higher density than Nickel and it pierces through CuPc to a greater extent than Nickel. So the free charge carriers generated have to travel a lesser distance. When compared between these two contacts we would prefer

Nickel because it is much cheaper and there is not a significant difference in the performance of the device using either of the contacts.

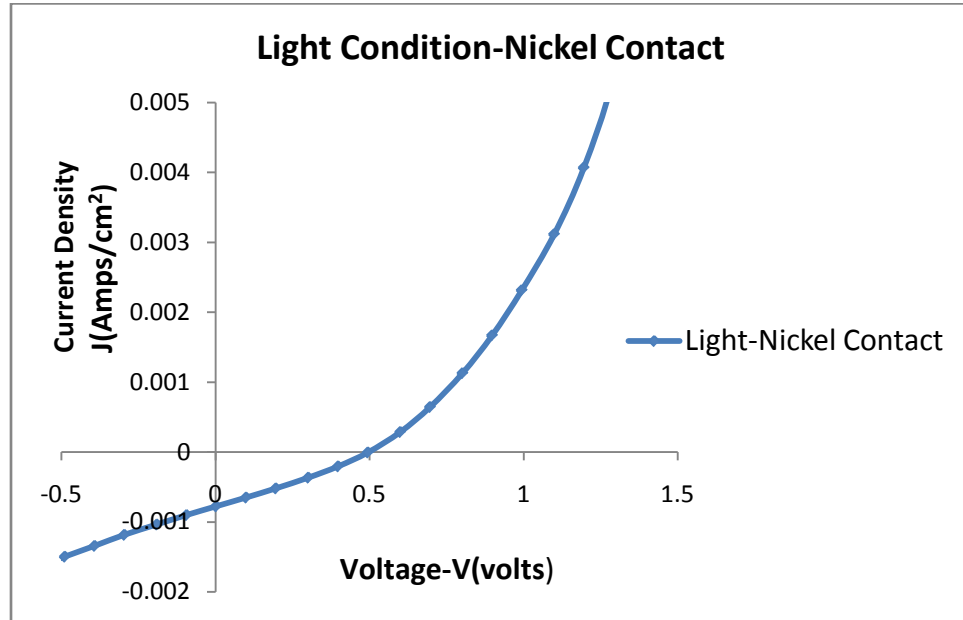


Figure 4.28: J-V curve (light) when thickness of CuPc is 300nm and CdS is 100nm

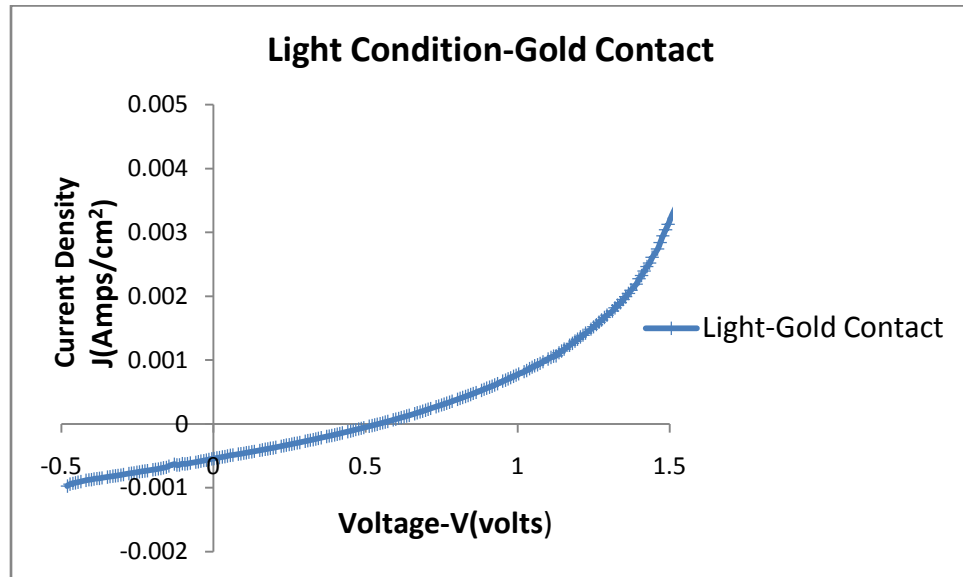


Figure 4.29: J-V curve (light) when thickness of CuPc is 300nm and CdS is 100nm

The Figure 4.30 shows that as the thickness increases the V_{oc} increases and reaches a saturation point. The J_{sc} increases till the CuPc thickness is about 500nm and then again starts decreasing. Increase in V_{oc} with thickness is attributed to reduction in

shorting and shunting paths across the CdS-CuPc junction. For the CuPc thickness ranging from 100nm to 700nm, there is an increase in J_{sc} due to increase in absorption of light and decreases after 500nm because the excitons created in the CuPc will not be able to reach the electrode. Beyond the exciton diffusion length, the excitons contributing to the current is very low. Increase in J_{sc} for thickness higher than 230nm could be due to the generation of extra excitons over powering the effect of exciton diffusion length limitation.

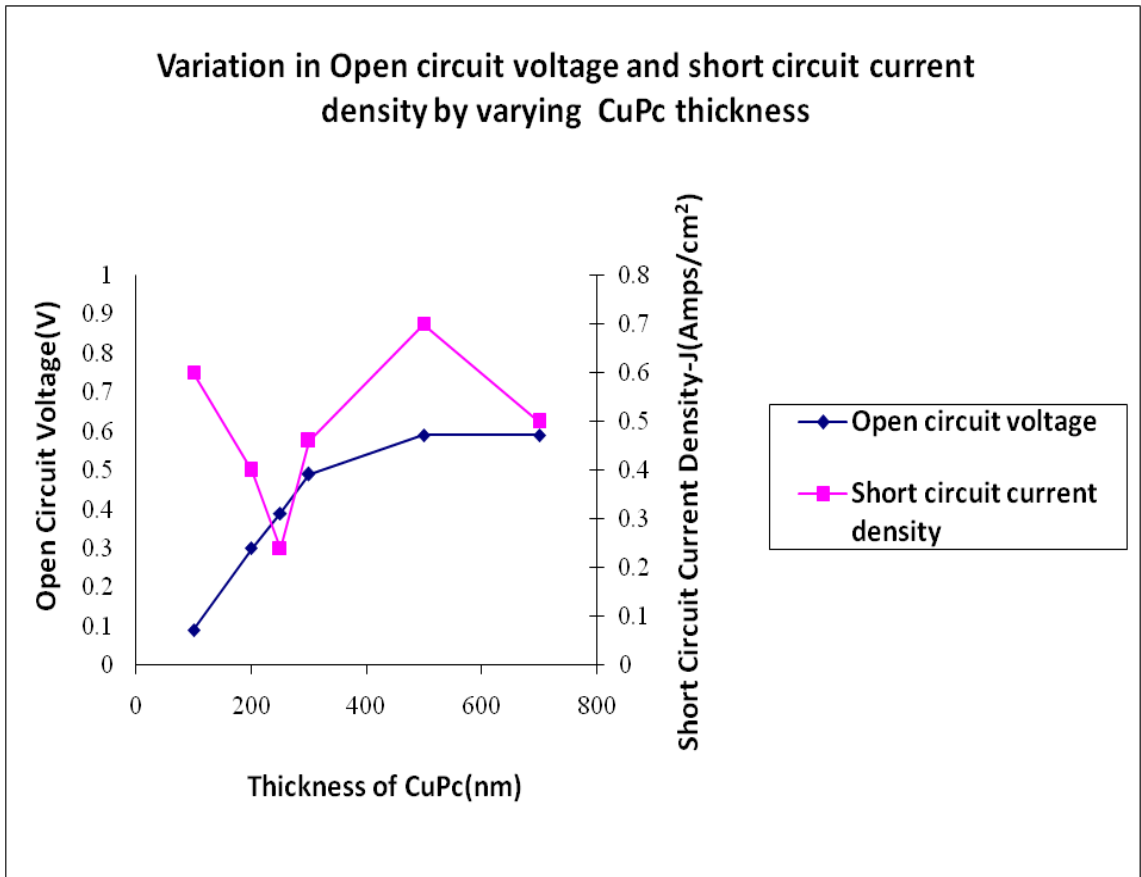


Figure 4.30: The effect of varying the thickness of CuPc on the open circuit voltage and short circuit current density

Electrochemical deposition of CdS instead of Chemical bath deposition was also experimented to see the effect on the currents and voltages in the fabrication of ITO/CdS/CuPc/Au solar cell structure. The only factor that could have been improved by altering the CdS deposition technique was the photocurrent because the maximum theoretically possible photo voltage has already been achieved by chemical bath deposition of CdS. There was not much improvement in the currents by altering the CdS

deposition technique. The photocurrents were slightly less when CdS was electrochemically deposited when compared with the results for Chemical bath deposited CdS for the fabricated solar cell.

CdS layer can be deposited by various techniques like electrochemical deposition, chemical bath deposition, closed space sublimation, but, the chemical bath deposition technique is preferred because CBD makes a very compact film that covers perfectly the ITO layer at the bottom of the device on which CdS is deposited [23].

5. Conclusion & Suggestions

The Heterojunction solar cells with ITO/CdS/CuPc/PEDOT:PSS/Au are fabricated and characterized in this work. The effect of variation of CuPc thickness and CdS thickness on the electrical characteristics of the device is also studied. PEDOT:PSS which acts as buffer layer also plays an important role in improving the performance of the devices fabricated. Open circuit voltage of 0.59V has been achieved in this work. Gold and Nickel were used as contacts for the device fabricated. Both yielded almost the same results since their work functions are very close. The maximum short circuit current density obtained for this device was $0.7\text{mA}/\text{cm}^2$. When compared with solar cells based on single layer, bi-layer or multi layered based solar cells prove to yield better results in terms of photocurrents and efficiency.

There is lot of scope for improvement of the efficiency of the solar cells based on bi-layered solar cells. CuPc form needle like structures when electrodeposited, thus future work can be focused on making CdS/CuPc heterojunction nanowires in AAO templates, thus, attaining better photovoltaic response.

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