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SCHOTTKY DIODES FROM CADMIUM SULFIDE (CdS) NANOWIRES DEPOSITED IN POROUS ALUMINA TEMPLATES

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This work aims to study the variation in electrical and optical properties of nanoscale Schottky diodes by varying their dimensions in the nanoscale. Experimental conditions for fabricating porous alumina with varying pore diameters and inter-pore distances were first optimized by anodizing Aluminum tape with variable currents. Cadmium Sulfide nanowires were then synthesized inside the membranes by dc electro-deposition. Finally a high work function metal was deposited on top as a contact for the metal-semiconductor Schottky diode junction. As a comparative study, Schottky diodes fabricated using the same metals and Cadmium Sulfide thin films deposited on conducting glass substrates using electro-deposition and annealed in different ambient were also studied. Device characterizations were carried out by field-emission scanning electron microscopy (FESEM), current – voltage (I-V) measurements, ultraviolet-visual (UV-Vis) absorption spectroscopy and X-Ray diffraction.

KEYWORDS: Cadmium Sulfide (CdS), Schottky diode, AAO membranes, Electro-deposition and Thermal Treatments.

Shounak Mishra
December 12, 2007
SCHOTTKY DIODES FROM CADMIUM SULFIDE (CdS) NANOWIRES DEPOSITED IN POROUS ALUMINA TEMPLATES

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SCHOTTKY DIODES FROM CADMIUM SULFIDE (CdS) NANOWIRES
DEPOSITED IN POROUS ALUMINA TEMPLATES

THESIS

A thesis submitted in partial fulfillment of the requirements for the degree of Master
of Science in the College of Engineering at the
University of Kentucky

By
Shounak Mishra
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Lexington, Kentucky
2007

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DEDICATION

To My Parents
ACKNOWLEDGEMENTS

I would like to take this opportunity to express my sincere thanks and heartfelt gratitude to my academic advisor and thesis chair Dr. Ingrid St. Omer for her guidance and support throughout my thesis. I am very thankful to my thesis co-director Dr. Vijay P. Singh for his constant encouragement and financial support during the thesis. I also would like to extend my thanks to Dr. Todd Hastings for serving on my thesis committee and providing me with invaluable comments and suggestions for improving this thesis.

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Schottky Diodes from Cadmium Sulfide (CdS) Nanowires Deposited in Porous Alumina Templates
1. Introduction

With the advent of nanotechnology during recent years, there has been a lot of interest in the research community to study the properties of semiconductors when synthesized in nanoscale regime. Cadmium Sulfide (CdS), Cadmium Telluride (CdTe) and Cadmium Selenide (CdSe) are among some of the well known inorganic materials that are currently being investigated for their nanoscale properties and possible integration into nanoscaled optoelectronic devices of the future. CdS being a direct bandgap II-VI semiconductor (bandgap = 2.42 eV), coupled with the fact that it is transparent at optical wavelengths and can be synthesized in both cubic-β and hexagonal-α forms especially generates a lot of interest from the scientific community.

Research on nanoscale CdS Schottky diodes has traditionally focused on fabricating nanocrystalline CdS on conducting substrates by techniques like chemical bath deposition (CBD)[1-2], monosurfactant systems[3], chemical vapor deposition (CVD)[4], etc. and carrying out various characterization experiments like Raman spectroscopy, I-V measurements, capacitance – voltage (C-V) measurements, FESEM, transmission electron microscopy (TEM), photoelectric effect experiments, X-Ray photoemission, etc. Though, the CBD, CVD and monosurfactant techniques do result in synthesis of nanoscaled CdS, but since the CdS grains tend to agglomerate, there is no actual separation between individual particles. Hence, a nanostructured device can’t be realized using these techniques. Therefore, many researchers prefer to use a pre-fabricated nanostructured template such as the porous alumina membrane to keep individual particles isolated. Confinement of CdS inside such a small space allows the device designer to have complete access to unique advantages like increased energy bandgaps due to quantum confinement. This enables the designer to fabricate devices with desired bandgap energies by custom-tailoring the nanoscale dimension of the template. Using these novel platforms, researchers have created many unconventional device structures, such as quantum dots [5-8] and nanowires [9-13].

The work in this thesis draws its inspiration primarily from the works of Routkevitch, et al. [9] who first demonstrated CdS nanowires fabricated by DC electroddeposition using an organic bath inside porous alumina membranes. Subsequent researchers in this realm have not only been able to duplicate their work [10-16] but have
also developed alternatives to deposit CdS inside anodic Aluminum Oxide (AAO) membranes such as by chemical vapor deposition (CVD) synthesis [17], chemical bath deposition (CBD) [18, 19] and pulsed DC electro-deposition [20].

We demonstrate galvanostatic anodizations as a means to fabricate porous AAO membranes with differing pore diameters and inter-pore distances in this work. We also discuss voltage ramping and chemical etching techniques as means of optimizing the AAO quality. These templates form the basis for fabricating CdS nanowire-Au/Ni Schottky diodes. Apart from demonstrating the variation in I-V characteristics of CdS nanowire-Au/Ni Schottky diodes with their nanowire diameters, this thesis also presents a comparative study of these diodes with those fabricated on a conducting glass substrate pre-coated with Indium tin oxide (InSnO$_2$). We also examine the changes in absorption spectra of CdS thin films when subjected to different thermal treatments.

This document focuses on explaining the theory, experimental and characterization procedures followed by results and their subsequent. Chapter 2 describes the theory behind metal-semiconductor junctions and the origin of Schottky diodes. The third chapter describes the fabrication procedures for the devices while the fourth chapter explains in detail the characterization techniques, preparation of samples, etc. The fifth chapter presents a discussion of results on the optimization work carried out for fabrication on porous AAO membranes by galvanostatic anodizations and barrier layer (B.L.) removal by voltage ramping and chemical etching. It also attempts to elucidate the differences between the electrical and optical characteristics of the Schottky diodes fabricated inside AAO templates and those fabricated on a conducting substrate using electro-deposition along with explaining the effects of thermal treatments. The discussion and analysis on the obtained results are provided simultaneously along with the results. The last chapter summarizes the thesis and presents the conclusions drawn and presents suggestions for future research work.
2. Metal – Semiconductor Junctions

A junction is said to be formed when two materials having different characteristics are brought together in such a fashion that the distances between them are comparable to inter-atomic distances. That being said, one can easily envisage the formation of a metal-semiconductor junction. In the early days of semiconductor research, such junctions were formed by pressing a piece of metal to the semiconductor surface. Nowadays, however, such contacts are made by photo-lithographically defining the contact area on a pre-cleaned semiconductor surface followed by metal layer deposition on top by means of thermal/e-beam evaporation or sputtering [21].

The study of metal-semiconductor junctions goes back as far as 1874 when Braun first presented a systematic approach to study the junction. In subsequent years, with the advent of quantum physics, researchers applied the energy band theory of solids to semiconductors to make a comprehensive study of junctions. Finally in 1938 Schottky proposed the lowering of potential energy for charge carrier emission upon application of electric field induced by an image-force, now named after him as the Schottky effect. The same year, Mott theoretically derived and proposed the Mott barrier in swept-out metal-semiconductor junctions [22].

As gate electrodes of MESFETS, source-drain contacts for MOSFETS, high-power IMPATT oscillators and in optoelectronic devices, metal-semiconductor junctions still find wide applications in the semiconductor industry. The discussion in this chapter concentrates primarily on the salient features and types of metal-semiconductor junctions. A detailed investigation of such junctions is out of the scope of this thesis and can be found in advanced textbooks listed in the References.

Metal-semiconductor junctions can be classified as either ohmic or rectifying (also known as Schottky diodes) contacts depending on the relative work function difference between the metal and semiconductor, and type of the semiconductor used (p-type or n-type). An ohmic contact behaves like any ordinary resistor thus, providing the means to connect a purely semiconductor based device to the outside world. A rectifying contact on the other hand, behaves like a p-n junction diode, having a typical characteristic “turn-on” voltage and I-V behavior. However, unlike the p-n junction diode, the current in a
metal-semiconductor junction is always because of majority carriers in the semiconductor (i.e. electrons for n-type and holes for p-type).

2.1 Ohmic Contacts

An ohmic contact is formed with an n-type semiconductor when a metal having a lower work function than that of the semiconductor (i.e. $\Phi_m < \Phi_s$) is deposited as a contact on the semiconductor surface. The energy band diagram for such a junction can be derived by first drawing the band diagrams of the materials involved when they are separated by a large distance, then aligning the Fermi levels. The band diagram for such a contact involving an n-type semiconductor is depicted in Figure 2.1. In equilibrium, the electrons (being the majority carrier) see no barrier when moving from the semiconductor to the metal. However, if the electrons were to move in the opposite direction (i.e. when reverse biased), they will come across a barrier, which breaks on application of small voltages. Hence, the junction effectively acts as a linear resistor. Conversely, for a p-type semiconductor a metal of higher work function (i.e. $\Phi_m > \Phi_s$) must be deposited on top of the semiconductor surface to form an ohmic contact. Schematic representation of the energy bands of such a junction is depicted in Figure 2.2 below. The Vacuum Level is the reference energy level for all materials and depicts the lowest state of an electron when removed from the material. The Electron Affinity ($\chi$) is defined as the energy required for moving an electron from the conduction band to the vacuum level. The Work Function ($\Phi$) is the energy required to move an electron from the Fermi level to the vacuum level. $E_{Fs}$ & $E_{Fm}$ are the Fermi energy levels of semiconductor and metal respectively and $E_C$ & $E_V$ are the conduction and the valence band energies respectively [21].
Figure 2.1: Energy band diagram for Ohmic Contact between metal & n-type semiconductor [21].

Figure 2.2: Energy band diagram for Ohmic Contact between metal & p-type semiconductor [21].
2.2 Schottky Diodes

A Schottky diode is formed with an n-type semiconductor when a metal of higher work function as compared to that of the semiconductor (i.e. $\Phi_m > \Phi_s$) is deposited on top of it. When the two materials are brought together, excess charges diffuse from the semiconductor to the metal thereby neutralizing the existing initial potential barrier. At thermal equilibrium there exists a depletion layer in the semiconductor which is devoid of majority carriers (i.e. electrons). This is equally matched by an equal and opposite (negative) charge on the metal surface. Since, the Fermi levels of both materials must align at equilibrium, the conduction and valence energy bands of the semiconductor must shift by a relative amount. In the case of the n-type semiconductor, the electro-static potential rises (i.e. the electron energy lessens) to accommodate this change brought about by the alignment of Fermi levels. The energy band diagrams for a Schottky diode involving an n-type semiconductor is depicted below in Figure 2.3. Conversely, for a p-type semiconductor a rectifying contact will be formed when a metal of lower work function is deposited on top (i.e. $\Phi_m < \Phi_s$). The energy band diagram of a Schottky diode involving a p-type semiconductor is shown in Figure 2.4 [21].

![Energy band diagram for Schottky diode between metal & n-type semiconductor](image)

Figure 2.3: Energy band diagram for Schottky diode between metal & n-type semiconductor [21].
2.2.1 Schottky Diode Characteristics

A Schottky diode is characterized by the observance of the Schottky effect. Essentially this means that when charges of a particular kind are present on the semiconductor surface (say negative for example), equal and opposite charges are induced on the metal surface (in this case positive). Upon application of an electric field (by applying a voltage for example) across this junction, the electric field together with the induced-charges results in the lowering of the work function. This effect is named after its discoverer as the Schottky effect [22].

Since the rectifying contact behaves the same way as a p-n junction diode, the following equation can be used to account for the I-V characteristics of the metal-semiconductor junction.

\[ I = I_s \left( e^{\frac{qV_A}{kT}} - 1 \right) \]

Where, \( I_s \) is the saturation current, \( V_A \) is the applied voltage, \( k \) is Boltzmann’s constant and \( q \) is the charge of a single electron [23].
Upon forward basing the Schottky junction, thermionic emission and tunneling are the dominant factors contributing to the flow of majority charge carriers across the junction. Recombination in the depletion region and hole diffusion from the metal to the semiconductor however, contribute negligibly to the current flow. Accounting for the thermionic emission process, the diode equation given above can be modified to truly account for the I-V characteristics as:

\[ I_D = A e^\frac{q(\Phi_m - \chi)}{kT} \]

Where, \( A \) is the area of the contact and \( A^* \) is the effective Richardson constant defined as [23]

\[ A^* = \left( \frac{m_n^*}{m_e} \right) \times 1.20 \text{amps/cm}^2/\text{K} \]

The energy band diagrams for an n-type metal-semiconductor rectifying contact under forward and reverse biasing conditions are shown in Figure 2.5 below.

Figure 2.5: Energy band diagrams of metal & n-type semiconductor in forward and reverse bias [21].

A detailed treatment of the Schottky diode characteristics involving non-idealities and thermionic emission theory can be found in the textbook mentioned in reference [22].
3. Fabrication Procedures

The fabrication of CdS-Au/Ni Schottky diodes inside porous alumina membranes of varying pore diameters and inter-pore distances involved a series of procedures aiming at the fabrication of AAO membranes having requisite characteristics, the study of different planar CdS thin films made by d.c. electro-deposition, and finally, optimizing the appropriate conditions (by techniques such as a.c., galvanostatic d.c., potentiostatic d.c. and chemical bath deposition) for deposition of CdS. The final device structure is shown in Figure 3.1 below. It consisted of a thick Aluminum back layer (50-55µm) on top of which a 2 to 2½ µm layer of porous AAO was grown. This was filled with CdS using d.c. electro-deposition followed by Au/Ni contact deposition by E-beam evaporation. Devices were characterized by scanning electron microscopy, UV-Visual absorption spectroscopy, X-Ray diffraction and I-V measurements.

![Figure 3.1: Schematic of device structure for CdS-Au/Ni Schottky diode inside AAO templates.](image)

3.1 Fabrication of nano-porous anodic alumina membranes

The history of nano-porous anodic alumina membranes can be traced all the way back to 1953 when Keller et al. [24] first devised a method to fabricate the membranes by anodizing Aluminum in an acidic bath and presented a case study demonstrating that
the porosity of such membranes could be controlled by means of changing the anodizing voltage. The actual turnaround in the history of AAO membranes however can be attributed to Masuda and his team at the Tokyo University, who in 1995, demonstrated a two-step process to fabricate porous AAO and suggested its suitability for use as a nanoscale template [25]. Subsequent studies by researchers have not only resulted in a detailed theoretical and practical investigation of the pore-formation process [26,27], but have also succeeded in optimizing the conditions to fabricate membranes with very small pores [28] both in a laboratory setting as well as on a commercial scale [29]. Different techniques to characterize the membranes have also been devised [30,31]. Researchers have also been successful in using the porous alumina membrane as the starting template to fabricate a myriad of nanoscaled materials, both metallic [32-38] and non-metallic [38-41], and lately even carbon [42-44] and silicon [45]. Their low cost, ease of fabrication, flexibility and electrical inertness makes these templates an ideal candidate for the development of a wide variety of practically applicable devices such as filtration membranes [46,47] for DNA separation [48], bacterial dispersion [49], desalination [50], gas permeation & separation [51], as well as fuel cells [52], rechargeable batteries [53], electro-osmotic pumps [54] and even for MEMS packaging [55].

Typically, the procedure for fabricating anodic alumina consists of an electrochemical cell with an Aluminum substrate as the anode and Platinum as the cathode suspended in an acidic bath. Anodizations are usually carried out with a constant voltage source. The characteristics of the anodic alumina thus produced depends on a host of experimental parameters, most notably the ambient temperature, concentration of acidic solution, type of acid used, distance between electrodes, physical dimensions of electrodes, current density and voltages used. Any of these parameters could be varied to produce AAO membranes with desired variation of pore diameters and inter-pore distances.

3.1.1 Galvanostatic Anodizations

Since the formation of pores in AAO depends directly on the existing electric field between the electrodes, it can be inferred that the current density at the electrodes is responsible for the porosity of the alumina membranes. Hence, for the purpose of
fabricating AAO with varying pore diameters and inter-pore distances, galvanostatic means of anodization was selected as the preferred choice. Additionally, the effect of varying anodization temperature on pore diameters was also studied.

A piece of Aluminum tape measuring 1 inch (in.) square (sq.) and 60 µm in thickness was first cut from the tape roll and smoothed out until flat. It was then immersed in Methanol and sonicated at high frequencies for a couple of minutes, followed by a de-ionized (D.I.) water rinse. Substrates were then subjected to a second round of sonication with Acetone, followed by a rinse with de-ionized water and drying in flowing Nitrogen. Substrates thus prepared and thoroughly cleaned were subsequently used for the electrochemical anodization procedure as detailed by Knaack, Redden and Onellion [56]. A flat Platinum sheet measuring 1 square inch was used as the cathode while the substrates were used as anode. This setup was placed in a 0.3M oxalic acid solution which was continually stirred at the rate of 60 revolutions per minute (rpm). The voltage was supplied using a Kepco (Model ABC 125-1DM) programmable power supply. Anodizations were carried out at the following currents: 6, 8, 10, 20, 40, 60, 75, 80 and 100 mA, in two different temperature ambients 5°C (performed inside a commercially available Frigidaire refrigerator) and at 27°C (i.e. room temperature). Anodization experiments were continuously monitored for variations in voltages with respect to elapsed time and were compared with the results of Ding et. al. [57] for consistency. The monitoring was done using an application software developed in-house using LabVIEW 7.0 student edition provided by National Instruments. A screenshot of the software is shown in Figure 3.2 below. Additional screenshots showing the back-end LabVIEW program are listed in the Appendix. Detailed explanations of the current and voltage vs. time graphs can be found in Chapter 5.

The AAO membranes thus fabricated were then rinsed in de-ionized water and dried in flowing Nitrogen after removal from the acidic bath. Membranes were then soaked in Acetone for a period of 24 – 48 hours to remove tape and adhesive from the back. Templates were then soaked in a mixture of Cupric Chloride (CuCl2) and dilute Hydrochloric Acid (HCl) solution to remove the excess Aluminum from the backside of the templates. Barrier layer formed at the junction of pores and residual Aluminum was removed by floating the templates for 2 minutes (min.) in a solution of 5% dilute
Phosphoric Acid (H₃PO₄) maintained at a constant temperature of 60°C. The membranes were then thermally annealed in pure oxygen at 400°C for a period of 2-3 hours to expel any remaining traces of water or other impurities present. Samples hence fabricated were characterized by scanning electron microscopy (SEM).

3.1.2 Barrier Layer Removal by Voltage Ramping

Studies attempting to decipher the inherent mechanisms of the anodization process have remarked on how the volume expansion of the porous structure always occurs in the transverse direction with almost negligible growth in the lateral directions [26]. One of the remarkable things to note is the formation of the cup-shaped structure at the junction of the residual Aluminum and the porous Al₂O₃ which plays a pivotal role in the volume expansion of the porous structure. This layer, also referred to as the barrier layer (B.L.) is not of much use from the device engineering point of view as it offers an electrically insulated barrier to the underlying substrate. In our case, since we aim to fill

![Screenshot of anodization setup automation software developed using LabVIEW 7.0.](image)
up the pores with a semiconducting material (i.e. CdS), and aim to fabricate a Schottky device at the top by depositing a metal, we need an ohmic junction at the bottom as the back contact. This back contact with the Aluminum substrate can be hampered due to the B.L. Hence, it was natural to undertake a study to evaluate and choose a means to eliminate the B.L. completely from the bottom of the pores.

Researchers studying the dynamics of B.L. etching have suggested two primary means of eliminating the B.L. completely. The first technique uses variation in the anodizing voltage during the last stages of the AAO growth to break through the B.L and separate the AAO from the underlying substrate. The other technique uses chemical etching as a means of dissolving the B.L. Both techniques were studied in detail to evaluate the suitability of a particular method for integration into the process of making Schottky diodes. The first technique is detailed here while the second technique is elaborately discussed in the next section.

Previous research indicates that the B.L. thickness can be easily influenced by varying process parameters such as the temperature of anodization [58]. Researchers have also demonstrated different means to eliminate B.L. completely. Most notably among these are: Stepping down the voltage uniformly at a specific rate when the anodization is nearing its end [59, 60]; Stepping up the voltage after anodization to free the AAO from the substrate [61]; Using a reverse voltage of appropriate magnitude to initiate a reaction at the anode which dissolves the B.L. [62], and re-anodizing the membrane to remove B.L. [63]. The advantage of the voltage ramping technique lies in the fact that B.L. can be removed in-situ simultaneously while anodizing. This eliminates the need to separate the AAO from the underlying conducting substrates, quite unlike the time-consuming chemical etching techniques which, almost always cause pore opening of the AAO, thereby degrading the quality of the membranes.

To study the effect of voltage ramping on 60 µm thick AAO membranes (measuring 1 in. sq.) two basic studies were performed. For the first set of experiments, anodization voltages were stepped down by different ramping rates while, for the second set of experiments, voltages were ramped up. The automated software developed for anodizations (as shown in Figure 3.2) was modified with a control for automatically ramping down the supply voltage by a user specified rate upon encountering very low
currents (signaling the end of anodizations). For voltage ramping-down studies, the following rates were tried: 0.0001, 0.001, 0.01, 0.07, 0.08, 0.09, 0.1, 0.2, 0.3, 0.4, 0.5, 0.6, 0.7, 0.8, 0.9, 1, 1.125, 1.5, 2, 2.5, 5, 7.5, and 10 Volts/second (V/sec.). For voltage ramping-up studies, supply voltage was stepped up at the rate of 0.05 V/sec after the completion of the anodization. All samples were characterized by scanning electron microscopy.

3.1.3 Barrier Layer Removal by Chemical Etching

Chemical means for removal of the B.L. is not an uncommon technique and has been widely studied before. Typically researchers have used dilute Mercury Chloride (HgCl₂) or dilute H₃PO₄ as the preferred etchant. Immersing membranes in a 5 wt.% H₃PO₄ for an extended time is one of the methods widely used [64] though immersing them in a 0.4M H₃PO₄ solution at elevated temperatures has also been investigated before [65].

For our purpose however, a 85 wt.% H₃PO₄ solution was used. A few droplets of this thick viscous solution were put on a glass petridish held at a constant temperature. The templates were floated on the solution for different time durations: ½ min., 1 min., 1-½ min., 2 min., 2-½ min., 2 min. 35 sec., 2 min. 40 sec., 2 min. 45 sec., 2 min. 50 sec, 2 min. 55 sec., 3 min. and 3-½ minutes. The experiments were conducted at two different temperatures: room temperature (i.e. 27°C) and at 45°C. Characterizations were done using field emission scanning electron microscopy. These results have been summarized in Chapter 5.

3.2 Fabrication of CdS thin films on conducting glass substrates

CdS thin films were deposited on conducting glass substrates and were studied for their electrical and optical properties. These studies were performed in order to generate a comparison study between planar structured CdS Schottky diodes and diodes fabricated in AAO templates. CdS thin films can be deposited on conducting substrates primarily by two techniques: chemical bath deposition and electro-deposition. The electrochemical technique can be affected by two means: an aqueous bath [18] or an organic bath based on Dimethyl Sulfoxide (DMSO). Applying constant d.c. voltage [10], constant current [66], using cyclic voltammetry [6] or using an a.c. source [9] are among the primary
techniques employed for electrochemical growth. For our purpose of fabricating a planar diode, d.c. electro-deposition at a constant voltage was chosen as the preferred means to deposit CdS thin films.

3.2.1 Thermal treatments on planar CdS thin films

Glass substrates measuring 1 in. sq. and 1 mm thick, coated with Indium Tin Oxide (ITO) on one side with a nominal sheet resistance of 28 Ω/in.² were first cleaned by sonication in Methanol for 10 minutes followed by rinsing in de-ionized water and drying in flowing Nitrogen. This was followed by a subsequent round of sonication with Acetone again for 10 minutes followed by rinsing and drying. Substrates thus cleaned were then used as the cathode while a sheet of 1 in. sq. Platinum was used as the anode in the electrochemical cell. The bath was prepared using 0.055M CdCl₂ and 0.19M elemental Sulfur dissolved in 175 ml of DMSO at 110 °C. The power supply was provided using a Kepco programmable power supply (Model ABC 125-1DM). Multiple electro-depositions were carried out at 8 Volts for durations of 6 minutes each. Samples were then annealed in ultra high purity Nitrogen, Argon and in a vacuum oven at temperatures of 200°C and at 300°C. Characterizations were done by UV-Visual absorption spectroscopy, X-Ray diffraction and by scanning electron microscopy.

3.2.2 CdS thin film Schottky diodes on conducting glass substrates

The d.c. electro-deposition technique as detailed in the above section was used to deposit thin films on conducting glass substrates. However, for this study both the voltage and duration of deposition were varied to obtain films with varying grain sizes and varying thicknesses respectively. For the first set of experiments, samples were fabricated with a supply voltage of 8 Volts and deposition times were varied as: 2 min., 4 min. 6 min. 8 min. and 10 min. For the second set of experiments, deposition time was kept constant at 6 minutes and supply voltages were varied as: 2V, 4V, 6V, 8V and 10V. Substrates were cleaned with DMSO after deposition and were characterized by X-Ray diffraction, UV-Vis spectroscopy and scanning electron microscopy. No annealing treatments were performed on substrates at any processing step. Afterwards, circular Gold and Nickel contacts, measuring 0.07 cm² in area and 100 nm in thickness, were deposited using e-beam evaporation and devices were characterized by I-V
measurements. Results of these have been summarized and presented as comparative study to the results obtained from CdS Schottky diodes fabricated in AAO membranes in Chapter 5.

3.3 Fabrication of CdS-Au/Ni Schottky diodes in AAO templates

Fabrication of CdS nanowires in porous AAO membranes was by far the most daunting task of the entire project. The initial experiments done on 60 µm thick AAO templates measuring 1 in. sq. (the fabrication methodology of which is detailed in the beginning of this chapter) failed miserably, owing to the fact that we were trying to fill up the entire 60 µm long channel using electro-deposition which wasn’t able to provide the required thrust to drive the CdS nano-particles present in the electro-chemical bath inside the long channels of the membrane. Many variations of electro-deposition were tried to this effect, namely potentiostatic d.c. electro-deposition, galvanostatic d.c. electro-depositions and a.c. electro-deposition with varying voltages. It was finally discovered that in order to fill up long channels (~60 µm in length) chemical bath deposition works the best, while electro-deposition works the best when the channels are much shorter (~2 µm in length); although, chemical bath deposition can also be used to deposit CdS inside the short channel AAO templates. The fabrication of CdS nanowires inside AAO pores can be viewed as two tasks. First is the fabrication of short channel AAO templates followed by the actual task of electro-deposition and metal deposition which results in formation of Schottky diodes.

3.3.1 Fabrication of short channel AAO templates

A piece of 60 µm thick Aluminum tape was first rolled onto a flat table top and flattened. Square pieces measuring 1 inch on each side were cut from this tape and were subjected to cleaning and de-greasing treatment. This was done by first sonicking the substrates in Methanol for 10 mins. followed by rinsing with de-ionized water and drying with flowing Nitrogen. A second round of sonication was then done using Acetone followed by the usual rinsing and drying. Substrates thus cleaned were then subjected to the first step of anodization using 0.3M oxalic acid solution. Anodizations were carried out at 20 Volts for 10 minutes after which the voltage was turned down abruptly. Substrates were then rinsed with de-ionized water and were immersed in a mixture of 5%
H₃PO₄ and 2% Chromic Acid (H₂Cr₂O₇) kept at a constant temperature of 80°C for 1 minute. This removed the initially formed Al₂O₃ from the substrates leaving nanoscaled imprints on the top surface. These imprints act as the initiation points for the subsequent anodizations resulting in better pore structures. Samples were then cleaned once again by rinsing with de-ionized water and drying with flowing Nitrogen. The second step involved anodization at a constant 40 Volts for a duration of 15 minutes at 27 °C using 0.3M oxalic acid. The electro-chemical bath was consistently stirred at 60 rpm for better homogeneity. At the end of anodization the supply voltage was ramped down at a constant rate of 3 Volts/min. until the supply reached 10 Volts. After this the ramping rate was reduced to 1 Volt/min. till the supply reached 1 Volt. At this point the anodization was allowed to go on for the next 10 minutes after which the supply was turned off. Substrates were then rinsed with de-ionized water and were dried using flowing Nitrogen. They were then immersed in Acetone solution for a period of 48 hours to allow for removal of tape and adhesive from the backside. Templates hence obtained were cleaned and then annealed in oxygen at a temperature of 400°C for period of 4 to 6 hours for removal of impurities such as hydroxides. For varying the pore diameters of the templates hence produced, the supply voltages were varied during the second anodization step. Templates with varying pore diameters were used for CdS depositions.

3.3.2 CdS Schottky diodes in AAO templates by chemical bath deposition

CdS nanowires were grown in short channel AAO templates using two techniques: chemical bath deposition and d.c. electro-deposition. Schottky diodes were fabricated using both the techniques and their characteristics studied and compared. For chemical bath deposition, templates were immersed in a solution prepared by dissolving 0.02M Cadmium Chloride (CdCl₂), 0.05M Thiourea ((NH₂)₂CS) and 0.05M Ammonium Chloride (NH₄Cl) in de-ionized water which was continually stirred and kept at a constant temperature of 80°C. When the solution became homogenous, Ammonium Hydroxide (NH₄OH) (used as the complexing agent) was added to adjust the pH to 11. Deposition was carried out for a period of 1 hour to allow for complete filling up of the pores. Templates were then taken out and wiped with cotton dipped in 38% HCl solution to clean off the excess CdS deposited on the top surface. Membranes hence treated were
then annealed in ultra high purity Argon at 400°C for 1 hr. to allow the CdS particles to coalesce and form into a nanowire. Gold and Nickel circular contacts measuring 0.07 cm² in area and 100 nm in thickness were then deposited on top by e-beam evaporation using a plain Aluminum foil as a mask. Devices were then subjected to a post-metal annealing treatment by annealing them in Argon at 400°C for 1 hour. Subsequent characterizations were done by SEM, X-Ray diffraction and I-V analysis. The results hence obtained are summarized in Chapter 5.

3.3.3 CdS Schottky diodes in AAO templates by d.c. electro-deposition

The chemical bath for d.c. electro-deposition was prepared by dissolving 0.055M CdCl₂ and 0.19M elemental Sulfur in 175 ml of Dimethyl Sulfoxide (DMSO) and heating the bath with continual stirring to 120°C. A square sheet of Platinum measuring 1 in. sq. was used as the anode while the substrates with different pore diameters were made the cathode. Galvanostatic d.c. depositions were carried out at 20 mA for a duration of 10 minutes each. Top surfaces of the substrates hence obtained were then cleaned with DMSO followed by 0.5N HCl which removed the excess CdS deposited at the top. Membranes were then subjected to annealing (to allow CdS particles to coalesce into nanowires), Gold and Nickel contact deposition, post metal annealing treatment and characterization experiments identical to as detailed in section 3.3.2. The results of these characterization experiments are discussed further under the chapter on results and discussion. For optical characterization, a small piece of the template was cut and floated on 85 wt.% H₃PO₄ solution kept at 80 °C for a duration of 1 min. This dissolved the porous alumina from the top of the template leaving the CdS nanowires freely floating in the solution. The template was then removed and the solution was extracted using a syringe. This solution was then characterized for optical absorption in the UV-Visual wavelengths against a solution of plain 85 wt.% H₃PO₄ which acted as the baseline.
4. Characterization Procedures

Characterization procedures form the bulk part of any research work. They not only help the researcher to ascertain the properties of a particular device fabricated but also help in establishing the cause of failures thereby allowing room for improvements in the processing steps. The devices and structures fabricated as a part of this thesis primarily relied on the following procedures for characterizations: Field Emission Scanning Electron Microscopy, Ultraviolet-Visual Absorption Spectroscopy, X-Ray Diffraction and Current – Voltage Analysis. The subsequent sections in this chapter attempt to present an encapsulated description of these procedures.

4.1 Field Emission Scanning Electron Microscopy

A Field Emission Scanning Electron Microscope (FESEM) works by scanning a high energy electron beam (usually generated by field emission of a Tungsten filament) in a typical raster fashion over a sample. Upon hitting the sample, the electron beam generates secondary electrons, back-scattered electrons and X-rays, all of which are collected by a collector to infer qualitative and quantitative information about the sample being studied. Typically such information involves a detailed topographic view of the sample and the elemental content at a particular location on the sample. A Hitachi FESEM (Model S-900) with a maximum magnification power of 800kX at an accelerating potential of 3k Volts was used for characterization purposes for this thesis work.

To image a particular sample, a very small section of the sample was cut-off from the original sample and mounted on a 2mm x 5 mm double-sided sticky carbon tape stuck on a small copper stub. The sample was coated with colloidal graphite on the edges and a known thickness of Gold-Palladium alloy was sputter coated to ensure proper electrical conductivity throughout the sample. Samples were typically imaged at 3kV to get the best resolution. Specimens were imaged for both topology as well as cross-sectional views. Imaging helped in ascertaining the pore diameters, inter-pore distances, thicknesses of CdS layer deposited as planar structures, their grain sizes and extent of AAO pore filling by CdS deposition.
4.2 Ultraviolet-Visual Absorption Spectroscopy

Absorption spectroscopy in the optical and ultraviolet wavelengths is a routine procedure employed in chemistry to quantitatively determine solutions of transition metal ions and conjugate organic compounds. However, the wavelength vs. absorption spectra that is obtained by the means of a UV-Vis spectrophotometer can also be used to infer the bandgap energy of the material being studied using Tauc’s Law [70-70]. UV-Vis spectroscopy was used to infer the optical properties of the CdS thin films deposited on conducting glass substrates with respect to varying thicknesses and grain sizes. Absorption spectrum of a material being studied is usually obtained against a specific background, in this case the spectrum obtained from a blank conducting glass substrate.

The experimental procedure involved using a Cary-50 v3.0 UV-Visual Spectrophotometer to scan a clean conducting glass substrate first as the background; the other samples with the CdS thin films were then subsequently scanned one by one and were plotted after the subtracting the background. Samples were typically scanned in between wavelengths of 200 nm to 800 nm. A detailed explanation of the graphs hence obtained is summarized in the next chapter.

4.3 X-Ray Diffraction

X-Ray Diffraction is a non-destructive characterization technique widely employed to ascertain the elemental composition and crystal structure of a particular material under investigation. It works by measuring properties of the scattered X-Ray beam as a function of its angle of incidence, intensity, polarization and wavelength for a particular material under investigation and comparing it with a known database kept by the International Center for Diffraction Data. Typically, X-Ray diffraction spectrum is plotted as intensity vs. 2θ, where θ is the angle of incidence. Every known material existing in elemental, alloy in compound form has an X-Ray spectrum associated with it which is characteristic of that particular material. Thus, X-Ray diffraction is typically used to ascertain the quality (or degree of purity) of a particular substance. For the purpose of this thesis work, X-Ray diffraction spectra were used to infer the quality and phase of CdS thin films deposited on planar structures. They were also used on nanowires deposited in AAO templates to investigate their crystallographic structures.
A Bruker-AXS D8 DISCOVER Diffractometer was used to obtain the X-ray diffraction spectra of all the films deposited. The glass substrate with appropriately deposited CdS film was first properly aligned with respect to the X-ray source and the detector. After alignment, automated proprietary software was used to obtain the diffraction spectrum for 20 values from 3° to 80° of angles of incidence. Patterns thus obtained were cross-referenced with the spectra in the reference database for suitable match and identification of compounds present in the sample.

4.4 I-V Characterization and Analysis

Current–voltage measurements form the basic backbone of any characterization procedure done on electrical devices. Besides giving an idea of how the currents flowing through the device change as a function of the voltage applied, which could be used to infer the power consumed by the device; the current-voltage plots are also employed to collect other valuable information about a device namely, the series resistance (R_s), shunt resistance (R_sh), diode ideality factor (η), diode saturation current (I_0), short circuit current (I_sc), open circuit voltage (V_oc), maximum power point (P_m), fill factor and conversion efficiency [70].

The experimental procedure to obtain the current vs. voltage (or more appropriately current density vs. voltage plot) involved the use of a solar simulator where fabricated devices were measured in both dark and light (illumination equivalent to 1 sun) conditions. The equipment consisted of a Kepco programmable bipolar operational amplifier/power supply (Model BOP 36-12M) and two Keithley digital multimeters employed as voltmeters (Model 2001 and 2000) interfaced with a common lab PC using an application software developed in-house with LabVIEW Student Edition 7.0 provided by National Instruments. Supply voltages were varied from -1 Volt to +5 Volts in steps of 0.1 Volts. Corresponding values of current were measured, converted to appropriate current density values and logged in the form of .txt files. A subsequent plot of these values generated the current density vs. voltage graphs from which other device parameters were calculated.
5. Results and Discussions

The results discussed in this chapter are categorized into three parts according to the experiments as discussed in the fabrication methodologies. The first section discusses the results of galvanostatic anodizations on Aluminum tapes and removal of barrier layer by voltage ramping and chemical etching techniques. The second section deals with planar CdS thin films, the effects of thermal treatments on their optical properties and electrical characteristics of planar Schottky diodes. The third and final section discusses the electrical characteristics of Schottky diodes formed by d.c. electro-deposition in AAO pores.

5.1 Porous AAO on Aluminum tapes

All the results discussed in this section are based on nano-porous anodic alumina membranes measuring 1 in. sq. and 60 µm in thickness.

5.1.1 Galvanostatic Anodizations

5.1.1.1 SEM Characterization

SEM characterization revealed in detail the variation in pore diameters and inter-pore diameters of the alumina membranes. The micrographs produced as such in Figure 5.1 and Figure 5.2 show the variation in pore diameters and inter-pore distances with anodization current. These results are also summarized in the graphs in Figure 5.3 and Figure 5.4. The graphs show that there is a linear dependence on pore diameter variation on the anodizing currents and that this phenomenon is independent of the temperature of anodization. Although the slope of the graph changes considerably with increase in temperature but the essential nature remains the same. This can be attributed to the fact that with the increase in currents, more ions of the solution become mobile but the increase in mobility action means that less ions of the acid actually reach the substrate to initiate the field-assisted dissolution process thereby resulting in small pore diameters hence the tendency of negative slope for pore diameters. Small pore diameters inherently mean larger inter-pore distances (and hence a positive slope).
Figure 5.1: SEM micrographs showing pore diameter & inter-pore distance variation with anodization currents at 5 °C: (a) 6mA (b) 8mA (c) 10mA (d) 20mA (e) 40mA (f) 60mA (g) 75mA (h) 80mA and (i) 100mA.
Figure 5.2: SEM micrographs showing variation in pore diameter and inter-pore distance with anodization current at 27 °C: (a) 20mA (b) 60mA (c) 75mA (d) 80mA and (e) 100mA.

Figure 5.3: Variation in pore diameters and inter-pore distances vs. anodizing currents at 5 °C.
Figure 5.4: Variation in pore diameters and inter-pore distances vs. anodizing currents at 27 °C.

Figure 5.5: Variation in pore diameters with respect to anodizing currents at 5 °C and at 27 °C.

Figure 5.5 above summarizes the variation in pore diameters with anodizing currents at different temperatures. The downward negative slope of both the curves can be very well attributed to the factors as mentioned above. Additionally it can also be inferred that at higher temperatures the pore diameters are greater than that formed at lower temperatures for the same anodizing currents. This can be attributed to the nature of anodization reaction. Anodization consists of two processes: electric field induced
dissolution and acidic bath associated oxidation of Aluminum. At higher temperatures, both the processes are far more active than that at lower temperatures. Hence, more and more Aluminum gets converted into Al₂O₃ leading to bigger sized pores.

### 5.1.1.2 Voltage – Time Graphs

We first present the case of a current – time graph from potentiostatic anodization. The graph shown in Figure 5.6 below depicts the entire record of current variation throughout the anodization process carried out at 5 °C at 40V. Zooming to the initial few seconds of the process, we find that it can be differentiated in three different zones: Region I shows the initial stage when the whole sample is conducting and hence conducts a high current. In the second region the drop in current is quite evident owing to the fact that the owing to the field assisted dissolution process a thin oxide layer forms on Aluminum substrate which is insulating in nature. The current drops to a particular value before rising again and becoming constant when both field assisted dissolution and chemical dissolution processes balance each other (Region III). Upon completion of anodization, the current essentially drops to zero signaling that the entire substrate has now become insulated (i.e. Al₂O₃).

![Figure 5.6: Current vs. Time graph for potentiostatic anodization at 40 Volts and 5 °C.](image)

A voltage – time graph for galvanostatic anodizations can also be explained in similar terms. The initial few seconds of such an experiment can also be differentiated in
three stages. However, since we are monitoring voltage, it will increase momentarily and then drop down. At the end of anodization, when the whole substrate is insulating, voltage will be as high as allowed by the setup. Figure 5.7 below depicts the graph for galvanostatic anodization carried out at 20 mA at 5 °C.

![Figure 5.7: Voltage vs. Time graph for galvanostatic anodization at 20 mA and 5 °C.](image)

**Figure 5.7:** Voltage vs. Time graph for galvanostatic anodization at 20 mA and 5 °C.

The graph shows three regions:
- **Region I:** Initial voltage increase due to ohmic heating.
- **Region II:** Voltage drops due to temperature stabilization.
- **Region III:** Voltage increases again due to current density increase.

![Figure 5.8: Voltage vs. Time graphs for galvanostatic anodizations at 5 °C at various currents.](image)

**Figure 5.8:** Voltage vs. Time graphs for galvanostatic anodizations at 5 °C at various currents.

- **6 mA**
- **10 mA**
- **20 mA**
- **40 mA**
- **60 mA**
- **75 mA**
- **80 mA**
- **100 mA**
The voltage vs. time graphs for galvanostatic anodizations carried out various currents at 5 °C are depicted in Figure 5.8. As the currents are progressively increased, it is observed that the initial voltage of anodization also increases. This is very much expected as with increased currents, more and more field induced dissolution takes place, leading to the formation of more and more alumina, hence the sample becomes more insulating thereby leading to higher initial voltages. The other observation that can be made from the above graph is that, with increasing currents, the actual time required for anodization decreases (signaled by the voltage which reaches its full value of 125 Volts). This can be also explained by the fact that the increasing currents leads to increase in the anodization process thus leading to quicker formation of AAO membranes.

Figure 5.9: Voltage vs. Time graphs for galvanostatic anodizations at 27 °C at various currents.

The above Figure 5.9 depicts the voltage – time graphs for the anodizations carried out at room temperature for various currents. The discussion for Figure 5.8 hold true for the case of Figure 5.9 as well; i.e. with the progressive increase in anodization
current, the initial anodization voltage increases and total time required to anodize a particular sample decreases.

Figure 5.10 below illustrates another important phenomenon. Voltages vs. time graphs for the same anodization current (i.e. 20 mA) are plotted for two different anodization temperatures viz. 5 °C and 27 °C. It is observed that the voltage for room temperature anodization is less than that at 5 °C indicating that less substrate surface is getting oxidized. At room temperature, ions of the electro-chemical solution become increasingly mobile and hence for the application of same anodization current less number of ions are available for the actual dissolution process. Hence less oxidation of Aluminum surface results leading to lower voltages of anodization.

![Figure 5.10: Voltage-Time graph for Galvanostatic anodization at 20mA carried out at 5 °C & 27 °C.](image)

### 5.1.2 Voltage Ramping studies for Barrier Layer removal

AAO membranes prepared for voltage ramping studies to remove B.L. from the membrane backside were fabricated by potentiostatic anodizations at 5 °C keeping the voltage constant at 40 Volts. The samples were characterized by scanning electron microscopy and current – time analysis.

#### 5.1.2.1 SEM Characterization

The SEM micrographs obtained for some cases of AAO membranes’ backside for voltage ramping up and ramping down are produced as such in Figure 5.11 below.
Figure 5.11: SEM micrographs of potentiostatic AAO membranes (40V, 5 °C) prepared with different ramping down voltages: (a) 0.1 V/s (b) 0.01 V/s (c) 0.001 V/s (d) 2.5 V/s (e) 5 V/s (f) 7.5 V/s (g) 10 V/s (h) 1.5 V/s and (i) ramping up by 0.05 V/s.

Unfortunately, all the micrographs reveal that there is almost no decipherable effect of voltage ramping (whether it is ramped up or down) on the thickness of the B.L.
and hence it can’t be used as a method to eliminate the issue of B.L. completely. The AAO membranes were also characterized by means of current-time graphs.

### 5.1.2.2 Current – Time Graphs

The current – time graphs for a few cases of anodizations with voltage ramping down studies are shown in Figure 5.12 below. The graphs characteristically show the different slopes as the voltage is gradually ramped down at a pre-specified rate to zero. Some plots also depict a lot of noise in the measurements which can be attributed to the fact that the conditions of anodizations were far from ideal and might have been contributed by fluctuations in anodization temperature, substrate surface perfectness and imperfections in electrical contacts.

![Current - Time graphs for potentiostatic anodizations (40 Volts, 5 °C) for different voltage ramping down rates.](image)

**Figure 5.12:** Current - Time graphs for potentiostatic anodizations (40 Volts, 5 °C) for different voltage ramping down rates.

### 5.1.3 Chemical Etching studies for Barrier Layer removal

The SEM micrographs showing the results of chemical etching by 85 wt.% H₃PO₄ (Phosphoric acid) at room temperature and at 45 °C are summarized in Figure 5.13 and Figure 5.14.
Figure 5.13: SEM micrographs showing effect of 85 wt.% H₃PO₄ etch at room temperature on B.L. for: (a) 1 min. (b) 1 min. 30 sec. (c) 2 min. (d) 2 min. 30 sec. (e) 2 min. 40 sec. (f) 2 min. 45 sec. (g) 2 min. 50 sec. (h) 2 min. 55 sec. and (i) 3 min.
The micrographs reveal that at room temperature 85 wt.% H$_3$PO$_4$ has little effect on the B.L. even when etching is done for durations up to 3 minutes. However, at elevated temperatures due to high reaction rate 85 wt.% H$_3$PO$_4$ can be effectively used to etch away the B.L. The micrographs in Figure 5.14 graphically illustrate the steps in B.L. etching. Until the 2$^{nd}$ minute of etching, there is almost no decipherable effect on the B.L., at the commencement of 2$^{nd}$ minute however B.L. starts to thin. At 2 min. 30 sec. spots revealing the underlying porous structure start to appear on the bottom surface. At 3$^{rd}$ minute most of the B.L. is gone and pores start to open up. The etching is finally complete at 3 min. 30 sec. when all the pores are fully opened up showing neatly ordered AAO pores of the underlying structure.
5.2 CdS planar thin films on conducting glass substrates

CdS planar thin films deposited on conducting glass substrates by d.c. electro-deposition were studied for effect of thermal treatments on their optical and physical properties. These characterizations were done by X-ray diffraction and UV-Vis spectroscopy. Electrical properties of such film based Schottky diodes were also studied. We summarize the results here as under.

5.2.1 Effect of thermal treatments

5.2.1.1 X-Ray Diffraction studies

The X-ray diffraction patterns obtained for CdS planar films grown by d.c. electro-deposition (8 Volts, 6 min.) and annealed in different ambients at 200 °C for 15 min. are shown in Figure 5.15 below. The intensity peak at 2θ≈28° refers to the hex-α phase of CdS. The secondary peak at 2θ≈10° can be attributed to the underlying conducting layer of Indium Tin Oxide (InSnO$_2$). Thus, it can be inferred that annealing in different ambients doesn’t affect the crystallographic properties of the CdS planar films.

![Figure 5.15: X-Ray Diffraction patterns for CdS thin films d.c. electrodeposited (8V, 6min.) on ITO coated glass substrates and annealed in different ambients at 200 °C for 15 min.](image-url)
5.2.1.2 UV-Vis Absorption Spectroscopy studies

The UV-Vis absorption spectroscopic studies reveal the relationship between the thermal treatments and the bandgap of the material synthesized. Films deposited on conducting glass substrates under identical conditions were treated in different ambients viz. Nitrogen, Argon and under vacuum for these studies. Figure 5.16 shows the variation in absorption spectra with wavelength for three cases annealed at 200 °C for 15 min. We observe that the point at which absorption starts to peak up (~ 490 to 500 nm) shifts to the right side as we move from Argon annealing to vacuum annealing with the values for Nitrogen annealing lying somewhere in between. This can be explained by the extent of oxidation that the films sustained while being thermally treated. Annealing in UHP grade Argon didn’t allow for any scope of oxidation hence the wavelength for absorption was the lowest in this case. Nitrogen in comparison had a little impurity of Oxygen while the vacuum oven was the worst case allowing a vacuum up to only 30 mTorr thus there was a lot of scope for the film to get oxidized, hence the tendency for the absorption spectra to shift towards the right.

![Figure 5.16: UV-Vis absorbance spectra of d.c. electro-deposited CdS thin films on ITO glass for thermal annealing treatments in various ambients @ 200 °C.](image-url)
The absorption spectra in Figure 5.16 were further used to calculate the bandgap using Tauc’s law [67-70]. Tauc’s relation allows one to predict the bandgap energy of an optical semiconductor by using the relation:

\[
(\alpha \times h \times \nu)^2 = (h \times \nu) - E_g
\]

Where, \(E_g\) is the bandgap energy, \(h\) is Planck’s constant and \(\nu\) is wave number and \(\alpha\) is referred to as the absorption coefficient and is computed using the relation:

\[
\alpha = \left(\frac{1}{t}\right) \times \ln\left(\frac{I_0}{I_t}\right)
\]

Here, \(t\) is the thickness of the sample, \(I_0\) is the intensity of light incident on the sample and \(I_t\) is the intensity of observed light after its transmission through the sample of thickness \(t\). The absorption spectrophotometer computes \(\log_{10}(I_0/I_t)\) for the range of wavelength specified by the user. This is presented as the absorbance in the Y-axis and hence this Y-axis data can be easily used to compute \((\alpha h \nu)^2\). These computations performed on the data presented in Figure 5.16 are shown in Figure 5.17. It was observed that with increasing extent of oxidation of the thin films the bandgap decreased progressively. This calculation of bandgap is shown in Figure 5.17 and clearly depicts the bandgaps for Argon annealed (3.95 eV), Nitrogen annealed (3.93 eV) and vacuum annealed (3.83 eV) CdS films all of which are significantly higher than the figures quoted for bandgap of CdS synthesized in the bulk regime (2.42 eV).

![Figure 5.17: Bandgap calculation for CdS films annealed in different ambients using Tauc's Law.](image)
Figure 5.18 and Figure 5.19 below show the absorption spectra and bandgap calculation respectively obtained for CdS film annealed in Nitrogen at two different temperatures. The graphs further support our theory that oxidation of CdS films decreases the bandgap energy. The shift towards the right in the absorption spectra is all too evident as in previous case and the bandgap is observed to decrease from 3.93 eV to 3.83 eV.

![Absorption Spectra and Bandgap Calculation](image)

**Figure 5.18:** UV-Vis absorbance spectra of d.c. electro-deposited CdS thin films after Nitrogen annealing at 200 °C and 300 °C.

**Figure 5.19:** Bandgap calculation using Tauc's Law for CdS d.c. electro-deposited films annealed in Nitrogen at different temperatures.
We further verify this by plotting the absorption spectra and bandgap calculations for CdS d.c. electro-deposited thin films annealed in UHP Argon at two different temperatures viz. 200 °C and at 300 °C. As before, the absorption spectra are observed to shift towards the right and the bandgap is observed to decrease from 3.95 eV (at 200 °C) to 3.83 eV (at 300 °C). The plots are shown in Figure 5.20 and Figure 5.21 in the subsequent pages.

![Absorbance Spectra of CdS Films](image)

**Figure 5.20:** UV-Vis absorbance spectra of d.c. electro-deposited CdS thin films after Argon annealing at 200 °C and 300 °C.

![Bandgap Calculation](image)

**Figure 5.21:** Bandgap calculation using Tauc's Law for CdS d.c. electro-deposited films annealed in Argon at different temperatures.
5.2.2 CdS-Au/Ni planar Schottky diodes on conducting glass substrates

CdS thin films were grown by d.c. electro-deposition on conducting glass substrates. The thicknesses of the films were varied by varying the duration of deposition while the grain sizes were varied by varying the supply voltage. The film thicknesses and grain sizes were characterized by scanning electron microscopy and the data thus obtained was compared to the optical properties of the deposited film. Bandgap calculations were also obtained from the UV-Vis absorption spectroscopy. Finally, the diodes formed were characterized by current-voltage analysis.

5.2.2.1 SEM Characterization

Figure 5.22: SEM micrographs showing different thicknesses of d.c. electro-deposited (8 Volts) CdS films obtained by varying duration of deposition: (a) 2 min. (b) 4 min. (c) 6 min. (d) 8 min. and (e) 10 min.
The SEM micrographs helped in the determination of the relationship between the thicknesses of film deposited with the variation in duration of deposition as well as the relationship between voltage of electro-deposition and the average grain sizes of deposited films.

Going by Faraday’s law of electrolysis, which states that “The mass of a substance produced at an electrode during electrolysis is proportional to the number of moles of electrons (the quantity of electricity) transferred at that electrode”; one would expect to observe the thicknesses of deposited films to linearly increase with duration of deposition. However, Figure 5.23 (summarizing observations from micrographs of Figure 5.22) shows no particular correlation between the two parameters. This may be attributed to the technique used for film thickness determination. FESEM technique used to determine the film thickness relies heavily on the skills of the operator for sample preparation. Since, these films were deposited on glass substrates, the glass cutting process, done for FESEM imaging purposes often damaged the CdS film. Hence, the measurements on film thicknesses weren’t very much reliable. The errors in the data obtained from the micrographs are hence incorporated in Figure 5.23. Stylus profilometry was also tried to measure the film thicknesses. But since, the films were un-annealed, they easily crumbled under the stylus pressure thereby rendering the profilometry data useless.

![Figure 5.23: Plot of film thickness vs. duration of electro-deposition.](image-url)
Usually one would expect the grain sizes to increase as the films are made thicker. Since, with increasing thicknesses, more material is available, which under normal processing techniques (carried out in elevated temperatures) has more opportunity to coalesce into bigger grains. But however, Figure 5.25 summarizing the measurements obtained from micrographs in Figure 5.24 illustrates a completely opposite phenomenon. It is observed that the grain sizes of CdS films actually decrease with increasing durations of deposition. A multitude of phenomena occurring at this point could be responsible for this behavior. Since, the depositions were done using potentiostatic means, the current densities kept varying throughout the interval of deposition. The exact value of current density that caused the deposition of the uppermost CdS layer hence will be responsible for the exact grain size as observed by the FESEM. In this case the currents ranged anywhere from 6 mA to 30 mA. Also there could be localized temperature fluctuations at the site of CdS deposition, because of occasional high current densities (which kept fluctuating, because of potentiostatic depositions) which may also affect the grain sizes considerably. Also, even though the grain sizes of the topmost films were very small for longer duration of depositions, the actual grain sizes of the underlying layers might be relatively bigger. Since, no FESEM based characterization was done on the grain sizes of these underlying layers, no conclusions about the variation of the actual average grain size (of the film as a whole) with duration of depositions could be drawn.

Figure 5.27 illustrates another important relationship between the applied voltage and grain size of deposited CdS thin film. It is observed that an increase in the applied voltage resulted in decrease of the average grain diameter of the deposited film. This is quite contrary to the usual perception that grain sizes should increase with corresponding increase in applied d.c. voltage, since the increasing potential should attract more CdS from the solution and force it to deposit on the cathode (corollary of Faraday’s law of electrolysis). Again this deviation from the usual behavior could be attributed to various factors like, potentiostatic anodizations which inherently meant varying deposition current densities, localized heating effects affecting grain sizes of the topmost layer and lack of FESEM imaging data on the underlying layers that might have given a better clue about the average grain size of the thin CdS film as a whole rather than just the topmost layer.
Figure 5.24: SEM micrographs showing different grain sizes of d.c. electro-deposited (8 Volts) CdS films obtained by varying duration of depositions: (a) 2 min. (b) 4 min. (c) 6 min. (d) 8 min. and (e) 10 min.

Figure 5.25: Plot of grain size vs. duration of deposition.
Figure 5.26: SEM micrographs showing different grain sizes of d.c. electro-deposited (6 min.) CdS films obtained by varying voltage of deposition: (a) 2 V (b) 4 V (c) 6 V (d) 8 V and (e) 10 V.

Figure 5.27: Plot of grain size vs. applied voltage of electro-deposition.
5.2.2.2 UV-Vis Absorption Spectroscopy studies

The variations in CdS film thicknesses with duration of deposition was reflected in the absorption spectra which showed higher values of absorbance at any given wavelength, with increasing film thicknesses. This is quite natural to expect since, increasing thicknesses meant that more material was available to absorb increasing number of photons hence, leading to higher values of absorbance. However, calculations performed for determination of optical bandgaps using Tauc’s law showed no observable trends in particular. The typical bandgap values obtained were 3.61 eV (2 min.), 3.90 eV (4 min.), 3.70 eV (6 min.), 3.94 eV (8 min.) and 3.87 eV (10 min.). The absorption spectra and the bandgap calculations are shown in Figure 5.28 and Figure 5.29 respectively. These differences in values of optical values could be attributed to only one structural property of the thin film namely, the grain sizes. But since, the exact relation between duration of deposition and grain sizes or film thicknesses and grain sizes are not known, owing to the factors as discussed in the previous section 5.2.2.1; a correlation can’t be drawn between optical bandgap and film thicknesses.

Plotting the absorption spectra for different applied d.c. voltages of electro-depositions, it was observed that the value of the absorbance obtained at a particular value of wavelength, increased with the applied voltage. This is very much expected, since larger values of voltage would have caused more CdS to deposit on the conducting substrate (corollary of Faraday’s law of electrolysis), and these thicker films would result in absorbance of more photons thereby increasing the net values of the absorbance. Typically one would expect to observe an increase in optical bandgap values with a corresponding decrease in the grain sizes. However, the calculations for determination of optical bandgaps using Tauc’s law showed no particular dependence on the grain sizes (which decreased with increasing voltages of depositions, see section 5.2.2.1). Typical bandgap values obtained were: 3.80 eV (2 Volts), 2.83 eV (4 Volts), 3.79 eV (6 Volts), 3.88 eV (8 Volts) and 3.66 eV (10 Volts). The observations are summarized in plots of Figure 5.30 and Figure 5.31 respectively. These deviations in the observed optical bandgap values can be very well explained if one has accurate data pertaining to average grain sizes of the CdS films. But, considering the factors discussed in section 5.2.2.1,
there is an acute lack of reliable data on grain sizes and hence, a correlation of grain sizes vs. optical bandgaps couldn’t be reached.

Figure 5.28: UV-Vis absorption spectra for d.c. electro-deposited CdS samples (8 Volts) for different durations.

Figure 5.29: Bandgap calculations using Tauc's law on CdS d.c. electro-deposited samples (8 Volts) for different durations.
Figure 5.30: UV-Vis absorption spectra for d.c. electro-deposited CdS samples (6 min.) for different applied voltages.

Figure 5.31: Bandgap calculations using Tauc's law on CdS d.c. electro-deposited samples (6 min.) for different applied voltages.
5.2.2.3 Current – Voltage Analysis

The current density – voltage graphs obtained for Schottky diodes fabricated on the above depositions (CdS d.c. electro-deposited on conducting glass substrates) are shown in Figure 5.32 to Figure 5.37. The graphs depict the variation in I-V with respect to film thicknesses and grain sizes in both dark and light conditions (~1 Sun). For any given diode (whether CdS-Au or CdS-Ni) it is observed that the current density obtained for a particular applied voltage increases with increasing film thickness and is true for both dark and light conditions owing to the fact that more material is available for absorbing the electrons injected with increasing thickness. A similar trend is observed when grain sizes are varied. With decreasing grain sizes, the current density increases owing to increasing tunneling effects among the CdS grains. This is also true for both dark and light conditions. For a given diode, the current density obtained in dark was observed to be more than that obtained for light conditions. The decrease in current density in light may be attributed to the increased recombination-generation effects that take place when the device is exposed to an external source of energy. For all CdS film based Schottky devices it was noted that the CdS-Au diode exhibited a greater current density than its CdS-Ni counterpart. This was attributed to the observation that a Nickel contact gets readily oxidized in atmosphere while the Gold surface doesn’t oxidize at all. And the oxide layer hence formed, being an insulator proves to be a hindrance to the flow of current in the device thus causing low current densities. Different device parameters calculated from the current-voltage graphs of the devices like the Diode Series Resistance ($R_s$), Diode Ideality Factor ($\eta$) and Reverse Saturation Current Density ($J_0$) for both Gold and Nickel diodes in dark and light conditions are tabulated in Table 5.1 and Table 5.2 at the end of this section.
Figure 5.32: Current density vs. Voltage curves in dark and light conditions for CdS-Au Schottky diodes on planar films for different film thicknesses.

Figure 5.33: Current density vs. Voltage curves in dark and light conditions for CdS-Au Schottky diodes on planar films for different grain sizes.
Figure 5.34: Current density vs. Voltage curves in dark and light conditions for CdS-Ni Schottky diodes on planar films for different film thicknesses.

Figure 5.35: Current density vs. Voltage curves in dark and light conditions for CdS-Ni Schottky diodes on planar films for different grain sizes.
Figure 5.36: Current density vs. Voltage graphs for CdS-Au and CdS-Ni Schottky diodes in dark and light conditions.

Figure 5.37: Current density vs. Voltage graphs in dark and light for Au and Ni contacts.
Table 5.1: Diode parameters for CdS-Au Schottky diodes on planar d.c. electro-deposited CdS films.

**Dark Curves**

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<th>Duration (in min.)</th>
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<th>Reverse Sat. Current Density (Amps./cm$^2$)</th>
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**Light Curves**

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Table 5.2: Diode parameters for CdS-Ni Schottky diodes on planar d.c. electro-deposited CdS films.

**Dark Curves**

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**Light Curves**

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5.3 CdS-Au/Ni Schottky diodes in AAO templates

CdS nanowires were grown in porous short-channel AAO membranes using two techniques: chemical bath deposition (CBD) and d.c. electro-deposition (ED). In both cases the diodes were characterized first by X-ray diffraction followed by scanning electron microscopy. Final characterization on good devices was done by current-voltage analysis. We summarize the results here as under.

5.3.1 CdS-Au/Ni Schottky diodes by Chemical Bath Deposition

5.3.1.1 X-Ray Diffraction studies

![XRD Pattern for CBD](image)

Figure 5.38: X-Ray Diffraction pattern obtained for CdS nanowires grown in short channel porous AAO templates by CBD.

The X-ray diffraction pattern for a typical CdS-Au Schottky diode made by chemical bath deposition is shown in Figure 5.38 above. The peak at $2\theta=44^\circ$ is for the residual Aluminum in the sample which constitutes the bulk part of the device. The peaks in between $2\theta=25^\circ$ and $2\theta=30^\circ$ show the phase of CdS nanowires grown. It is evident that since these nanowires were precipitated from a CdCl$_2$ based solution their phase obtained is hexagonal $\alpha$-form [71].
5.3.1.2 SEM Characterization

Figure 5.39: SEM micrographs of CdS nanowires grown in porous AAO membranes by chemical bath deposition: (a) top view (b) fractured cross section and (c) close-up of cross sectional view.

The SEM micrographs of CBD grown nanowires (as summarized in Figure 5.39 above) show some interesting structures. The cross-sectional images show a dense deposition of CdS nanoparticles (10-20 nm in size) inside the channels. Occasionally CdS nanowires can also be seen. However the deposition is not entirely uniform and at many locations inside the channel a void between consecutive particles can be observed, thereby making this sample unsuitable for further device fabrication. The reason for the existence of these voids can be explained if one observes the top view of the sample which shows a dense deposition of thick film of CdS (grain size 20 nm) uniformly covering all the pores from the top. Since, chemical bath deposition relies solely on gravity driven precipitation to make the nanowire and doesn’t have any force driven parameter (like the electric field for example in the d.c. electro-deposition case) to assist in the nanowire fabrication, the presence of this thick top layer of CdS covering the top acts as a barrier hindering the further deposition of CdS inside the channels. Thus chemical bath deposition is found to be an ineffective method to deposit CdS inside AAO templates. Hence, no Schottky devices were further fabricated on these substrates. The Schottky devices were fabricated on CdS nanowires grown in AAO templates using d.c. galvanostatic driven electro-deposition instead. The characterizations on these devices are reported in the subsequent sections.
5.3.2 CdS-Au/Ni Schottky diodes by Galvanostatic d.c. Electro-Deposition

5.3.2.1 X-Ray Diffraction studies

The X-ray diffraction pattern obtained for CdS-Au Schottky diode fabricated in short channel porous AAO membranes is showed in Figure 5.40 above. Like before in section 5.3.1.1, we note the peak at $2\theta=44^\circ$ corresponding to Aluminum substrate, the new peak observed at $2\theta=38^\circ$ here however corresponds to Gold. We also observe that since CdS like before was synthesized using a CdCl$_2$ bath (though in an organic solution of DMSO), the film obtained has a hexagonal $\alpha$-phase. Hence the conclusion that the structural crystallographic phase of CdS remains unchanged (i.e. hexagonal $\alpha$-phase in this case) with the technique employed to synthesize CdS (whether electro-deposition or chemical bath deposition) provided that one keeps the synthesis source the same.

5.3.2.2 SEM Characterization

The SEM micrographs obtained for CdS nanowires grown in short-channel AAO templates by galvanostatic d.c. electro-deposition (shown in Figure 5.41 below) shown some very interesting structures. The cross-sectional images (Figure 5.41 (b) and (c)) show densely filled AAO channels. No voids can be observed in between particles and
one can clearly distinguish solid CdS nanowires as deposited in the channels. The top surface (Figure 5.41 (a)) is very clean and the top of CdS nanowires can be observed as deposited in the AAO pores. No thick CdS layers are seen obstructing the access to underlying CdS nanowires as seen in the previous case of chemical bath deposited nanowires (section 5.3.2.1), thus making this an ideal platform to fabricate CdS nanowire based devices.

Figure 5.41: SEM micrographs of CdS nanowires grown in porous AAO membranes by galvanostatic d.c. electro-deposition: (a) top view (b) & (c) cross sectional views.

5.3.2.3 UV-Vis Absorption Spectroscopy studies

The UV-Vis absorption spectra obtained from CdS nanowires of diameters 10 nm and 25 nm, suspended in 85 wt.% H3PO4 solution are reproduced as such in Figure 5.42. It is observed that the absorbance at a given wavelength is higher for a 25 nm diameter CdS nanowire as compared to a 10 nm diameter nanowire. This behavior can be justified by the fact that the 25 nm diameter nanowire had more CdS than the 10 nm one, which accounted for more absorption of photons and hence, higher values of absorbance. There is however, no exact absorption band-edge visible for both. In both the cases, the absorption spectrum gradually starts to rise at 750 nm, which continues until the peak value is reached around 375 nm. This is very much expected as the concentration of CdS nanowires in the 85 wt.% H3PO4 solution is relatively small and hence, a clear absorption band edge is very difficult to obtain. A magnified plot of the absorption spectra of 10 nm diameter CdS nanowires (Figure 5.43) reveals another interesting
property. Instead of the usual smooth line spectra that one would expect to see (as in sections 5.2.1.2 and 5.2.2.2), the graph demonstrates widely distributed scattered data points. It’s theorized that even though the nanowires have the same crystallographic composition, their different orientations in the suspension will affect the way light is transmitted through the solution. Thus, resulting in a scattered absorption spectrum, quite contrary to the one observed for a thin film.

Figure 5.42: UV-Vis absorption spectra for CdS nanowires (dia. 10 nm and 25 nm) suspended in 85 wt.% H₃PO₄ solution.

Figure 5.43: Magnified UV-Vis absorption spectra for CdS nanowires (dia. 10 nm) suspended in 85 wt.% H₃PO₄ solution.
5.3.2.4 Current – Voltage Analysis

The current density vs. voltage graphs for the CdS-Au/Ni Schottky diodes fabricated inside porous AAO membranes show some very interesting characteristics. As we move from the bulk regime to the nanoscaled regime, important differences between the device characteristics and their electrical behavior become all too apparent. For a Schottky diode fabricated inside a 25 nm pore diameter AAO template, which can be considered as the bulk region, the current densities in dark conditions are higher than the current densities in light conditions (Figure 5.46 and section 5.2.2.3). However, in the nanoscale region, the light currents are observed to be higher than in the dark conditions (Figure 5.44). Also for a given metal contact (whether Au or Ni) in both dark and light conditions it was observed that the current densities obtained for Schottky diodes fabricated in the nanoscaled regime (10 nm pore diameter AAO template) were considerably higher than that obtained in the bulk regime (25 nm pore diameter AAO template) (Figure 5.48 and Figure 5.49). In the bulk region (i.e. 25 nm) while the current density obtained for CdS-Au diodes was observed to be higher than the current densities obtained for CdS-Ni diodes (Figure 5.47) the opposite was true in the nanoscale region (i.e. 10 nm) where the current densities for CdS-Ni diodes were considerably higher than the current densities obtained for CdS-Au diodes (Figure 5.45). This was consistent for both dark and light conditions. The device parameters obtained from the current density vs. voltage graphs are summarized in Table 5.3 and Table 5.4 at the end of this section.
Figure 5.44: Current density vs. Voltage graphs for CdS-Au and CdS-Ni diodes in AAO templates (10 nm pore dia.) in dark and light conditions.

Figure 5.45: Current density vs. Voltage graphs in dark and light conditions for CdS-Au and CdS-Ni diodes in AAO templates (10 nm pore dia.).
Figure 5.46: Current density vs. Voltage graphs for CdS-Au and CdS-Ni diodes in AAO templates (25 nm pore dia.) in dark and light conditions.

Figure 5.47: Current density vs. Voltage graphs in dark and light conditions for CdS-Au and CdS-Ni diodes in AAO templates (25 nm pore dia.).
Figure 5.48: Current density vs. Voltage graphs in dark and light conditions for CdS-Au diode in AAO templates with pore diameters 10 nm and 25 nm.

Figure 5.49: Current density vs. Voltage graphs in dark and light conditions for CdS-Ni diode in AAO templates with pore diameters 10 nm and 25 nm.
Table 5.3: Diode parameters for CdS-Au Schottky diodes on d.c. electro-deposited CdS nanowires in porous AAO.

<table>
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<tr>
<th>Pore Diameter</th>
<th>Dark Curves</th>
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<tr>
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<td>Series Resistance (Ohms)</td>
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<table>
<thead>
<tr>
<th>Light Curves</th>
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<tbody>
<tr>
<td>Duration</td>
</tr>
<tr>
<td>10 nm</td>
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<tr>
<td>25 nm</td>
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</tbody>
</table>

Table 5.4: Diode parameters for CdS-Ni Schottky diodes on d.c. electro-deposited CdS nanowires in porous AAO.

<table>
<thead>
<tr>
<th>Pore Diameter</th>
<th>Dark Curves</th>
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</thead>
<tbody>
<tr>
<td></td>
<td>Series Resistance (Ohms)</td>
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<td>1249.038</td>
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<tr>
<td>25 nm</td>
<td>10245.63</td>
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<table>
<thead>
<tr>
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<tbody>
<tr>
<td>Duration</td>
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<tr>
<td>10 nm</td>
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<td>25 nm</td>
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6. Conclusions and Scope for Future Work

An optimal way to produce thick (60 µm) nanoporous anodic alumina membranes with pore widths ranging from 55 nm to 15 nm was investigated using galvanostatic means of anodization at different temperatures. Investigations were also carried out on automated voltage ramping and chemical etching using 85 wt.% phosphoric acid to evaluate their suitability as means for removal of barrier layer from the bottom of anodic alumina membranes. It was observed that chemical etching at elevated temperatures was by far the best technique to eliminate the issue of barrier layer completely. Complete barrier layer removal was achieved when templates were floated in 85 wt.% phosphoric acid solution kept at 45 °C.

We report a high bandgap of CdS (~3.95 eV) when synthesized in the nanoscale realm by potentiostatic d.c. electro-deposition on conducting glass substrates. The grain sizes of these films were found to decrease with increasing duration of depositions and increasing applied voltages. The optical bandgaps of these films calculated using Tauc’s law were found to vary from 2.83 eV to 3.95 eV, all of which are significantly higher than the figures quoted for bulk CdS (2.42 eV).

Two techniques namely, chemical bath deposition and galvanostatic d.c. electro-deposition were investigated for their suitability as means to fabricate CdS nanowires inside porous alumina membranes. While no discrepancy in the crystallographic structure was decipherable for CdS fabricated by either of the techniques (both were hexagonal α-form), the substrates with electro-deposited CdS were chosen for fabrication of Schottky diodes owing to more uniform deposition, dense filling of pores and availability of a clean top surface. Optical characterization by UV-Vis absorption spectroscopy showed higher values of absorbance for the 25 nm diameter CdS nanowire as compared to the 10 nm diameter CdS nanowire. However, the absorption spectra couldn’t be used for determination of optical bandgaps as no clear band-edges were visible. The scattered data points in the absorption spectra (instead of the usual smooth curve, as obtained for CdS thin films) were attributed to the ever-changing orientations of CdS nanowires in the suspension. The electrical properties of Schottky devices with Gold and Nickel hence fabricated were investigated by current-voltage analyses.
As a future exercise, additional investigations need to be carried out to determine exact film thicknesses of CdS films deposited on conducting glass substrates by d.c. electro-depositions. This would assist in establishing the relationship between durations of deposition and thicknesses of deposited films. Also, the relationship between grain sizes and durations of deposition need to be established. Instead of potentiostatic, galvanostatic d.c. electro-depositions could be investigated for depositing CdS thin films with better uniformity of grain sizes. To obtain better current density vs. voltage curves on CdS thin films based Schottky diodes fabricated on conducting glass substrates, longer durations of depositions could be investigated. Also, the films may be annealed in Argon ambient for 1 hour, both after film deposition and deposition of contact, to result in better metal – semiconductor junctions. More data on the UV-Vis absorption would be helpful in determination of reliable values of bandgap energies for CdS nanowires with different diameters. This could be obtained by dissolving more AAO templates with as deposited CdS nanowires in 85 wt.% phosphoric acid solution at elevated temperatures.

CdS grown in insulated porous alumina membranes being nanoscaled and possessing higher bandgap energies which can be custom-tailored by varying the physical dimensions, serve as a novel platform for potential applications in the realms of field emission devices, especially either as field emission transistors (created from CdS nanoribbons obtained by growing aligned CdS nanowires) or field emission display devices.
Appendix

Screenshots of the LabVIEW program for anodization automation are shown below.
References


Vita

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