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A SINGLE-PHASE DUAL-OUTPUT AC-DC CONVERTER WITH HIGH QUALITY INPUT WAVEFORMS

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ABSTRACT OF THESIS

A SINGLE-PHASE DUAL-OUTPUT AC-DC CONVERTER WITH HIGH QUALITY INPUT WAVEFORMS

A single-phase, buck-boost based, dual-output AC-DC converter is studied in this thesis. The converter has two DC outputs with opposite polarities, which share the same ground with the input power line. The power stage performance, including the input filter, is studied and procedure to select power components is given. The circuit model is analyzed to develop appropriate control. Zero-crossing distortion of the source input current is addressed and a solution is proposed. Experimental results are satisfactory in that a high power factor line current results for steady-state operation.

Keywords: single-phase PFC, AC-DC converter, buck-boost converter, dual output converter, zero-crossing distortion

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A SINGLE-PHASE DUAL OUTPUT CONVERTER WITH HIGH QUALITY INPUT WAVEFORMS

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THESIS

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The Graduate School
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2003

A SINGLE-PHASE DUAL OUTPUT CONVERTER WITH HIGH QUALITY INPUT WAVEFORMS

THESIS

A thesis submitted in partial fulfillment of the requirements
for the degree of Master of Science in Electrical Engineering in the
College of Engineering at the University of Kentucky

By

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Lexington, Kentucky

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Lexington, Kentucky

2003

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I thank my parents and sister for their forever love. And, thanks are extended to my friends, both in China and in the United States, for their support.

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TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

LIST OF FILES

1. Introduction

1.1 Background

With very few exceptions, distribution of electric power is in AC format. AC-DC conversion at the end-use point is a necessary operation in many applications. The need for DC power may be ancillary, such as use in electronic controls, or primary, such as the DC link of a motor drive. Until about fifteen years ago, all AC-DC power conversion utilized a circuit similar in principle to that shown in Figure 1.1 composed of a diode bridge and bulk capacitor. Inherently, the circuit draws pulse current from source line. The pulsating current results in a low total power factor and a high RMS line current. The line voltage, output voltage, and the source current are shown in Figure 1.2.

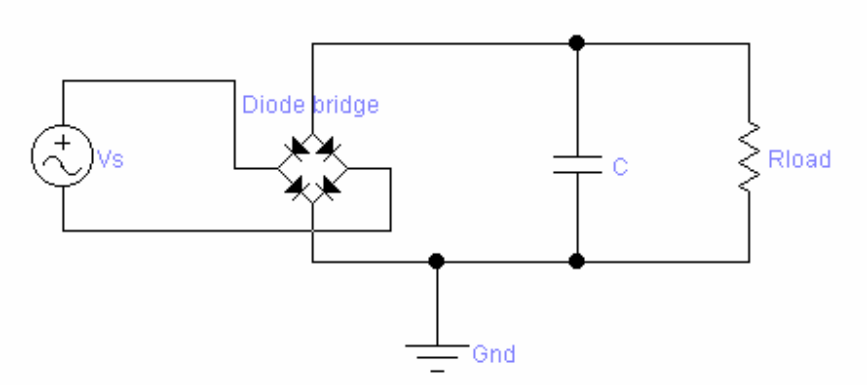


Figure 1.1 Power supply composed of diode bridge and bulk capacitor

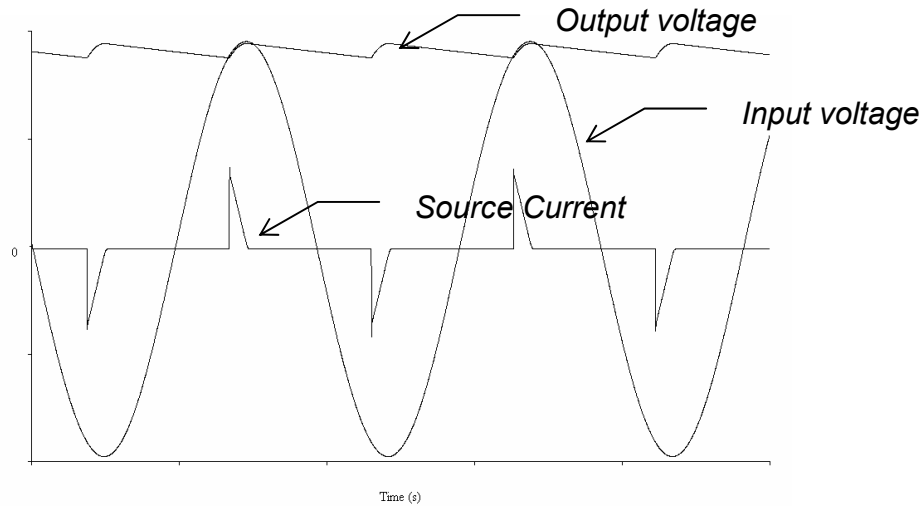


Figure 1.2 Line voltage, output voltage, and source current

In order to meet ever-increasing EMC standards and power quality recommendations on conducted harmonics for power supplies, numerous power factor correction (PFC) topologies for the AC-DC rectifier have been proposed. Figure 1.3 shows a typical two stage AC/DC PFC power supply with sinusoidal input current in phase with line voltage. The two stage PFC converter has shown superior performance. Its sinusoidal line current can satisfy any regulations. It is suitable to operate with universal line voltage. It can be designed for good hold-up time. However, this typical configuration uses two converters. The energy is processed twice. So, its cost, size, and efficiency are penalized. [1]

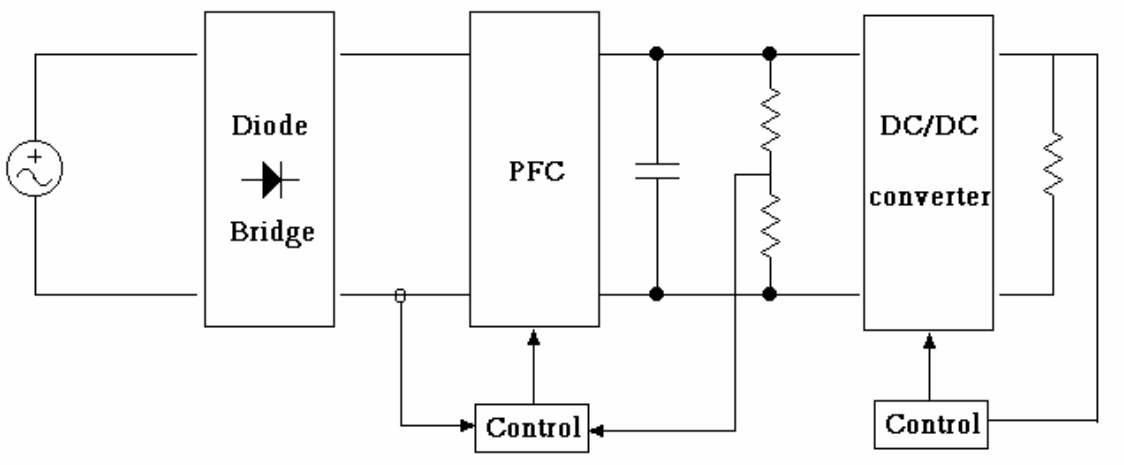


Figure 1.3 Typical two stage PFC converter

To offer a compromise between performance and cost, many single-stage power factor correction topologies have been proposed[2][3]. Among those circuits, the boost type converter is the dominant topology due to its inherent advantages, such as grounded transistor, continuity of input current, and its simplicity. PFC circuits based on flyback converter[4][5], SEPIC[6], and Cuk[7] topologies are also studied, but not to the extent as the boost converter.

1.2 Problem definition

When we began to study the topologies, we wanted to find a suitable scheme to build a solid-state distribution transformer, which has no wound core transformers in it. Its input voltage is either 2400 or 7200 volts, and the output is 120/240 volts. Standard practice safety consideration dictates that both the input and output of a distribution transfer must be grounded.

Figure 1.4 shows the commonly used single-stage AC-DC PFC circuit. In this circuit, input line voltage is rectified into a positive pulsating voltage with a ripple frequency of two times the line input supply. Then, the power factor correction circuit and DC-DC converter produce a DC voltage with little AC line current harmonics. However, unless an isolation transformer is introduced between the AC source and the rectifier, either only the load, or only the source can be grounded.

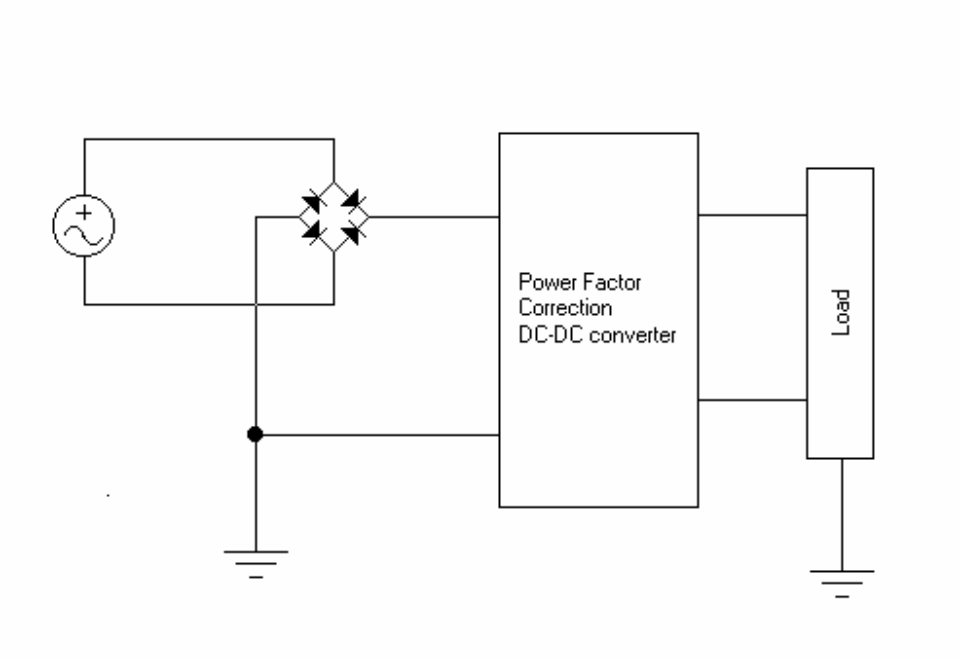


Figure 1.4 Full-bridge AC-DC Power Factor Correction Circuit

In our specific application, the half-bridge rectifier offers a solution to solve the grounding requirement without use of a wound core transformer. Figure 1.5 shows the configuration selected to solve this problem. Two single-stage power factor correction DC-DC converters are used to produce two DC output voltages with opposite polarity, but sharing the same ground with the AC supply.

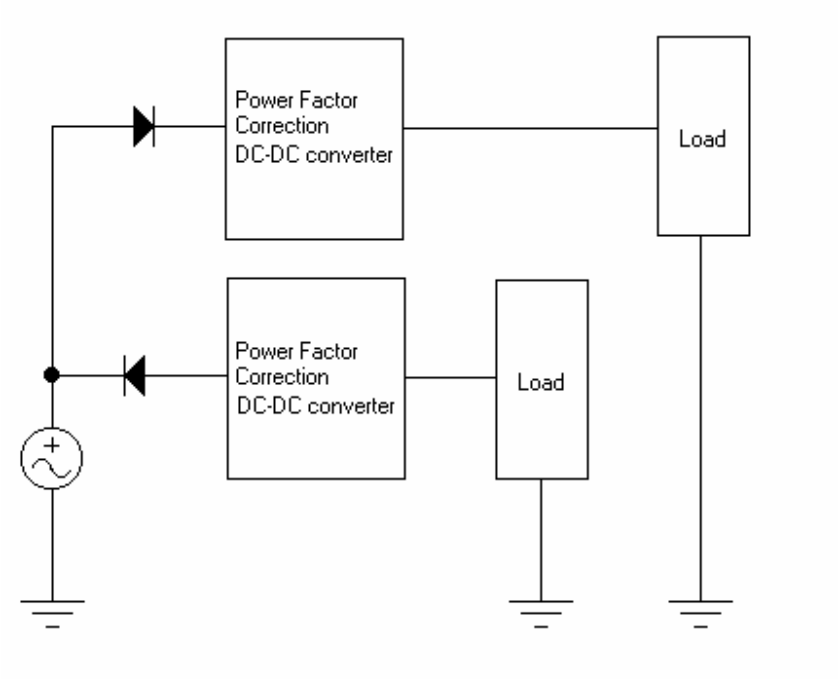


Figure 1.5 Half-bridge AC-DC Power Factor Correction Circuit with outputs sharing same ground with the power supply

Each one of the two power factor correction DC-DC converters is active only over a half cycle of the line supply. One works when the input voltage is positive and the other works when the input voltage is negative. In principle, a realization could be built based on any one of the three basic DC-DC converter topologies: buck converter, boost converter, or buck-boost converter. However, the discussion that follows will justify the buck-boost topology as the preferred choice.

1.2.1 Boost type half-bridge AC-DC power factor correction circuit

Figure 1.6 shows a feasible boost type half-bridge AC-DC power factor correction circuit. Diode D1, D2, switch Q1, inductor L1, and capacitor C1 comprise the basic DC-DC boost converter with positive output voltage across capacitor C1. While, D3, D4, Q2, L2, and C2 form another DC-DC boost converter with negative output voltage across capacitor C2.

The boost converter is the dominant topology in power factor correction. A large quantity of papers has been published pertaining this topology and different kinds of its variations [2][3].

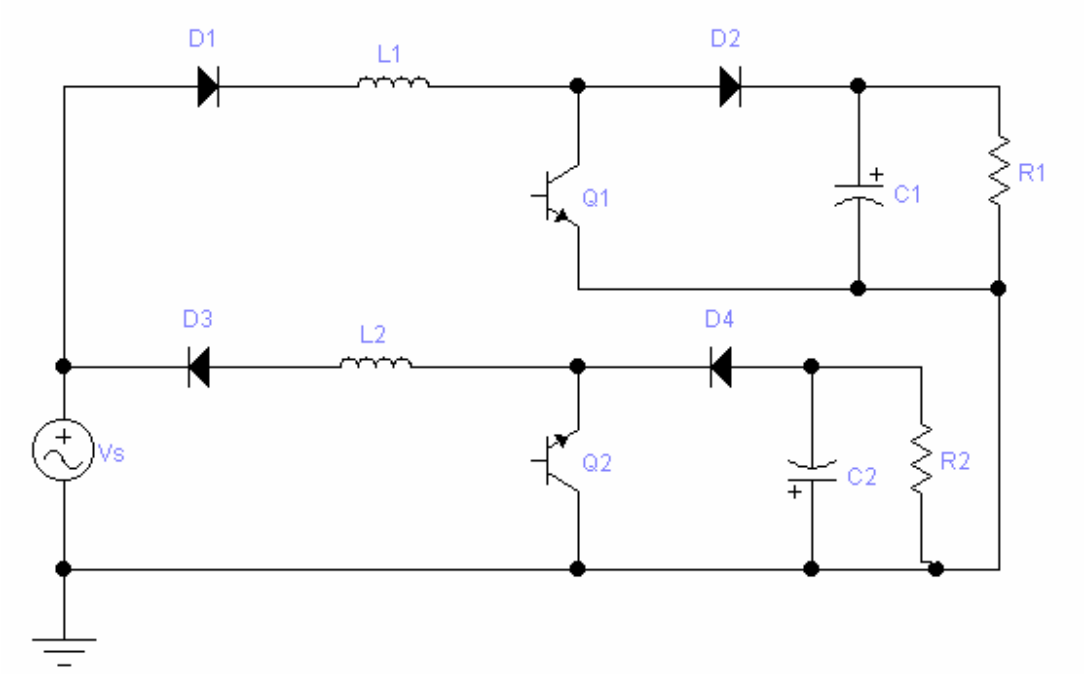


Figure 1.6 Boost type half-bridge AC-DC PFC circuit with dual output

In the boost converter, the inductor is in series with the ac line input. In continuous conduction mode, source current is naturally continuous, and has much less current ripple than other two topologies. For both the buck and buck-boost converters, the source currents are inherently discontinuous. Consequently, the boost converter performs satisfactorily with an input filter that uses smaller inductor and capacitor values than required by either the buck or buck-boost converters. It is widely used in both academic research and commercial products [8], [9].

However, the boost converter produces an output voltage higher than its input. An output voltage lower than the input is preferred. Another DC-DC converter is used to step down the high DC voltage, but the configuration would

then be the undesired two-stage topology with associated cost and efficiency penalties. For our specific case of a single-stage converter, if a 2400/120/240 distribution transformer is supposed to be built, and if a single-stage boost style converter is used, the DC voltages will be $2400 \times \sqrt{2}$ = 3394V. This imposes high voltage stress on the bulk capacitor. And, to obtain 120/240 V AC voltages from the final inverter stage, the modulation index of the inverter would be below 0.07. Such a small modulation ratio would be almost impossible to implement with acceptable accuracy.

1.2.2 Buck type half-bridge AC-DC power factor correction circuit

Figure 1.7 shows a possible buck type half-bridge AC-DC power factor correction circuit. Diode D1, D2, switch Q1, inductor L1, and capacitor C1 comprise the basic DC-DC buck converter with positive output voltage across capacitor C1. D3, D4, Q2, L2, and C2 form another DC-DC buck converter with negative output voltage across capacitor C2. When input supply voltage is positive, switch Q1 is active transferring energy to inductor L1 and capacitor C1. Conversely, input AC voltage is negative, switch Q2 is active transferring energy to L2 and C2.

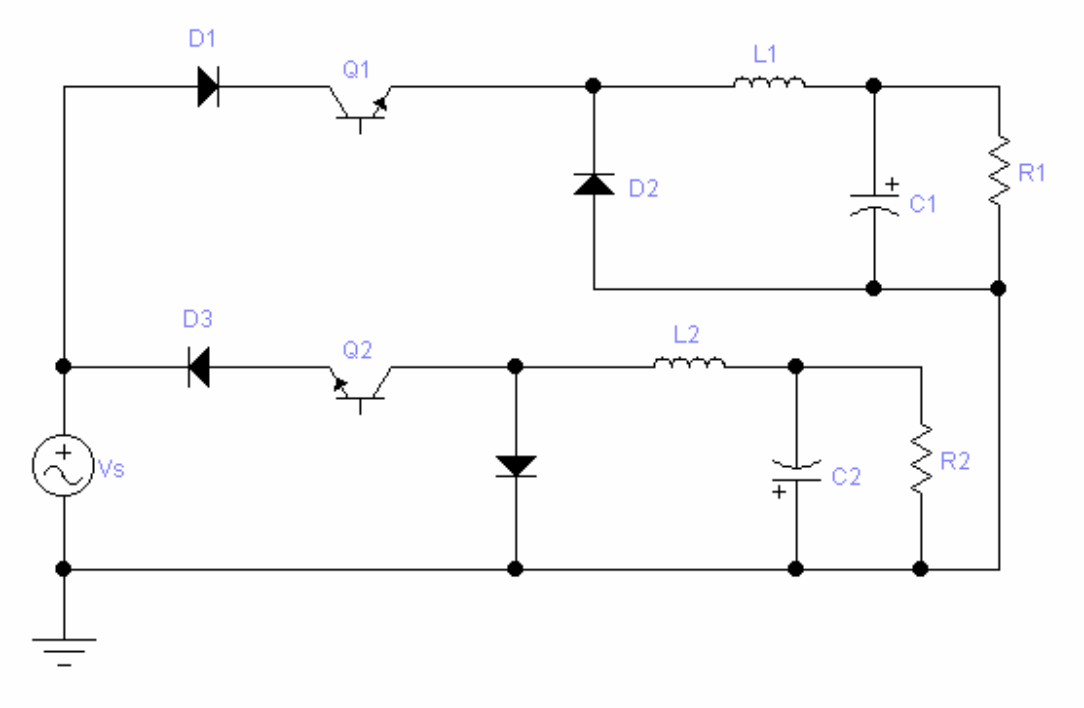


Figure 1.7 Buck type half-bridge AC-DC PFC circuit with dual output

The output voltage of a buck converter is lower than its input. Thus, a buck type AC-DC converter is feasible in our application from the viewpoint of providing lower output DC voltages. However, for a buck-type AC-DC converter, when the absolute value of input AC voltage is lower than the absolute value of its output, energy can not be transferred from the power source.

Figure 1.8 shows the source AC voltage, output voltage, and inductor current in a buck-type AC-DC converter. Switches can only conduct when the input voltage is higher than the voltages across the output capacitors. Figure 1.9 illustrates the source voltage, output voltage, and source current in a buck-type AC-DC converter after addition of an input LC filter to yield some improvement in the input current. However, there is still a “dead band” in the input current that leads to significant lower-order harmonics.

To solve this problem, some researchers added additional switches to make the circuit work as a boost converter when the input line voltage is lower than the

output voltages[10]. Katsuya Hirachi and Mutsuo Nakaoka applied pulse area modulation control scheme to shape the input current into sine wave and eliminate the output voltage ripple[11]. These methods require additional devices to maintain sinusoidal input current, and thus, increase the cost and complication of control. Further, there is a decrease in the efficiency of the system.

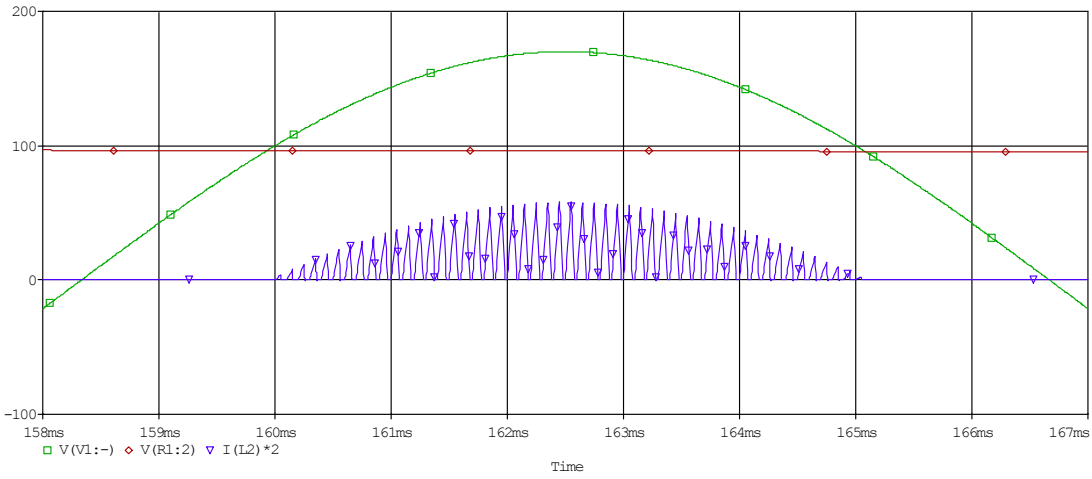


Figure 1.8 Source voltage, output voltage, and inductor current in buck type AC-DC converter

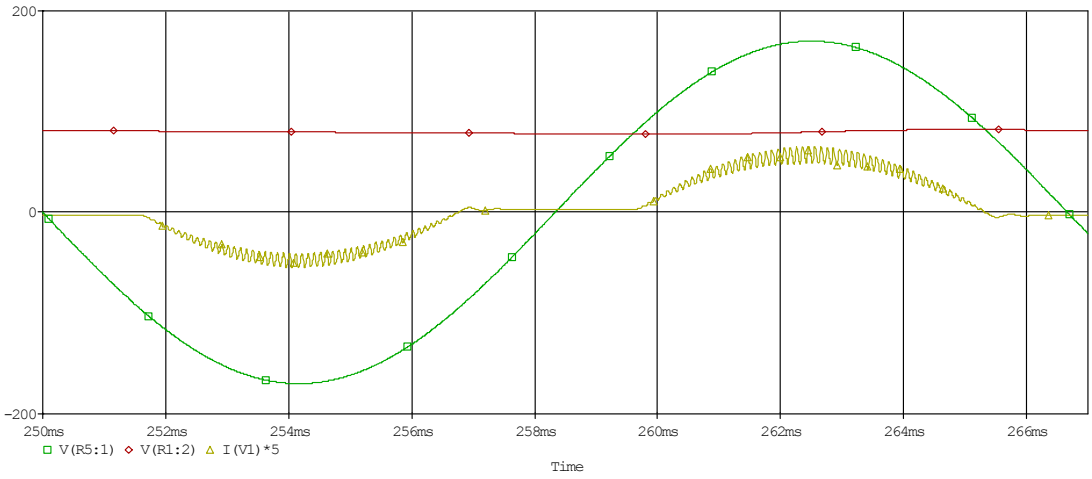


Figure 1.9 Source voltage, output voltage, and source current after filter in buck type AC-DC converter

1.2.3 Buck-boost type half-bridge AC-DC power factor correction circuit

Figure 1.10 shows a buck-boost type half-bridge AC-DC power factor correction circuit. Diode D1, D2, switch Q1, inductor L1, and capacitor C1 comprise the basic DC-DC buck-boost converter with negative output voltage across capacitor C1. D3, D4, Q2, L2, and C2 form another DC-DC buck-boost converter with positive output voltage across capacitor C2. When the input supply voltage is positive, switch Q1 is active transferring energy to inductor L1 and capacitor C1. While input AC voltage is negative, switch Q2 transfer energy to L2 and C2.

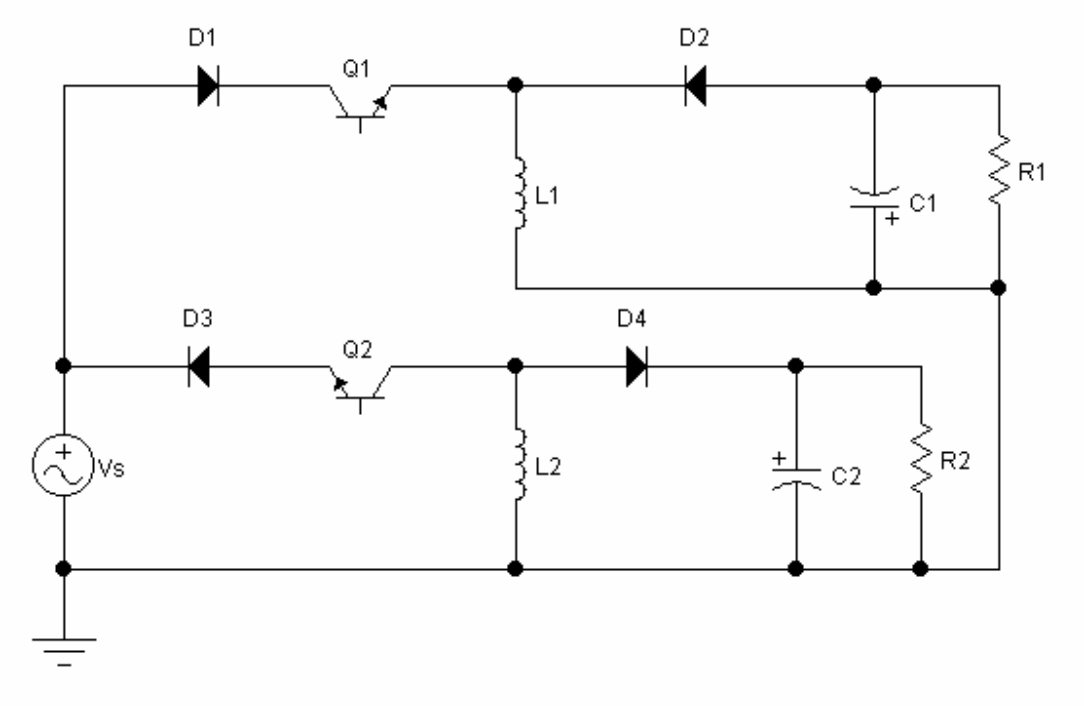


Figure 1.10 Buck-boost type half-bridge AC-DC PFC circuit with dual output

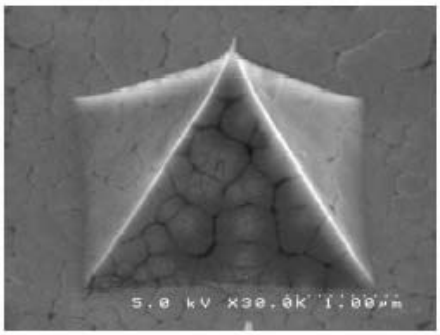
Output voltage of buck-boost converter can be higher or lower than its input. And, there is no “dead-area” in source current in the regions of zero crossing. Thus, the buck-boost type AC-DC converter is suitable in our application as it does not have the fundamental fallacies present with the boost and buck converters. Since the buck-boost converter satisfies the necessary fundamental

principles, the balance of the problem is one of designing proper control to meet performance requirements.

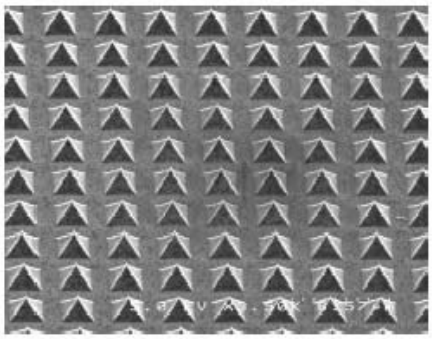
1.2.4 Other considerations

In high power application, efficiency is another important factor to be considered. To minimize the power losses, it is good to use as few as switching devices as possible, to use better devices with smaller on-state resistance, and to minimize the times energy is transferred between storage devices. If boost type AC-DC converter is used, normally, a step-down DC-DC converter is necessary to convert high voltage to low voltage. That means another time of energy transfer, thus, more power losses in switching and storage devices.

Most power electronics switches become short-circuit when they fail. So, normally for safety consideration, a transformer is used to provide necessary isolation between an input supply and the end-use load. Fortunately, over the last two decades, a very promising material, chemical vapor deposition (CVD) diamond, has been studied by many institutions and companies. It has numerous attractive physical and electrical properties that make it very useful in electronic application, such as its wide band gap, low or negative electron affinity, strong crystal structure, high electrical breakdown field, radiation hardness, and high thermal conductivity [12] [13]. And, when the device fails, it shows very high impedance, or it is open-circuit. Thus, this kind of device may provide necessary isolation for power electronic devices. Consequently, CVD diamond electric devices are very promising in power electrics application. Figure 1.11 shows SEMs of diamond microelectrode with single diamond microtip and an array of diamond microtips.



SEM of Diamond Microelectrode with a Diamond Microtip



SEM of Diamond Microelectrode with an Array of Diamond Microtips

Figure 1.11 CVD diamond microtip and array of diamond microtips

1.3 Operation of the power factor correction circuit

Two well-known, but different, control methods are available for power factor correction: hysteretic inductor current control [14], and constant-frequency pulse width modulation (PWM) inductor current control [15]. Constant-frequency PWM inductor current control has the advantage of constant harmonic frequency for both source and output, so that filter design is simplified.

In this thesis, the buck-boost type power factor correction circuit with constant-frequency PWM inductor current control is discussed. Figure 1.12 shows negative output portion of the buck-boost type, half-bridge power factor correction (PFC) circuit, along with the functional block diagram of its independent controller. This circuit rectifies over the positive value of source voltage V_s. The other half of the circuit, that is not shown, has the diodes and transistor reversed to rectify when the AC input is negative. It produces an output voltage of opposite polarity.

In Figure 1.12, output dc voltage (V_o) is scaled down and compared with desired DC reference voltage (V_{ref}). Output of the Error Amplifier (v_E) is the error signal between the fixed DC reference voltage and actual DC output. Sensed

source voltage (V_s) is scaled down and multiplied with the output of the voltage loop compensation circuit. The product of the two voltages is used as the source current reference. The source current is sensed by a Hall-effect current transducer and controlled to follow its current reference by a PID controller. If the output voltage drops, the error signal will increase. Thus, the current reference will be increased. The increased current reference will cause the output of the current PID to increase, thus increase the PWM duty cycle for the switch. A detailed analysis of the controller operation is presented in Chapter 3.

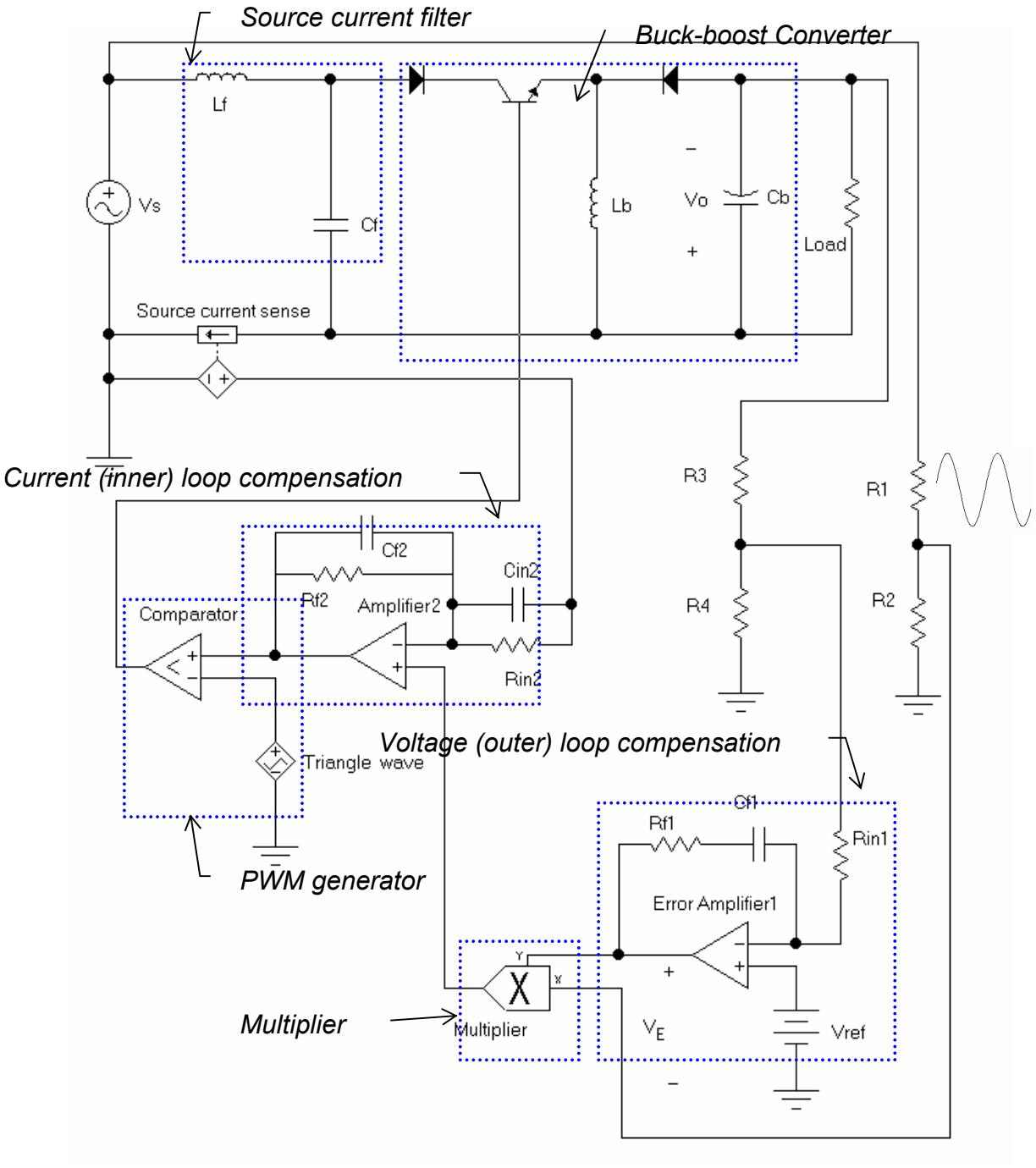


Figure 1.12 Functional diagram of buck-boost type half bridge DC output Power Factor Correction Circuit

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2. Main circuit Analysis and design

Due to symmetry and independence of the two half-bridge converters, complete understanding of the power level signals of the buck-boost converter results from analysis of the AC half-bridge buck-boost converter shown in Figure 2.1. The L_f-C_f filter components of Figure 1.12 are sized so that L_f offers a low impedance at source frequency. And, the voltage drop across diode D1 should be negligible compared with the voltage of the source. Thus, the converter input voltage over the positive half cycle is approximately equal to the source voltage. The source voltage and the converter input voltage are illustrated in Figure 2.2.

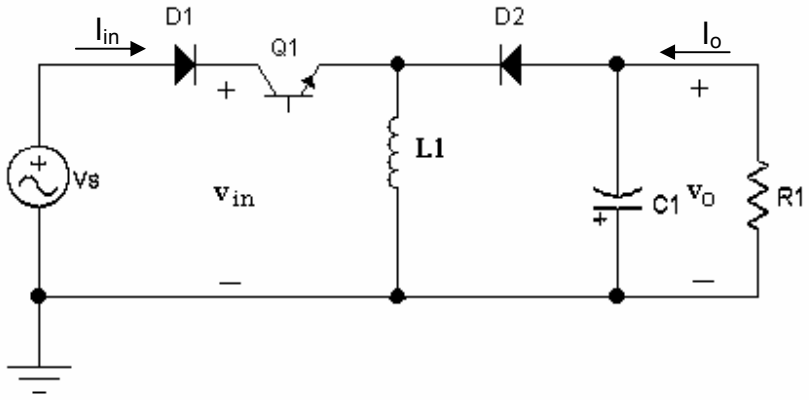

Figure 2.1 AC-DC half-bridge buck-boost converter

For the positive half cycle of the power supply, the rectified voltage (v_{in}) is positive, and Q1 switches on and off according to its gating signal determined by the PFC controller. During the negative half cycle of the power supply, the rectified voltage is zero, and Q1 remains off. In our analysis, we make the following assumptions:

(1) Diodes, switch, inductor, and capacitor are ideal components.

(2) Switching frequency f_s is much higher than AC line frequency f, so that over a switching period, the rectified line voltage, v_{in}, can be considered constant.

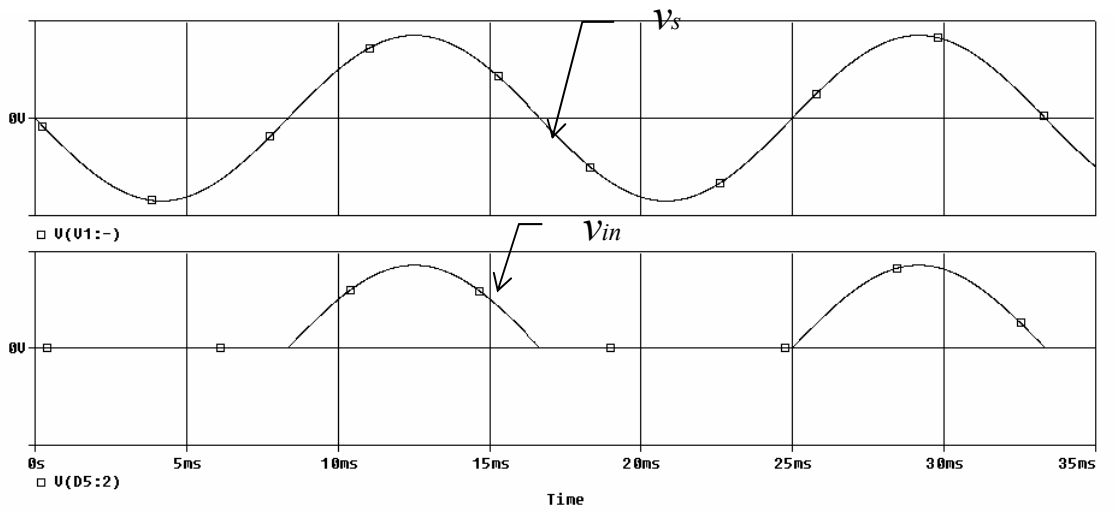

Figure 2.2 Source and rectified voltages in AC-DC buck-boost converter

According to the nature of the current through the inductor, the circuit can work in discontinuous conduction mode (DCM) or continuous conduction mode (CCM). In DCM, current through the inductor is discontinuous for each switching period over the complete positive half cycle of the power supply. In CCM, we assume that the current through the inductor is continuous all the time in the positive half cycle. We will analyze the circuit for these two different modes.

2.1 Discontinuous conduction mode analysis

If inductor L_1, switching frequency f_s, and load current I_o are small enough, the buck-boost converter will work in discontinuous conduction mode. Specifically, the inductor current goes to zero in every switching cycle and its

stored energy is completely transferred to the output before next time the switch Q_1 is on.

2.1.1 Duty cycle

Figure 2.3 shows the converter input voltage v_{in} and the inductor current i_L in discontinuous conduction mode. Even when the input voltage is in its peak value, current through the inductor is discontinuous.

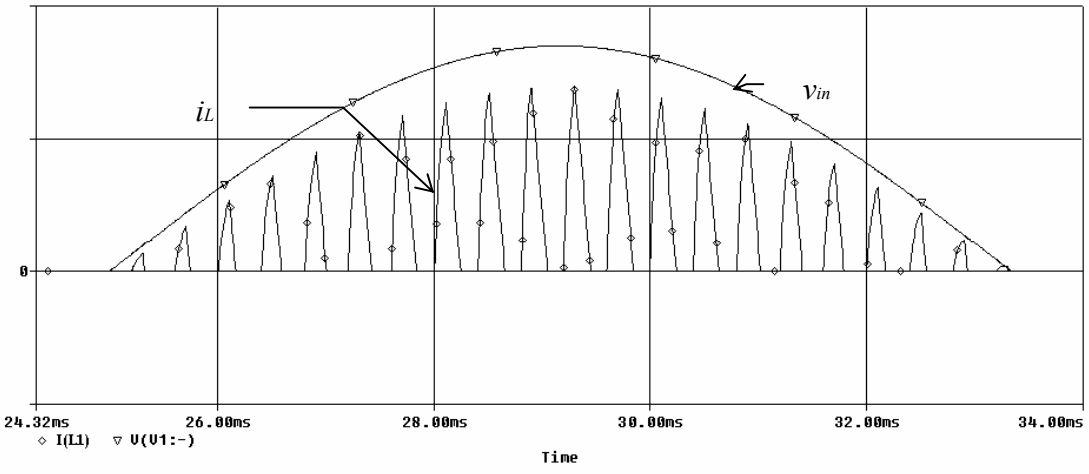

Figure 2.3 Converter input voltage and inductor current

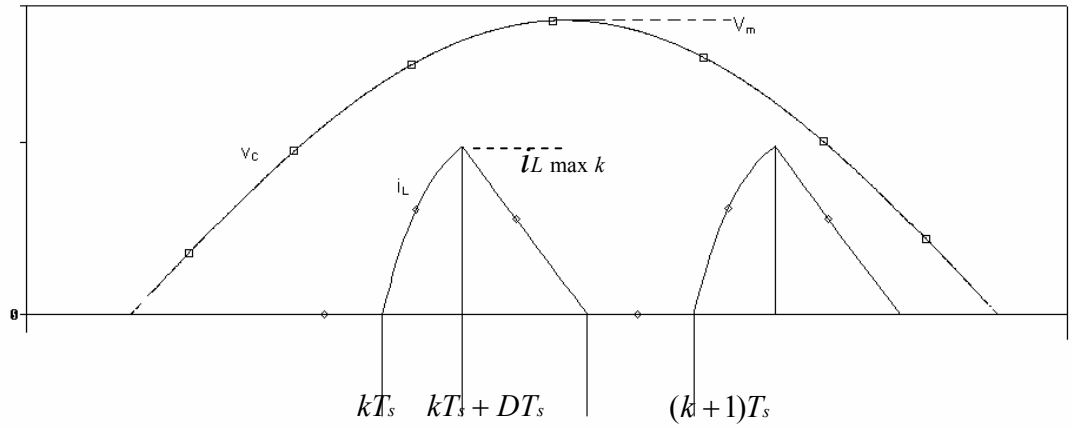

Figure 2.4 Inductor current in discontinuous mode

Figure 2.4 shows the inductor current for an arbitrary switching period where D is the duty cycle of the switch. When the switch is on, the inductor current is

$$i_L(t) = \frac{1}{L_1}\int_{kT_s}^{t} V_m \sin(\omega\tau)\,d\tau$$

$$= \frac{V_m}{\omega L_1}(\cos k\omega T_s - \cos \omega t) \qquad (2.1.1)$$

where $T_s = \frac{1}{f_s}$ is the switching period, V_m is the peak value of the source voltage, and $\omega = 2\pi f$ is the angular frequency of the source voltage.

The maximum value of $i_L(t)$ during the k_{th} switching cycle is

$$i_{L\max k} = i_{L1}((k+D)T_s)$$

$$= \frac{V_m}{\omega L_1}[\cos k\omega T_s - \cos \omega (k+D)T_s]$$

$$= \frac{V_m}{\omega L_1}[\cos(k\omega T_s) - \cos(k\omega T_s)\cos(\omega DT_s) + \sin(k\omega T_s)\sin(\omega DT_s)] \qquad (2.1.2)$$

Since switching frequency is much higher than the source frequency, $\omega DT_s \to 0$. Thus, $\cos(\omega DT_s) \to 1$, and $\sin(\omega DT_s) \to \omega DT_s$. Using these approximations, Equation 2.1.2 can be written as

$$i_{L\max k} = \frac{V_m}{L_1} DT_s \sin(k\omega T_s) \qquad (2.1.3)$$

where, $1 \le k \le \frac{f_s}{2f} = \frac{T}{2T_s}$

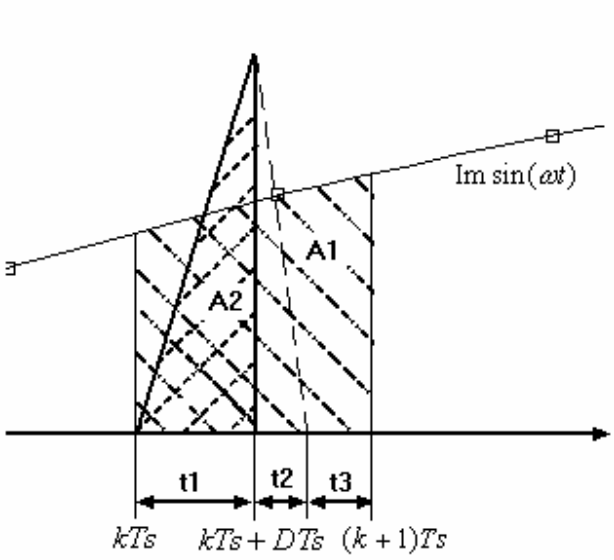

Figure 2.5 Area under the source current in a switching cycle is equal to the area under the switch current

Figure 2.5 shows the reference in phase component of source current along with the switch current pulse in a typical discontinuous switching cycle. $t1$ is the time period in which the switch is on, $t2$ is the time period in which the switch is off, and, $t3$ the time interval in which the inductor current is zero. According to the Equal Area Criterion [1][2], the discontinuous current pulse contains the same amp-second area as that of the reference input current for each switching period. The two areas A1 and A2 are determined and equated.

$$A1 = \frac{1}{T_s}\int_{kT_s}^{(k+1)T_s} \mathrm{Im}\sin(\omega\tau)d\tau \qquad (2.1.4)$$

$$A2 \approx \frac{1}{T_s}(\frac{1}{2})(DT_s)(\frac{V_m}{L_1}DTs\sin(k\omega T_s) \qquad (2.1.5)$$

So,

$$\frac{1}{T_s}\int_{kT_s}^{(k+1)T_s} \mathrm{Im}\sin(\omega\tau)d\tau = \frac{1}{T_s}(\frac{1}{2})(DT_s)(\frac{V_m}{L_1}DT_s\sin(k\omega T_s))$$

or,

$$\frac{\mathrm{I_m}}{\omega}[\cos(k\omega T_s) - \cos(k\omega T_s)\cos(\omega T_s) + \sin(k\omega T_s)\sin(\omega T_s)]$$

$$= \frac{V_m}{2L_1} D^2 T_s{}^2 \sin(k\omega T_s) \qquad (2.1.6)$$

Since $\omega T_s \to 0$, we get $\cos(\omega T_s) \to 1$, and $\sin(\omega T_s) \to \omega T_s$. Thus, Equation 2.1.6 can be written as

$$\mathrm{I_m} T_s \sin(k\omega T_s) = \frac{V_m}{2L_1} D^2 T_s{}^2 \sin(k\omega T_s) \qquad (2.1.7)$$

Solving 2.1.7 for the duty cycle yields

$$\mathrm{D} = \sqrt{\frac{2\,\mathrm{I_m} L_1}{V_m T_s}} \qquad (2.1.8)$$

Assume that unity power factor control is achieved, and that the magnitudes of the output voltages and the loads of both the half-wave converters are equal, then the total input and output powers are respectively

$$P_{in} = \frac{\mathrm{I_m} V_m}{2} \qquad (2.1.9)$$

$$P_o = 2 I_o V_o \qquad (2.1.10)$$

where, V_o and I_o are the DC voltage and load current of the two identical DC outputs.

From Equation 2.1.9 and 2.1.10

$$\mathrm{I_m} = \frac{4 V_o I_o}{V_m} \qquad (2.1.11)$$

Using 2.1.11 in 2.1.8, and realizing that $I_o = \frac{V_o}{R_1}$, 2.1.8 can be written as

$$\mathrm{D} = \frac{2V_o}{V_m}\sqrt{\frac{2L_1 f_s}{R_1}} \qquad (2.1.12)$$

where R_1 is the DC load resistor.

2.1.2 Switch RMS current

The switch RMS current can be obtained by first calculating its RMS value over a switching period and then summing all the switching cycles over the rectified line cycle. Suppose i is the total switch current, and i_1, i_2, $\ldots i_n$ are the n currents for every switching cycle over the line period. Then, the total switch current can be expressed as the summation of all the n currents

$$i = \sum_{k=1}^{k=n} i_k \tag{2.1.13}$$

According to its definition, RMS value of the switch current is

$$I_{RMS}^{sw} = \sqrt{\frac{1}{T}\int_0^T i^2(\tau)d\tau}$$

$$= \sqrt{\frac{1}{T}\int_0^T (\sum_{k=1}^{k=n} i_k)^2 d\tau}$$

$$= \sqrt{\sum_{k=1}^{k=n}[\frac{1}{T}\int_{(k-1)T_s}^{kT_s} (i_k{}^2 d\tau)]} \tag{2.1.14}$$

When integrating over an arbitrary switching period, it does not matter how the time axis is chosen. So, the integration can be completed from 0 to the end of a switching period of current waveform as illustrated by Figure 2.6.

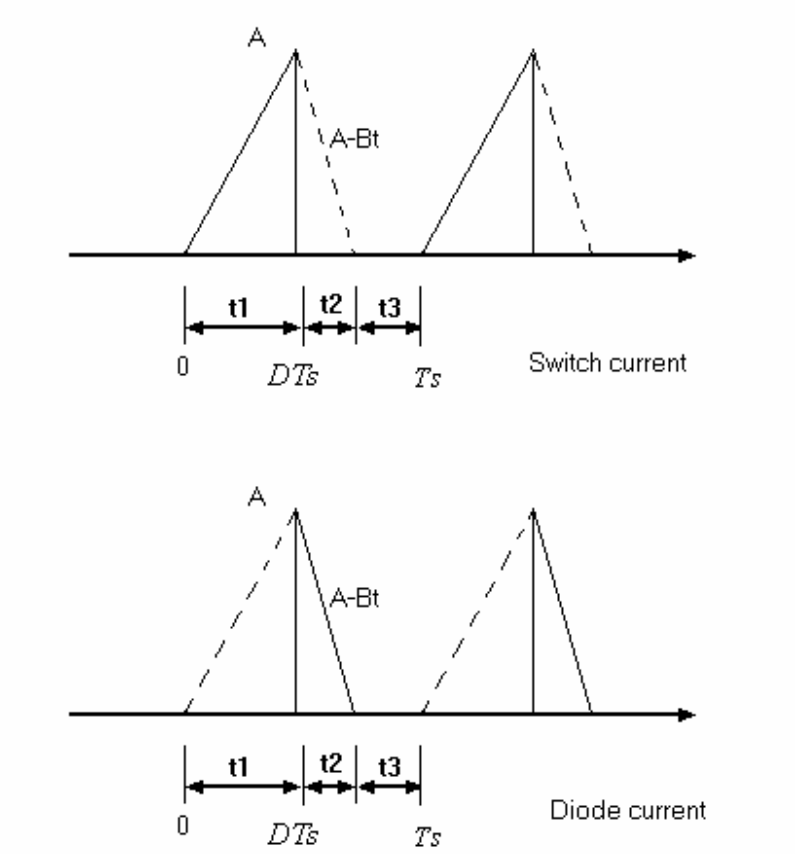

Figure 2.6 Switch and diode current in an arbitrary switching cycle

For the k_{th} switching cycle, the maximum value of inductor current A = $\frac{V_m}{L_1} DT_s \sin(k\omega T_s)$, the decreasing slope is B = $\frac{V_o}{L_1}$, and the time period over which the inductor current decrease to zero is t2 = $\frac{V_m}{V_o} DT_s \sin(k\omega T_s)$ = $\frac{L_1 A}{Vo}$. For this switching cycle, under a straight line assumption for the rise in current

$$\frac{1}{T}\int_0^{T_s} i^2(\tau)d\tau = \frac{1}{T}\int_0^{DT_s} i^2(\tau)d\tau$$

$$= \frac{1}{T}\int_0^{DT_s} (\frac{V_m}{L_1}\sin(k\omega T_s))^2 \tau^2 d\tau$$

$$= \frac{{V_m}^2 D^3 {T_s}^3}{3{TL_1}^2}\sin^2(k\omega T_s) \qquad (2.1.15)$$

Equation 2.1.14 then yields

$$I_{RMS}^{sw\ 2} = \sum_{k=1}^{k=n}[\frac{1}{T}\int_{(k-1)T_s}^{kT_s}(i_k{}^2 d\tau)]$$

$$= \sum_{k=1}^{k=n}[\frac{V_m{}^2 D^3 T_s{}^3}{3TL_1{}^2}\sin^2(k\omega T_s)]$$

$$= \frac{V_m{}^2 D^3 T_s{}^3}{3TL_1{}^2}\sum_{k=1}^{k=n}[\sin^2(k\omega T_s)] \qquad (2.1.16)$$

Because switching frequency is much higher than the line frequency, the summation in equation 2.1.16 can be approximated as an integration over line period.

$$I_{RMS}^{sw\ 2} = \frac{V_m{}^2 D^3 T_s{}^3}{3TL_1{}^2}\sum_{k=1}^{k=n}[\sin^2(k\omega T_s)]$$

$$= \frac{V_m{}^2 D^3 T_s{}^2}{3TL_1{}^2}\sum_{k=1}^{k=n}[T_s\sin^2(k\omega T_s)]$$

$$\approx \frac{V_m{}^2 D^3 T_s{}^2}{3TL_1{}^2}\int_0^{\frac{\pi}{\omega}}\sin^2(\omega t)dt$$

$$= \frac{V_m{}^2 D^3 T_s{}^2}{3TL_1{}^2}\frac{\pi}{2\omega}$$

$$= \frac{V_m{}^2 D^3 T_s{}^2}{12L_1{}^2}$$

By use of 2.1.12, the RMS value of the current through the power switch can be expressed as

$$I_{RMS}^{sw} = 2V_o\sqrt{\frac{V_o}{3V_m R_1}\sqrt{\frac{2}{R_1 L_1 f_s}}} \qquad (2.1.17)$$

2.1.3 Diode RMS current

The diode RMS current can be evaluated by using the same approach as the one we used to calculate the switch RMS current of 2.1.17. For one switching cycle,

$$\frac{1}{T}\int_0^{T_s} i^2(\tau)d\tau = \frac{1}{T}\int_0^{t_2} i^2(\tau)d\tau$$

$$= \frac{1}{T}\int_0^{t_2} (A - B\tau)^2 d\tau$$

$$= \frac{(3V_o{}^2L_1 - 3V_oBL_1{}^2 + B^2L_1{}^3)}{3TV_o{}^3} A^3 \qquad (2.1.18)$$

Integrating the value over a source cycle and applying the expressions for A and B leads to

$$I_{RMS}^{d}{}^2 = \frac{(3V_o{}^2L_1 - 3V_oBL_1{}^2 + B^2L_1{}^3)}{3TT_sV_o{}^3} \int_0^{\frac{\pi}{\omega}} \frac{V_m{}^3D^3T_s{}^3}{L_1{}^3} \sin^3(\omega t)dt$$

$$= \frac{4(3V_o{}^2 - 3V_oBL_1 + B^2L_1{}^2)V_m{}^3D^3T_s{}^2}{18\pi L_1{}^2Vo^3}$$

$$= \frac{2V_m{}^3D^3T_s{}^2}{9\pi L_1{}^2Vo}$$

By use of 2.1.2, the RMS value of the current through the diode can be obtained as

$$I_{RMS}^{d} = \frac{2V_mDT_s}{3L_1}\sqrt{\frac{V_mD}{2\pi V_o}}$$

$$= \frac{4V_o}{3}\sqrt{\frac{2}{\pi R_1}\sqrt{\frac{2}{RL_1f_s}}} \qquad (2.1.19)$$

2.1.4 Inductor RMS current

Inductor current RMS value can be obtained from the switch RMS current and diode RMS current as

$$I_{RMS}^{ind} = \sqrt{{i_{RMS}^{d}}^2 + {i_{RMS}^{sw}}^2}$$

$$= 4V_o\sqrt{\frac{V_o}{V_m R_1}\left(\frac{V_m}{9\pi V_o}+\frac{1}{12}\right)\sqrt{\frac{2}{RL_1 f_s}}} \qquad (2.1.20)$$

2.1.5 Output filter capacitor

The output filter capacitor can be sized based on the output voltage ripple specification. During a line period, the output filter capacitor is charged when the switch is on. When the switch is off, the output capacitor is discharged. The discharge current is the output current. The output voltage ripple can be evaluated as

$$\Delta V_o = \frac{1}{C_{fout}}(I_o T_{off})$$

where, I_o is the average value of output current, T_{off} is the total discharge time for the output filter capacitor in one line period given by,

$$T_{off} = \frac{T}{2} + \sum_{k=1}^{k=\frac{T}{2T_s}}[(1-D)T_s]$$

$$= \frac{T}{2} + \sum_{k=1}^{k=\frac{T}{2T_s}}\left[\left(1-\frac{2V_o}{V_m}\sqrt{\frac{2L_1 f_s}{R_1}}\right)T_s\right]$$

$$\approx \frac{T}{2} + \int_0^{\frac{T}{2}}\left(1-\frac{2V_o}{V_m}\sqrt{\frac{2L_1 f_s}{R_1}}\right)dt$$

$$= T - \frac{V_o T}{V_m}\sqrt{\frac{2L_1 f_s}{R_1}}$$

$$= \left(1-\frac{D}{2}\right)T \qquad (2.1.21)$$

where T is the source period.

Consequently, the output filter capacitor can be sized as

$$C_{fout} = \frac{1}{\Delta V_o}(I_o T_{off})$$

$$= (1-\frac{D}{2})T\ \frac{V_o}{R\Delta V_o} \qquad (2.1.22)$$

2.2 Continuous current mode analysis

As shown in Figure 2.7, in continuous conduction mode (CCM), the inductor current never goes to zero in a switching period.

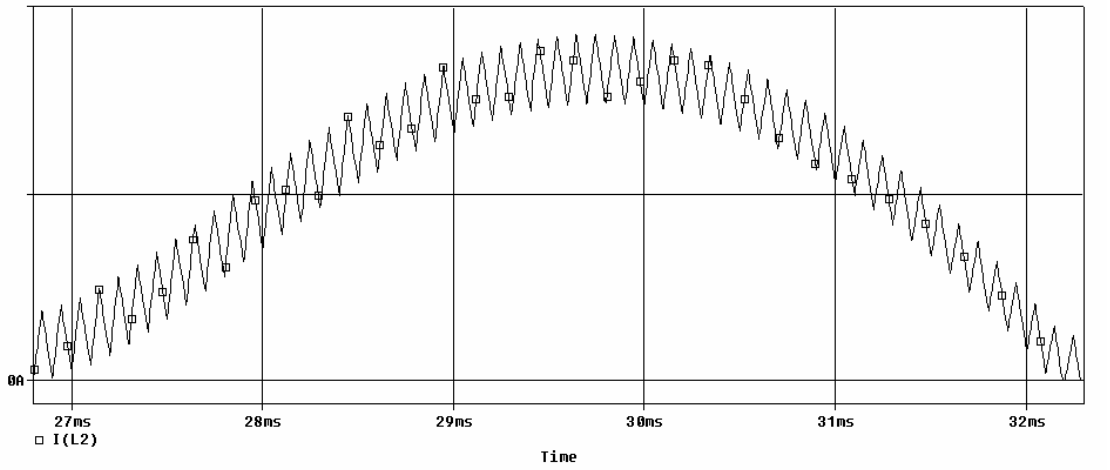

Figure 2.7 Converter inductor current in CCM

2.2.1 Duty cycle

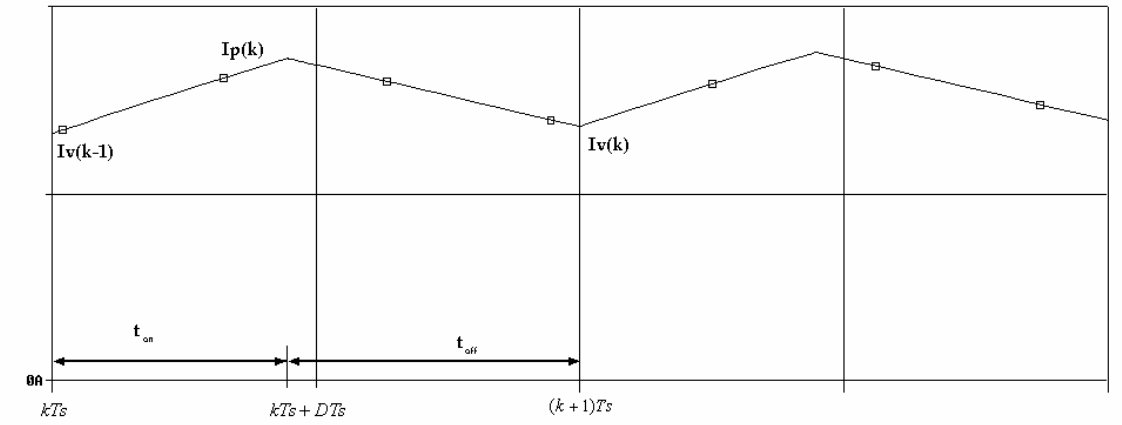

Figure 2.8 Inductor current waveform in CCM

As shown in Figure 2.8, the inductor current in an arbitrary switching period rises over the transistor on time, t_{on}, and decreases when the switch is off. During the transistor on time, the inductor current can be expressed as

$$i_L(t) = I_V(k-1) + \frac{1}{L_1}\int_{kT_s}^{t} V_m \sin(\omega\tau)d\tau$$

$$= I_V(k-1) + \frac{V_m}{\omega L_1}(\cos k\omega T_s - \cos \omega t) \qquad (2.2.1)$$

where, $I_V(k-1)$ is the value at the end of the previous switching period. The maximum value of $i_L(t)$ during the k_{th} switching cycle occurs at time $(k+d)T_s$. We denote it as $I_p(k)$. It is expressed as

$$I_p(k) = I_V(k-1) + \frac{V_m}{\omega L_1}[\cos k\omega T_s - \cos \omega(k+d)T_s]$$

$$= I_V(k-1) + \frac{V_m}{\omega L_1}[\cos(k\omega T_s) - \cos(k\omega T_s)\cos(\omega d T_s) + \sin(k\omega T_s)\sin(\omega d T_s)] \qquad (2.2.2)$$

Using the same approximation as in Equation 2.1.2, the Equation 2.2.2 can be simplified to

$$I_p(k) = I_V(k-1) + \frac{V_m}{L_1} d T_s \sin(k\omega T_s) \qquad (2.2.3)$$

where, $1 \le k \le \frac{f_s}{2f} = \frac{T}{2T_s}$

When the switch is off, inductor current begins to decrease, and it is expressed as Equation 2.2.4.

$$i_L(t) = I_p(k) - \frac{V_o}{L_1}(t - kT_s - DT_s) \qquad (2.2.4)$$

At time $(k+1)T_s$, the inductor current decreases to its minimum value in the k_{th} switching period.

$$I_v(k) = I_p(k) - \frac{V_o}{Lv}(1-d)T_s \qquad (2.2.5)$$

Substitute 2.2.3 into 2.2.5, to give

$$I_v(k) = I_{v(}k-1) + \frac{V_m}{L_1} dT_s \sin(k\omega T_s) - \frac{V_o}{L_1}(1-d)T_s \qquad (2.2.6)$$

Since T_s is much smaller than half of the half period T, letting $I_v(k) = I_V(k-1)$ introduces negligible error into our calculation. Using this approximation, we find the duty cycle for CCM as

$$d = \frac{V_o}{V_o + V_m \sin(k\omega T_s)}$$

$$= \frac{1}{1 + \frac{V_m \sin(k\omega T_s)}{V_o}} \qquad (2.2.7)$$

2.2.2 Switch RMS current

Figure 2.9 shows the instantaneous inductor current for several switching cycles. From kT_s to $kT_s + dT_s$, inductor current increases, and from $kT_s + dT_s$ to $(k+1)T_s$, it decreases. In fact, from kT_s to $kT_s + dT_s$, inductor current is the same as the current through the switch, and from $kT_s + dT_s$ to $(k+1)T_s$, it is the same as the current through the diode. Average of the current through the

switch over the switching period should be the average of the source current over the same switching period. That is

$$< i_{in} >|_{T_s} = < i_{switch} >|_{T_s} \quad \frac{\frac{I_v(k-1)+I_p(k)}{2} dT_s}{T_s} = \frac{I_v(k-1)+I_p(k)}{2} d \qquad (2.2.8)$$

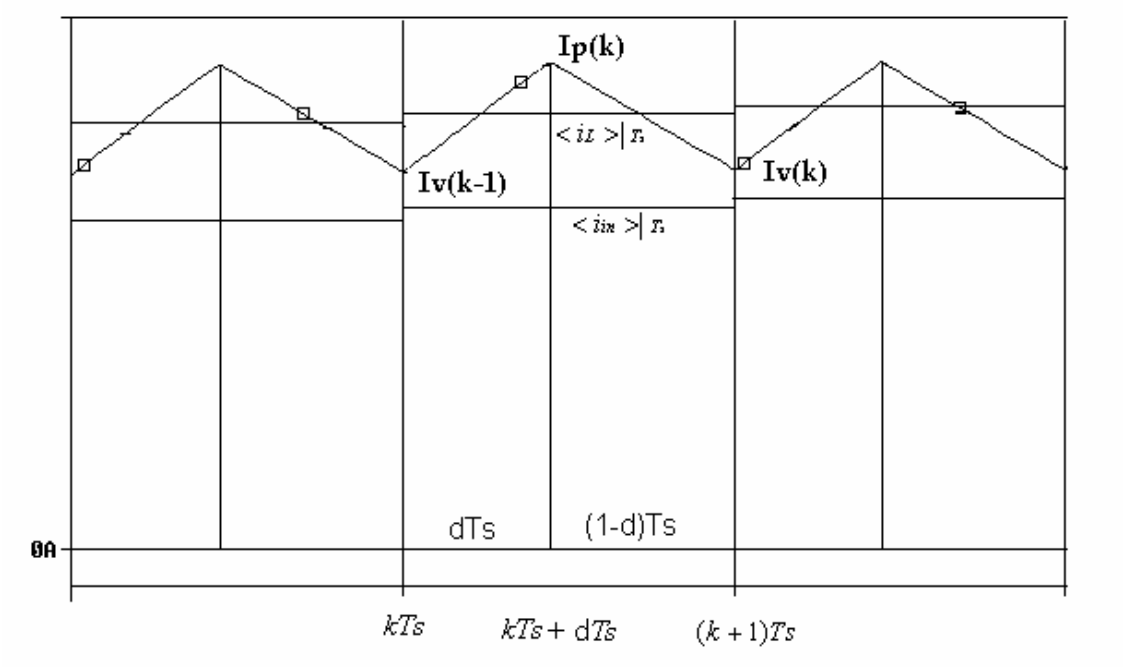

Figure 2.9 Inductor current in CCM

In the same switching period, the average of the inductor current is

$$< i_L >|_{T_s} = \frac{I_v(k-1)+I_p(k)}{2} \qquad (2.2.9)$$

From 2.2.8 and 2.2.9, the following equation can be obtained

$$< i_L >|_{T_s} = \frac{< I_{in} >|_{T_s}}{d} \qquad (2.2.10)$$

Assuming that the source current is perfectly in phase with the line voltage and can be assumed constant over a switching period without significant analytical error, in k_{th} switching period, the source current is

$$i_{in}(kT_s) = \mathrm{I_m}\sin(k\omega T_s) \tag{2.2.11}$$

where $\mathrm{I_m}$ is the maximum value of the source current.

From 2.2.10 and 2.2.11, we can get the average inductor current during the same switching period.

$$< i_L >|_{T_s} = \frac{\mathrm{I_m}}{d}\sin(k\omega T_s) \tag{2.2.12}$$

Thus, using the same method in 2.1.2, the switch RMS current can be evaluated as

$$\frac{1}{T}\int_0^{T_s} i^2(\tau)d\tau = \frac{1}{T}\int_0^{dT_s} i^2(\tau)d\tau$$

$$= \frac{1}{T}\int_0^{dT_s}[\frac{\mathrm{I_m}}{d}\sin(k\omega T_s)]^2 d\tau$$

$$= \frac{\mathrm{I_m}^2}{T}[1+\frac{V_m}{V_o}\sin(k\omega T_s)]\sin^2(k\omega T_s)\ T_s$$

$$= \frac{\mathrm{I_m}^2}{T}[\sin^2(k\omega T_s)+\frac{V_m}{V_o}\sin^3(k\omega T_s)]T_s$$

$$I_{RMS}^{sw\ 2} = \sum_{k=1}^{k=n}[\frac{1}{T}\int_{(k-1)T_s}^{kT_s}(i_k{}^2 d\tau)$$

$$= \sum_{k=1}^{k=n}\frac{\mathrm{I_m}^2 T_s}{T}[\sin^2(k\omega T_s)+\frac{V_m}{V_o}\sin^3(k\omega T_s)]$$

$$\approx \frac{\mathrm{I_m}^2}{T}\int_0^{\frac{\pi}{\omega}}[\sin^2(\omega t)+\frac{V_m}{V_o}\sin^3(\omega t)]dt$$

$$= \frac{\mathrm{I_m}^2}{T}(\frac{\pi}{2\omega}+\frac{V_m}{V_o}\frac{4}{3\omega})$$

$$= \mathrm{I_m}^2(\frac{1}{4}+\frac{V_m}{V_o}\frac{2}{3\pi})$$

So, the switching RMS current can be obtained as

$$I_{RMS}^{sw} = \mathrm{Im}\sqrt{\frac{1}{4}+\frac{V_m}{V_o}\frac{2}{3\pi}}$$

$$= I_{RMS}^{src}\sqrt{\frac{1}{2}+\frac{V_m}{V_o}\frac{4}{3\pi}} \qquad (2.2.13)$$

where, I_{RMS}^{src} is the source current RMS value.

2.2.3 Diode RMS current

When the power switch is off, current flows through the diode and the inductor. When the power switch is on, current through the diode is zero.

$$\frac{1}{T}\int_0^{T_s} i^2(\tau)d\tau = \frac{1}{T}\int_0^{(1-d)T_s} i^2(\tau)d\tau$$

$$= \frac{1}{T}\int_0^{(1-d)T_s}[\frac{\mathrm{Im}^2}{d^2}\sin(k\omega T_s)]^2 d\tau$$

$$= \frac{V_m \mathrm{Im}^2}{V_o T}[1+\frac{V_m}{V_o}\sin(k\omega T_s)]\sin^3(k\omega T_s)\ T_s$$

$$= \frac{V_m \mathrm{Im}^2}{V_o T}[\sin^3(k\omega T_s)+\frac{V_m}{V_o}\sin^4(k\omega T_s)]\ T_s$$

$$I_{RMS}^{d\ 2} = \sum_{k=1}^{k=n}[\frac{1}{T}\int_{(k-1)T_s}^{kT_s}(i_k{}^2 d\tau)$$

$$= \sum_{k=1}^{k=n}\frac{V_m \mathrm{Im}^2\ T_s}{V_o T}[\sin^3(k\omega T_s)+\frac{V_m}{V_o}\sin^4(k\omega T_s)]$$

$$\approx \frac{V_m \mathrm{Im}^2}{V_o T}\int_0^{\frac{\pi}{\omega}}[\sin^3(\omega t)+\frac{V_m}{V_o}\sin^4(\omega t)]dt$$

$$= \frac{V_m \mathrm{Im}^2}{V_o}(\frac{2}{3\pi}+\frac{V_m}{V_o}\frac{3}{16})$$

So, $I_{RMS}^{d} = \mathrm{Im}\sqrt{\frac{V_m}{V_o}(\frac{2}{3\pi}+\frac{V_m}{V_o}\frac{3}{16})}$

$$= I_{RMS}^{src}\sqrt{\frac{V_m}{V_o}(\frac{4}{3\pi}+\frac{V_m}{V_o}\frac{3}{8})} \qquad (2.2.14)$$

where, I_{RMS}^{src} is the source current RMS value.

2.2.4 Inductor RMS current

We assume that the inductor current is constant during a switching period, so

$$\frac{1}{T}\int_0^{Ts} i^2(\tau)d\tau = \frac{1}{T}\int_0^{Ts} i^2(\tau)d\tau$$

$$= \frac{1}{T}\int_0^{Ts}[\frac{\mathrm{Im}}{d}\sin(k\omega Ts)]^2 d\tau$$

$$= \frac{1}{T}(\frac{\mathrm{Im}}{d})^2\sin^2(k\omega Ts)Ts$$

$$I_{RMS}^{ind\ 2} = \sum_{k=1}^{k=n}[\frac{1}{T}\int_{(k-1)Ts}^{kTs}(i_k{}^2 d\tau)$$

$$= \frac{1}{T}\sum_{k=1}^{k=n}[\frac{\mathrm{Im}^2}{d^2}\sin^2(k\omega Ts)Ts]$$

$$= \frac{1}{T}\sum_{k=1}^{k=n}[\mathrm{Im}^2\sin^2(k\omega Ts)[1+\frac{V_m}{V_o}\sin(k\omega Ts)]^2 Ts]$$

$$\approx \frac{\mathrm{Im}^2}{T}\int_0^{\frac{\pi}{\omega}}[\sin^2(\omega t)+\frac{2V_m}{V_o}\sin^3(\omega t)+\frac{V_m{}^2}{V_o{}^2}\sin^4(\omega t)]dt$$

$$= \frac{\mathrm{Im}^2}{T}\int_0^{\frac{\pi}{\omega}}[\sin^2(\omega t)+\frac{2V_m}{V_o}\sin^3(\omega t)+\frac{V_m{}^2}{V_o{}^2}\sin^4(\omega t)]dt$$

So, $I_{RMS}^{ind} = \mathrm{Im}\sqrt{\frac{1}{4}+\frac{4V_m}{3V_o\pi}+\frac{3V_m{}^2}{16V_o{}^2}}$

$$= I_{RMS}^{src}\sqrt{\frac{1}{2}+\frac{8V_m}{3V_o\pi}+\frac{3V_m{}^2}{8V_o{}^2}} \qquad (2.2.15)$$

where, I_{RMS}^{src} is the source current RMS value.

2.2.5 Output filter capacitor

Output filter capacitor can be sized based on the output voltage ripple specification. In a line period, the output filter capacitor is charged when the switch is on. When the switch is off, the output is discharged. The discharge current is the output current. So, the output voltage ripple can be evaluated as

$$\Delta V_o = \frac{1}{C_{fout}}(I_o T_{off}) \tag{2.2.16}$$

where, T_{off} is the total discharge time for the output filter capacitor in one line period.

$$\begin{aligned}
T_{off} &= \frac{T}{2} + \sum_{k=1}^{k=\frac{T}{2T_s}}[(1-d)T_s] \\
&= \frac{T}{2} + \sum_{k=1}^{k=\frac{T}{2T_s}}\{[1-\frac{1}{1+\frac{V_m \sin(k\omega T_s)}{V_o}}]T_s\} \\
&\approx \frac{T}{2} + \int_0^{\frac{\pi}{\omega}}(1-\frac{1}{1+\frac{V_m}{V_o}\sin\omega t})dt \\
&= T - \frac{2\tan^{-1}\{\frac{[\frac{V_m}{V_o}+tg(\frac{\omega t}{2})]}{\sqrt{1-(\frac{V_m}{V_o})^2}}\}}{\omega\sqrt{1-(\frac{V_m}{V_o})^2}}\Bigg|_0^{\frac{\pi}{\omega}} \\
&= \mathrm{Re}\{1-\frac{1}{2\sqrt{1-(\frac{V_m}{V_o})^2}}+\frac{\tan^{-1}[\frac{V_m}{V_o\sqrt{1-(\frac{V_m}{V_o})^2}}]}{\pi\sqrt{1-(\frac{V_m}{V_o})^2}}\}T
\end{aligned} \tag{2.2.17}$$

From 2.2.16, the output filter capacitor can be decided as

$$C_{fout} = \frac{I_o T_{off}}{\Delta V_o} \qquad (2.2.18)$$

2.3 Input filter design

To limit conducted electromagnetic interference, it is necessary to place a filter network between the power source and converter, as shown in Figure 2.10, to attenuate the switching harmonics that are present in the converter input current waveform. The input filter should provide sufficient attenuation for the current component of switching frequency and avoid any possible oscillation.

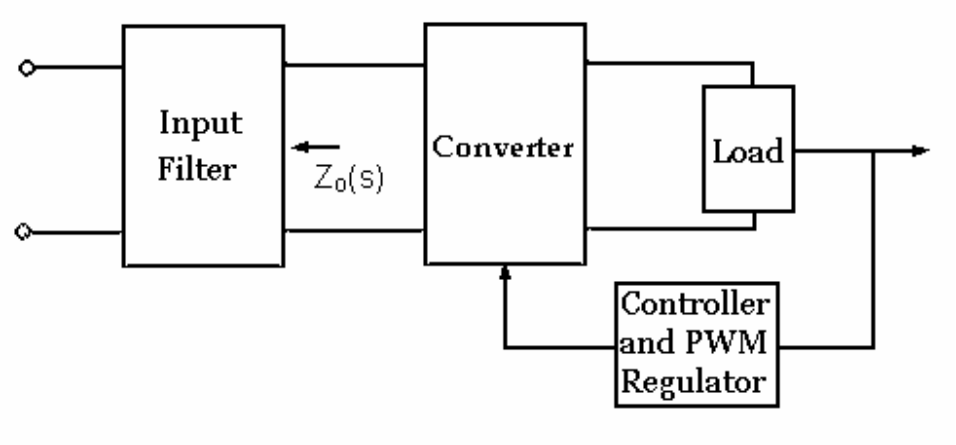

Figure 2.10 Addition of input filter to switching power regulator

Figure 2.11 shows the chosen LC filter with damping resistor R_f for the converter circuit. The converter is modeled by a current source having currents of fundamental frequency and harmonic frequencies, including switching frequency.

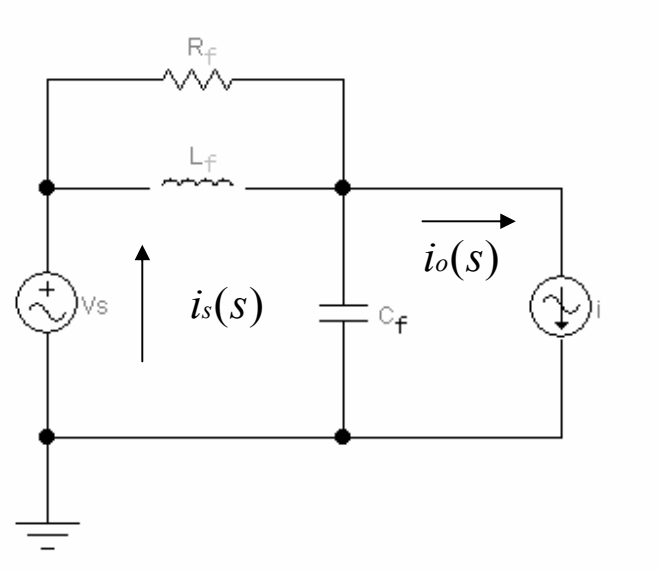

Figure 2.11 LC filter with damping resistor

In order to study the current (i_s) through the source, we need to know the transfer function $H(s) = \frac{i_s(s)}{i_o(s)}$. Deactivate the independent voltage source v_s as shown in Figure 2.12. Then, by KCL and KVL,

$$i_o(s) = i_c(s) + i_s(s) \tag{2.3.1}$$

$$i_c(s)\frac{1}{sC_f} = i_s(s)\frac{sR_fL_f}{R_f + sL_f} \tag{2.3.2}$$

Solving 2.3.1 for $i_c(s)$ and substituting the result into 2.3.2, the transfer function can be obtained as

$$H(s) = \frac{sL_f + R_f}{s^2L_fC_fR_f + sL_f + R_f} \tag{2.3.3}$$

A characteristic bode plot of this transfer function is displayed by Figure 2.13. It shows that for high frequencies, current through the source is significantly suppressed. However, the filter inductor and capacitor should be chosen carefully to avoid oscillation at the resonant frequency $f_f = \frac{1}{2\pi\sqrt{L_fC_f}}$.

Specifically, the converter switching frequency must be greater than the filter corner frequency and the source frequency must be less than the corner frequency.

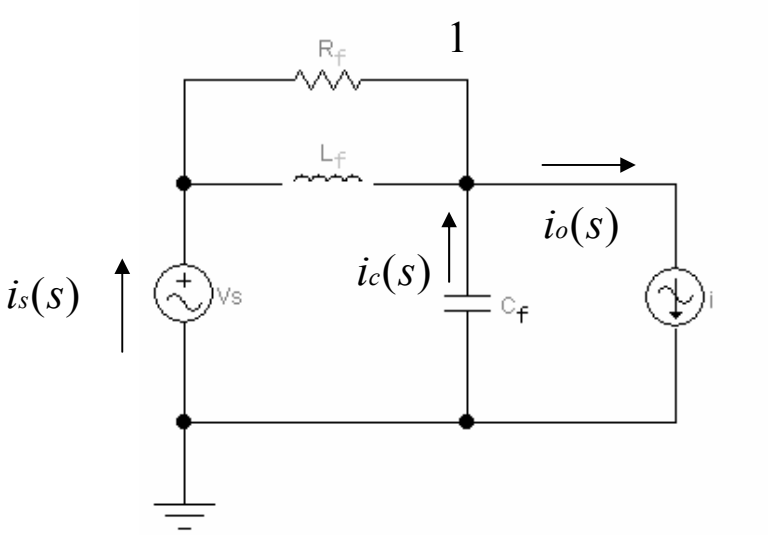

Figure 2.12 Decide the current transfer function

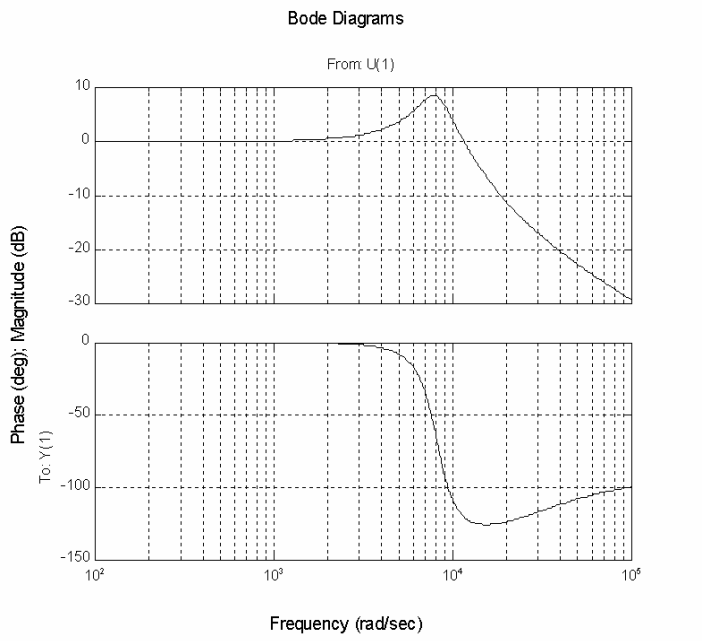

Figure 2.13 Characteristic bode plot for the current transfer function of the input filter

After the input filter is added into the switching power supply, it may affect the dynamics of the converter. If an inappropriate input filter is added into the switching power regulator, it can adversely affect the regulator's performance, or even cause instability in the power system. However, if the output impedance of the input filter $|Z_0(s)|$ is small enough, its impact on converter's control-to-output transfer function can become negligible[3]. Thus, the input filter should be designed to have very low output impedance.

Output impedance of the filter can be determined by setting the independent voltage source to zero, as is shown in Figure 2.14. The output impedance is the parallel impedances of the inductor, resistor, and capacitor:

$$Z_o(s) = Z_L \,||\, R_f \,||\, Z_C = \frac{1}{\frac{1}{sL_f} + \frac{1}{1/sC_f} + \frac{1}{R_f}}$$

$$= \frac{sR_fL_f}{s^2L_fC_fR_f + SL_f + R_f} \qquad (2.3.4)$$

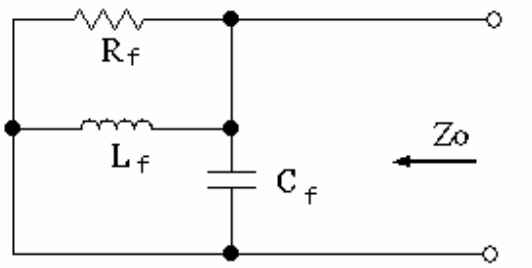

Figure 2.14 Determine the output impedance of the simple LC input filter

The characteristic bode plot of the impedance is plotted as Figure 2.15. It is seen that for the resonant frequency $f_f = \frac{1}{2\pi\sqrt{L_fC_f}}$, the output impedance of the filter has a maximum value that is equal to the value of the resistor. In fact, at resonant frequency ω_f, magnitudes of the inductor and capacitor impedances are identical so that their parallel combination forms an infinite impedance that shunts the resistor R_f. Equation (2.3.4) yields

$$\omega_f L_f = \frac{1}{\omega_f C_f}$$

$$Z(j\omega_f) = \frac{1}{\frac{1}{j\omega_f L_f} + \frac{1}{1/(j\omega_f C_f)} + \frac{1}{R_f}} = R_f \qquad (2.3.5)$$

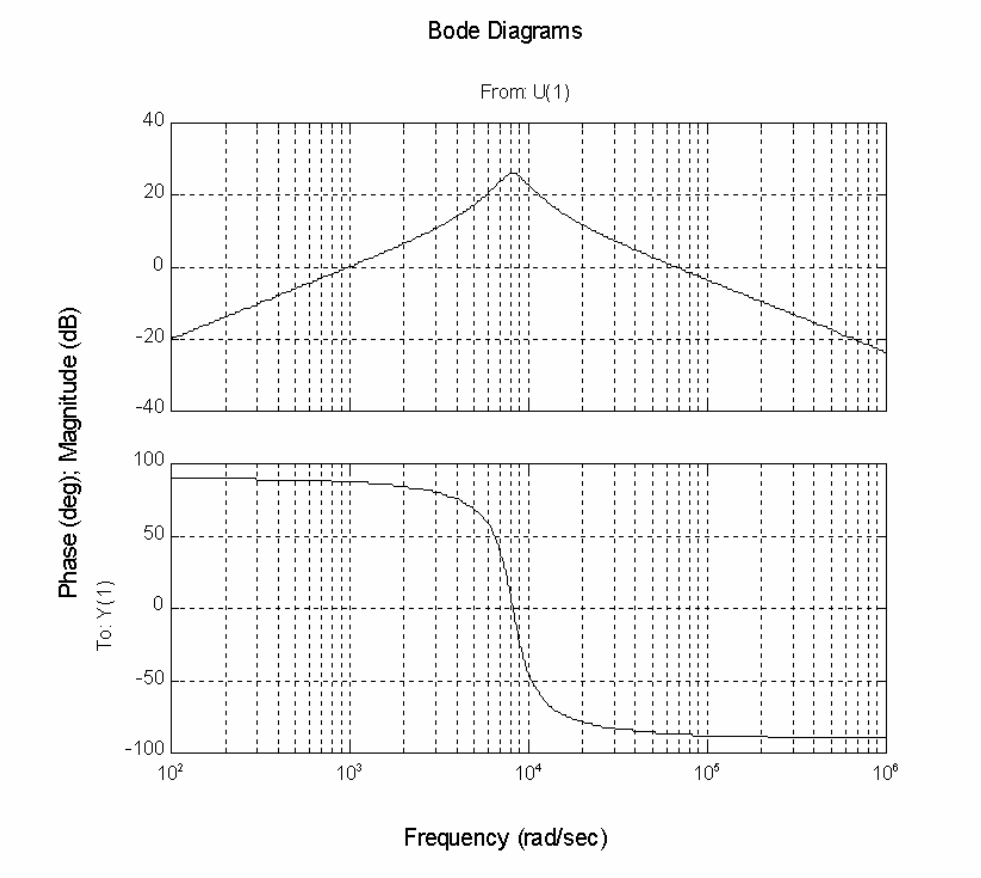

Figure 2.15 Characteristic bode plot for the output impedance of the input filter

To reduce the output impedance, it is necessary to decrease the inductance and resistance, and increase the capacitance. However, according to Equation 2.3.3, large values of R_f and L_f are needed to diminish the high frequency current flowing through the source. But, large values of R_f and L_f also reduce the voltage available at the converter input, thereby diminishing performance. Further, decrease of L_f and R_f will result in the filter input impedance appearing more capacitive so that it draws more leading

current from the source, degrading the power factor. So, proper compromise is required in determination of the value for R_f and L_f.

Reference

1. Chen Zhou, “Design and analysis of an active power factor correction circuit”, Master’s thesis, Virginia Polytechnic Institute and State University, Sep. 1989.
2. Ramesh K. Tripathi, Shyama P. Das, and Gopal K. Dubey, “Mixed-Mode Operation of Boost Switch-Mode Rectifier for Wide Range of Load Variations”, IEEE Transactions On Power Electronics, Nov. 2002, Vol.17, No. 6, pp999-1009.
3. M.S. Dawande and G.K. Dubey, “Programmable input power factor correction method for switch mode rectifiers”, IEEE Transactions On Power Electronics, Vol. 11, July 1996, pp585-591.
4. Sandra Y. Erich and William M. Polivka, “Input filter design for current-programmed regulators”, IEEE APEC’90, pp781-791.

3. Control design

In chapter 2, the justification for selecting the dual half-wave buck-boost converter power circuit arrangement is made. The objectives of this chapter are to present and develop the control method and its physical implementation.

3.1 Control method review in switching power electronics

Generally, control methods for switching power supplies are classified into voltage mode control and current mode control. Voltage mode control uses a reference and the actual output voltage to produce the error between them. The error voltage is compensated and compared with ramp voltage to produce desired PWM gating signals for the power switches. In current mode control, a target current in the power stage is sensed and compared with a reference current signal to produce PWM gating signals for the power switches. A short review of the operation and features of available control methods is necessary to understand the underlying reasons for choice of control for the converter of this thesis.

3.1.1 Voltage mode control

Direct duty cycle control

As shown in Figure 3.1, in a direct duty cycle control scheme, the output voltage is sensed and compared with its reference. A compensation network is added to stabilize the closed-loop system. The error voltage V_{error} is

compensated and compared with a ramp-voltage carrier-signal to produce a desired gating signal for the power switch. Actual circuit implementation of a voltage-mode control pulse-width-modulator is simply a ramp generator and a comparator. The ramp waveform can be either a sawtooth waveform or a triangle waveform. As the ramp waveform varies from its minimum level to its maximum, the output of the PWM comparator switches from a high level to a low level, with the transition occurring when the two comparator inputs are equal. This control scheme is easy to implement. And, because frequency of the PWM signal is fixed, it simplifies the power filter design to remove harmonics of switching frequency.

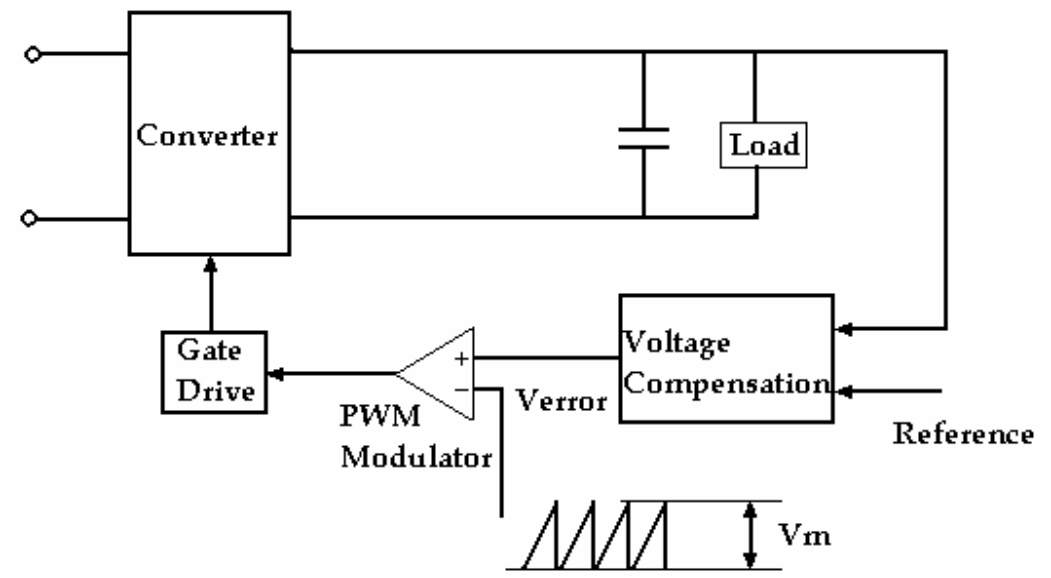

Figure 3.1 Basic voltage mode control block diagram

However, this method has the following disadvantages:

(1) No voltage feed-forward signal is provided to anticipate the effects of input voltage changes. Its open-loop line regulation is poor, and requires higher loop gain to achieve specifications. [4]

(2) The output filter capacitor is part of the closed-loop system and introduces a phase lag that delays correction for V_{in} changes. [4]

Voltage feedforward control

An improved voltage mode control is voltage feedforward control. In voltage feedforward control, amplitude of the sawtooth ramp (V_m) varies in proportion to the input voltage. Because ramp voltage varies directly with input voltage, if carrier signal is constant, the duty cycle varies inversely with the input voltage. Thus, the volt-second product of the output voltage remains constant without any control action. Open-loop line regulation is very good, and the problem of direct duty cycle control in is corrected. Closed-loop gain is reduced and dictated by mostly the level necessary to achieve good dynamic response.

3.1.2 Current mode control

Another type control method is current mode control. This is a two-loop control system. An inner control loop compares a target current with its reference to produce desired gating signal. All of the problems of the direct duty cycle control method are corrected by using this control method. In current mode control, the switching power supply inductor is in the inner current control loop. As a consequent, the transfer function from control voltage to output voltage has a single-pole roll-off. In voltage mode control, the control to output transfer function has a two-pole roll-off. So, the current mode control system can be stabilized with a simpler compensation network.

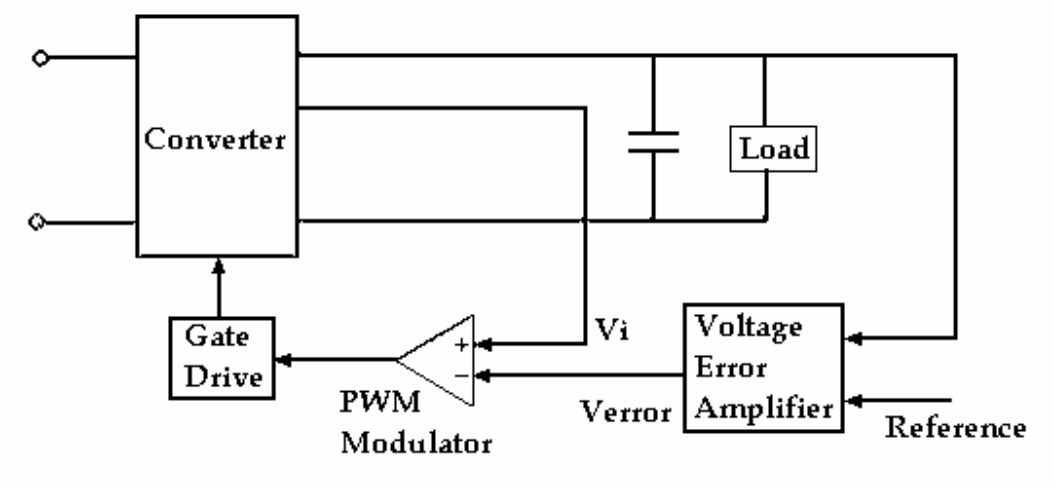

Figure 3.2 Peak current mode control block diagram

Peak current mode control

As shown in Figure 3.2, in peak current mode control, upslope of inductor current (V_i) (or power switch current) is compared with a current command signal (V_{error}) set by an outer voltage control loop. Output of the PWM circuit goes to low level when the instantaneous current increases to the desired level.

The peak current mode control has the disadvantages:

(1) It is susceptible to noise. Noise spikes coupled from power circuit to control circuit can cause the switch turn off immediately[4].

(2) When duty cycle is higher than 0.5, the peak current control is inherently unstable. A compensation ramp is needed to stabilize the control circuit. When this control is applied in power factor correction circuit, a fixed ramp with adequate compensation can work with for varying input voltage. However, it results in performance degradation and increased distortion[4].

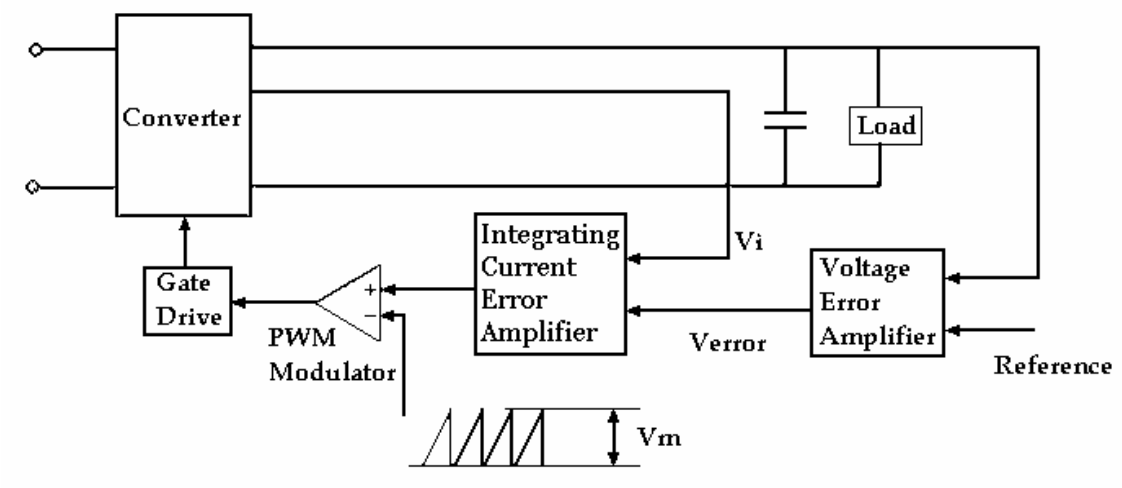

Figure 3.3 Average current mode control block diagram

Average current mode control

Figure 3.3 shows the block diagram for the average current mode control. In average current mode control, an integrating current error amplifier is introduced into the current loop. Output of the current amplifier is the amplified difference between the averaged inductor current (V_i) (or power switch current) and the current command (V_{error}) decided by the outer loop.

In average current mode control, the inner loop gain-bandwidth characteristic can be tailored for optimum performance by the compensation network around the current amplifier. And, its lower frequencies gain can be made much greater than that of peak current mode control[4].

Average current mode control is good for power factor correction due to the following advantages over peak current mode control:

1) In average current mode control, the average current tracks the current command with a high degree of accuracy. It is a particular advantage for power factor correction circuit.
2) Average current mode control can be used to control the current in any circuit branch in all the three basic switch mode converter topologies. It

can control the input current accurately with both buck and buck-boost topologies, and it can control output current with boost and buck-boost topologies.

3) Slope compensation, which is a must for peak current mode control when the duty ratio is above 0.5, is not necessary in average current mode control.
4) It has excellent noise immunity.

Huai Wei and Issa Batarseh compared the basic topologies for power factor correction in[1][2]. If basic DC-DC converters are used in power factor correction, there is no need for a control loop from the input side point of view, due to their inherent power factor correction property. According to their study, buck-boost and flyback converter have excellent self power factor correction ability when they work in discontinuous current mode (DCM). Average input current in the buck-boost converter linearly follows the input line voltage. Erikson, Madigan, and Singer have also analyzed and substantiated these findings for the buck-boost PFC converter in discontinuous current mode [3].

If power stage components are chosen properly to make the buck-boost converter in DCM, only a voltage negative feedback is necessary to produce a sinusoidal input current waveform. However, DCM poses high peak current stress on the inductor, switches, and output capacitor. The peak currents through the power switch and rectifier are nearly twice as high as with continuous mode operation. A bulky capacitor is needed to balance the instantaneous power between the input and output. Practical application is limited to low to medium power levels.

In our application, the power stage components are chosen to make the PFC circuit function in Continuous Current Mode(CCM). When the circuit works in CCM, it may suffer from the problem that the boundary is crossed into discontinuous mode at light loads and high input voltage. And, at the beginning

and end of every line half cycle, the inductor current may be discontinuous due to low input voltage. Fortunately, this problem can be solved inherently in average current mode control [4]. It works well with both the continuous and discontinuous current mode, and it allow implementation with minimum inductance value.

In Figure 3.3, generally the inductor current or switch current is sensed and controlled to follow its reference. Particularly, in the buck-boost converter based power factor correction circuit, the switch current is sensed and controlled. Figure 3.4 shows the commonly used control scheme.

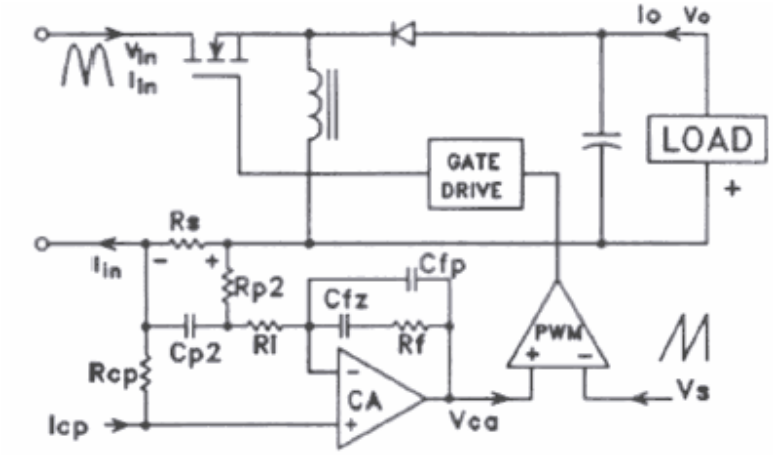

Figure 3.4 Buck-boost based PFC using average current mode control

In designing the current error amplifier in Figure 3.4, the chopped current sensed by R_s is averaged by the high-pass filter consisting of R_{p2} and C_{p2}. The filter should be designed with high DC gain, but with significant attenuation of high frequencies. When the switching frequency is quite high, it is easy to design a filter with a corner frequency above the line frequency. In high power applications, lower switching frequency is often used to reduce the switching loss. As a consequent, high pass filter design in Figure 3.4 may be somewhat more difficult when trying to avoid significant phase shift in the source current at line frequency.

In buck and buck-boost converters, the converter input current wave is chopped at switching frequency. So, it is necessary to place a filter between the converter and line input to remove high frequency harmonics. Since it is the goal for PFC circuit to yield good quality input sinusoidal current waveform viewed from the power source, it should be a better approach to make the input current the direct control target. As shown in Figure 3.5, the line input current is sensed and sent into the current error amplifier to be compared with its reference from the outer loop. In this chapter, the direct input current control method and its physical implementation are presented and developed.

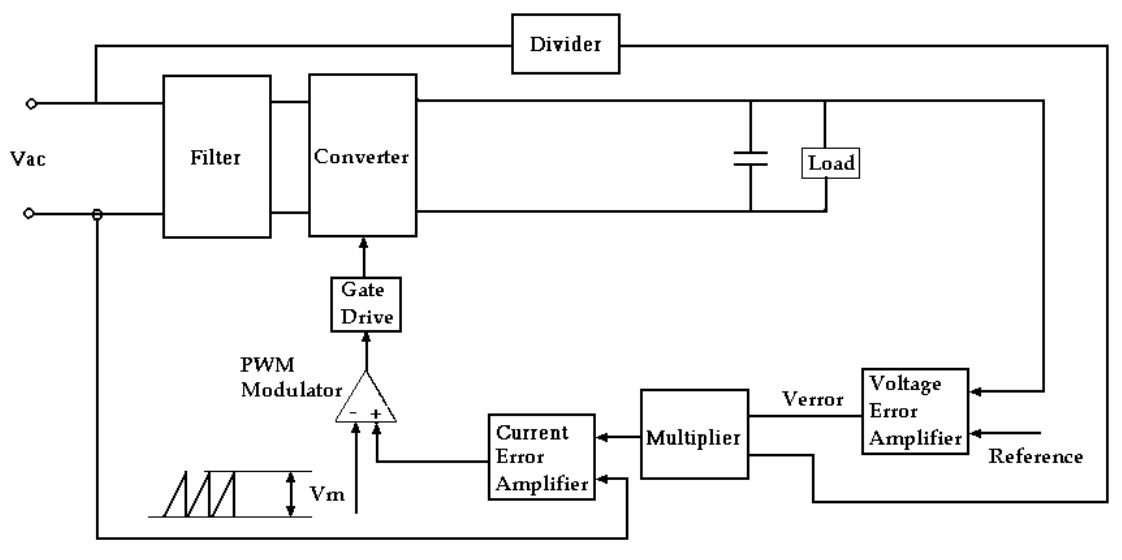

Figure 3.5 Direct input current control

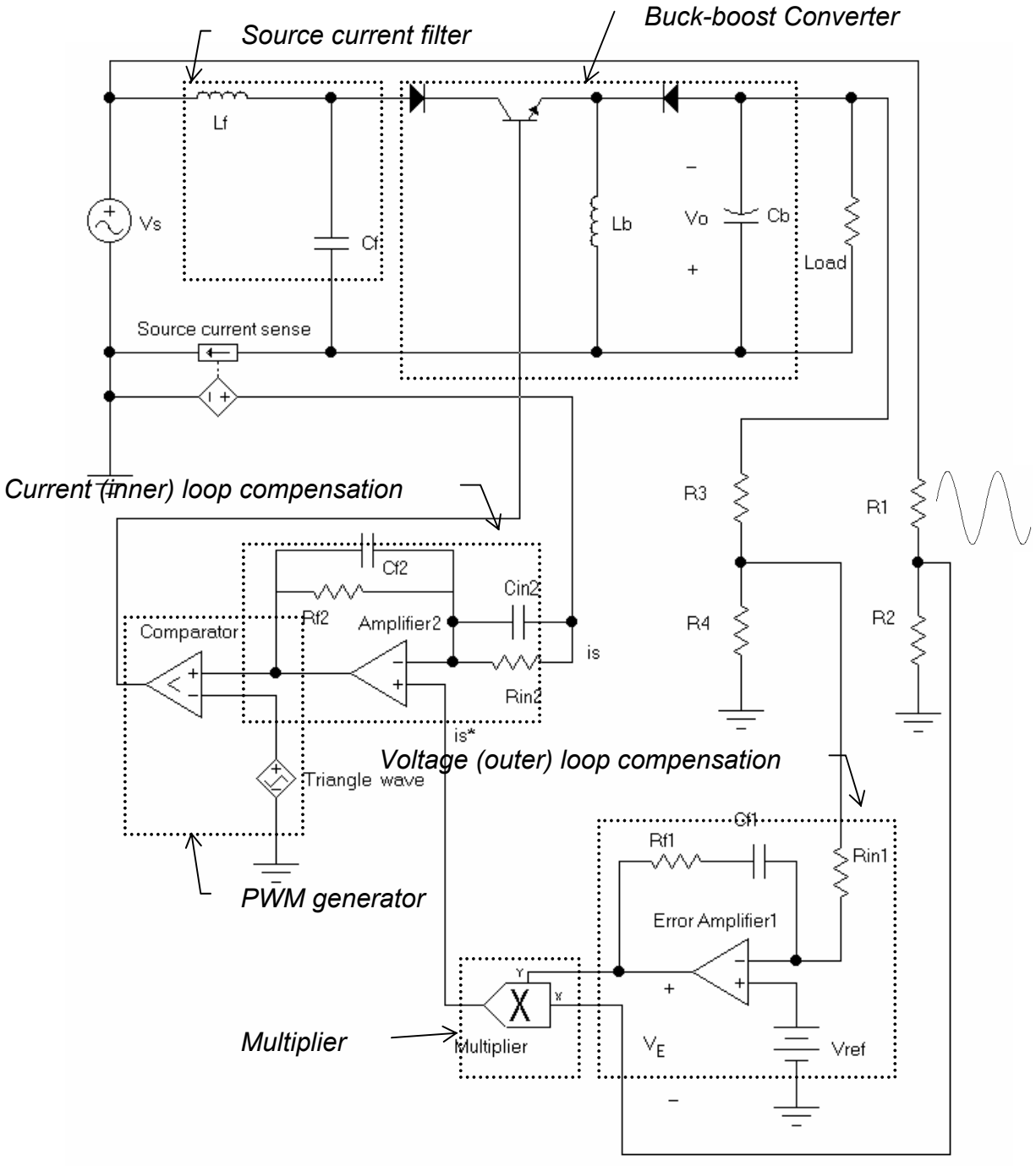

Figure 3.6 Functional diagram of buck-boost type half bridge DC output Power Factor Correction Circuit

3.2 Basic control

To facilitate explanation of the control circuit, Figure 2.1 is redrawn here as Figure 3.6.

3.2.1 Control functional description

As shown in Figure 3.6, Amplifier1, R_{f1}, R_{in1}, and C_{f1} compose a Voltage Compensation Network (VCN). The DC output voltage is sensed by the voltage divider consisting of R_3 and R_4 by the scale of $\frac{R_4}{R_3 + R_4}$. Output of the divider and the output voltage reference (V_{ref}) are sent into the VCN. The output of VCN is the error between the actual DC output and its reference.

A voltage divider formed by R_1 and R_2 scales down the source voltage (v_s) by $\frac{R_2}{R_1 + R_2}$. Output of the multiplier is the product of VCN output and scaled source voltage, which is the necessary source current to regulate the output DC voltage.

Amplifier2, R_{f2}, R_{in2}, and C_{f2} compose a Current Compensation Network (CCN). Source current is sensed and supplied to the inverting terminal of the amplifier. The output of CCN is the amplified error between the desired current reference and actual source current. It is compared with a triangle wave by the PWM generator. The output of the comparator is the necessary gating signal for the power switch. It is applied to the switch driver circuit.

3.2.2 Compensation network sizing

Since the frequency of AC line input is much less than the switching frequency, the AC input can be viewed as slowly varying DC by the converter. Quasi-static approximation [5] is used in designing the current error

compensation network. In quasi-static approximation control design, stability compensation is more critical. The closed loop bandwidth must be large enough that significant phase shift does not occur at the AC input frequency. And, the current loop gain should have a positive phase margin at all operation points in half-cycle of the line input.

To design the current control loop compensation network, it is necessary to find the transfer function that describes how the change in duty cycle changes the input line current. From Appendix A,

$$H(s) = \frac{\hat{i}_{Lf}(s)}{\hat{d}(s)} =$$

$$\frac{s^2 R_1 C_1 L_1 I_{L1} + s[(V_s - V_{C1})DR_1 C_1 + L_1 I_{L1}] + [DD' R_1 I_{L1} + D(V_{Cf} - V_{Cb}) + RD'^2 I_{L1}]}{s^4 R_1 L_f C_f L_1 C_1 + s^3 L_f C_f L_1 + s^2 (R_1 L_1 C_1 + R_1 D^2 L_f C_1 + R_1 L_f C_f D^2) + s(L_1 + D^2 L_f) + R_1 D'^2} \quad (3.1)$$

This is a fourth order system. Since we sense the current before the input filter, there are four energy storage components in the system. In normal operation, the output voltage should have negligible harmonic content. We could assume that the output capacitor is large enough that its effect on the duty-cycle-to-input-current transfer function is negligible. Thus, as shown in Appendix A, the transfer function can be simplified to

$$H(s) = \frac{1}{L_f C_f} \frac{sI_{Lb}(kT_s) + \frac{D(kT_s)}{L_b}[V_s(kT_s) - V_{Cb}(kT_s)]}{s(s^2 + \frac{1}{L_f C_f} + \frac{D(kT_s)^2}{L_b C_f})} \quad (3.2)$$

When the output power is 300 watts, and the circuit element values of L_f = 1.5 mH, C_f = 15 uF, L_1 = 1mH, and C_1 = 2 mF are used, the bode plot of the transfer function at the input voltage peak is shown in Figure 3.7. At its cut-off frequency the system has about -8^0 phase margin. So, the system is not stable without necessary compensation. To increase the phase margin of the system, a lead compensator is added to the CCN. Figure 3.8 shows the system bode plot after

the compensator is added. After the lead compensator is added into the system, the phase margin is improved to about 31^0. To assure the system stability, the system transfer function must be checked for the complete output power range and the entire input voltage range.

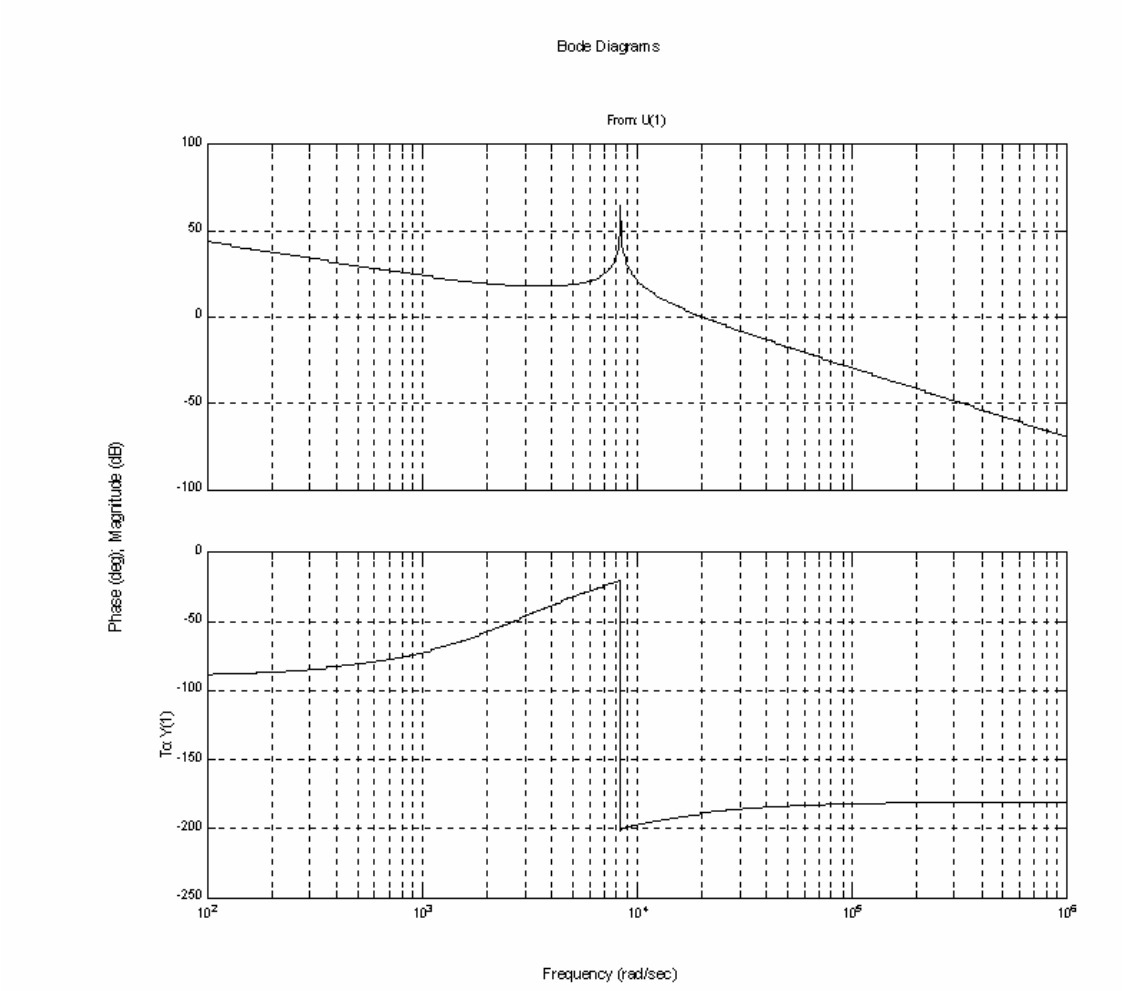

Figure 3.7 Bode plot of control-to-input-current transfer function

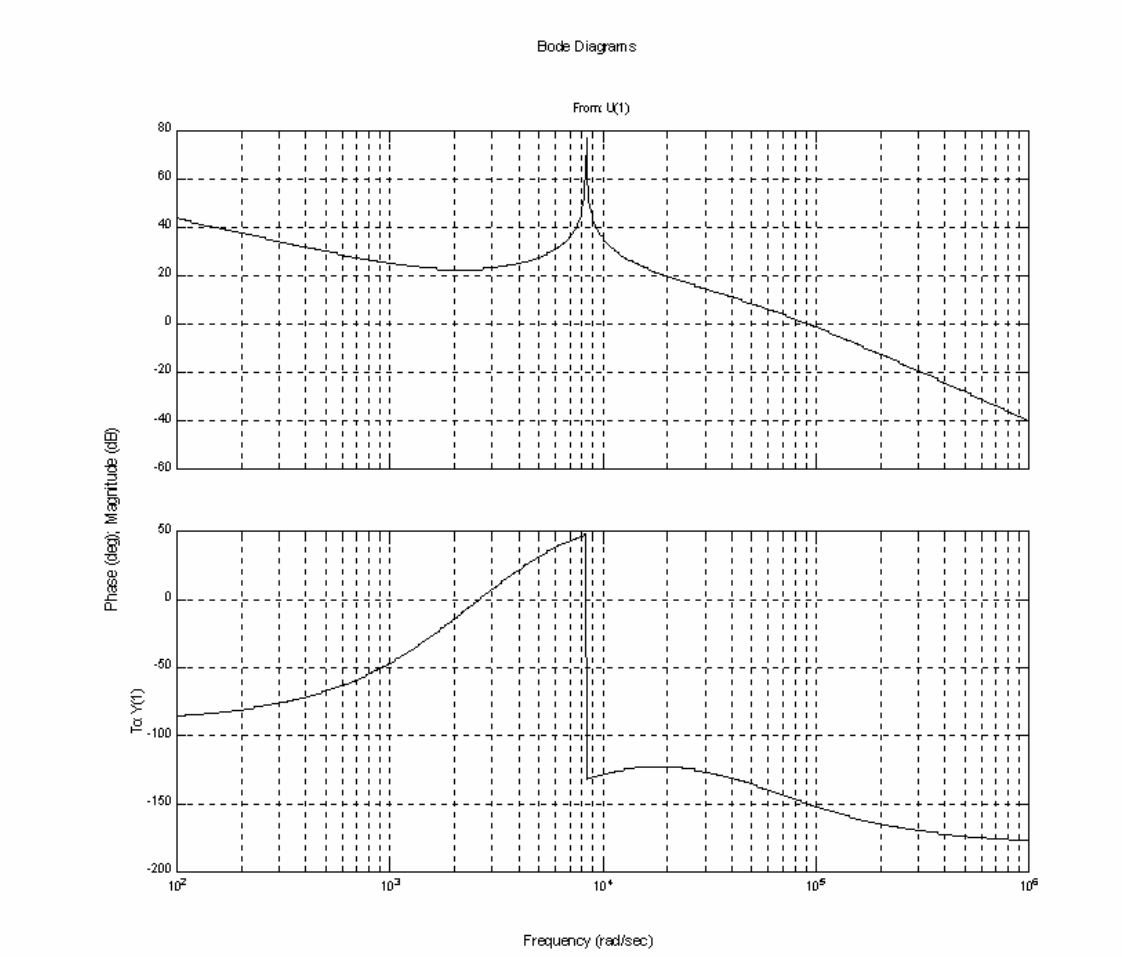

Figure 3.8 Bode plot of control-to-input-current transfer function with lead compensator

3.3 Zero-crossing distortion

Due to the capacitance in the source current filter, the source current will have a leading phase with respect to the source voltage as illustrated by Figure 3.9. The PFC objective is to maintain the fundamental component of converter input current in phase with the source voltage. However, the converter input current is discontinuous rendering it a poor choice from a control point of view to use as input to the CCN. On the other hand, the source current is a high quality sinusoidal waveform suitable for use by the CCN. If the source current is simply

sensed as feedback to the CCN, significant distortion in the source current results in the region of signal zero crossings. Figure 3.10 shows the command current and the resulting source current waveforms from a simulation.

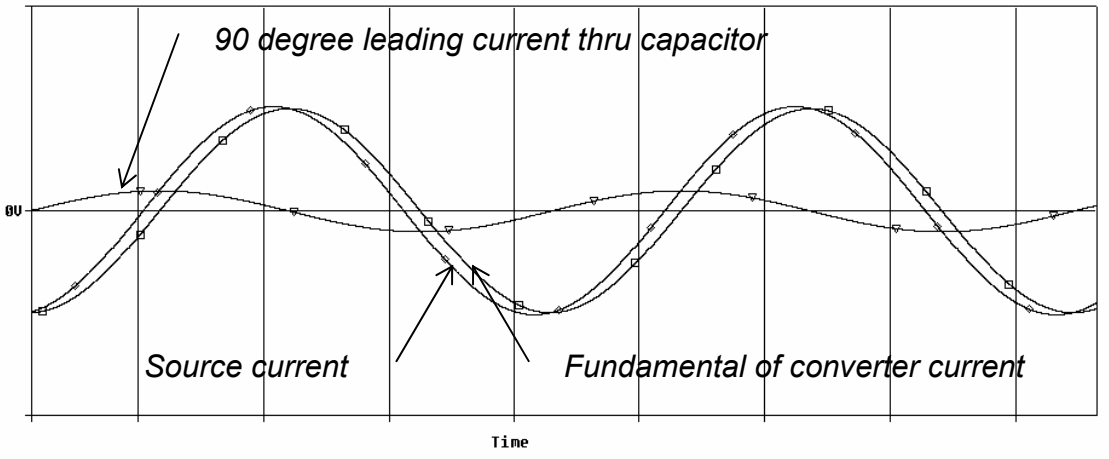

Figure 3.9 Source current leading due to filter capacitor

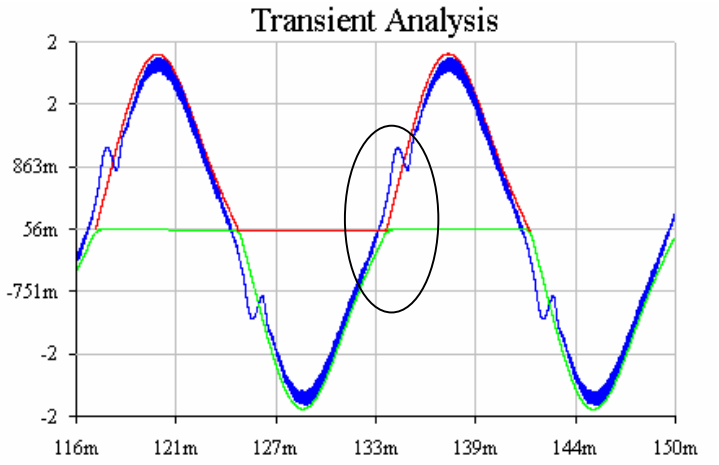

Figure 3.10 Current distortion at zero-crossing

Figure 3.11 shows the detailed waveforms circled in Figure 3.10. When the source current crosses zero, current through filter capacitor is dominant. This current is leading the source voltage, and thus, leading the current reference command. In our control scheme, current error signal is

$$Verr(s) = \frac{R_{f2}(1+SR_{in2}C_{in2})}{R_{fn2}(1+SR_{f2}C_{f2})}(i_s^* - i_s) \tag{3.3}$$

where i_s^* is source current reference and i_s the sensed source current.

If the source current is leading its reference, $V_{err}(s)$ will be a negative value as the current command signal passes the zero crossing point. When this voltage is compared to triangle wave to produce necessary PWM gating signal for the switches, there will be a short "dead period" with no gating signals for the switches. So, the fundamental frequency current component into in the buck-boost will be like unto the solid line with squares shown in Figure 3.11. There is a rapid increase after the voltage zero-crossing, due to the accumulated output voltage error in the "dead period".

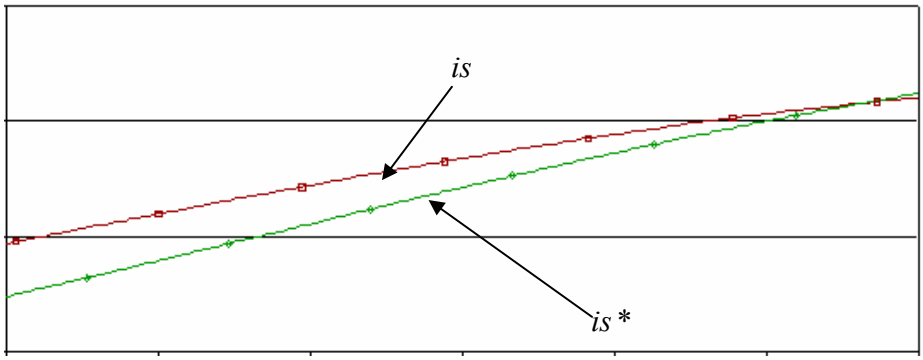

Figure 3.11 Close view of source currents crossing zero

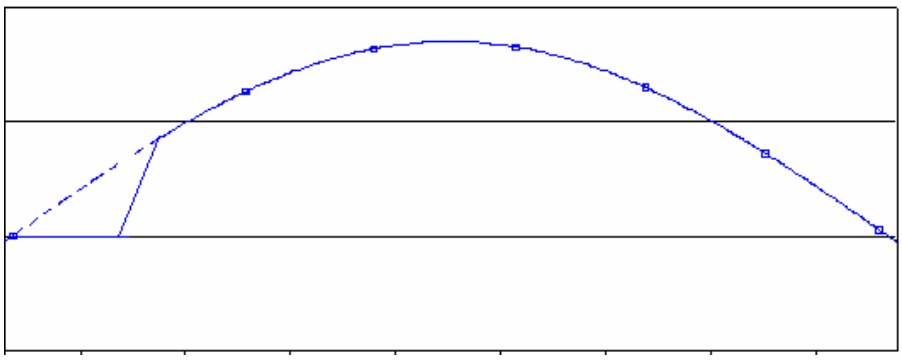

Figure 3.12 Input current zero-crossing distortion due to filter capacitor current

Figure 3.12 illustrates the ideal case that the source current catches up its reference immediately with no overshoot. In the real circuit, the transient process may cause the source current overshoot and oscillate for some time. This is just what we have found in Figure 3.10.

In order to eliminate the zero-crossing distortion due to the effect of the filter capacitor, it is necessary to subtract the current through the capacitor from the sensed source current prior to processing the signal by the CCN. Figure 3.13 shows the control circuit after 90 degree lagging signal is injected into the sensed source current by the Delay Network.

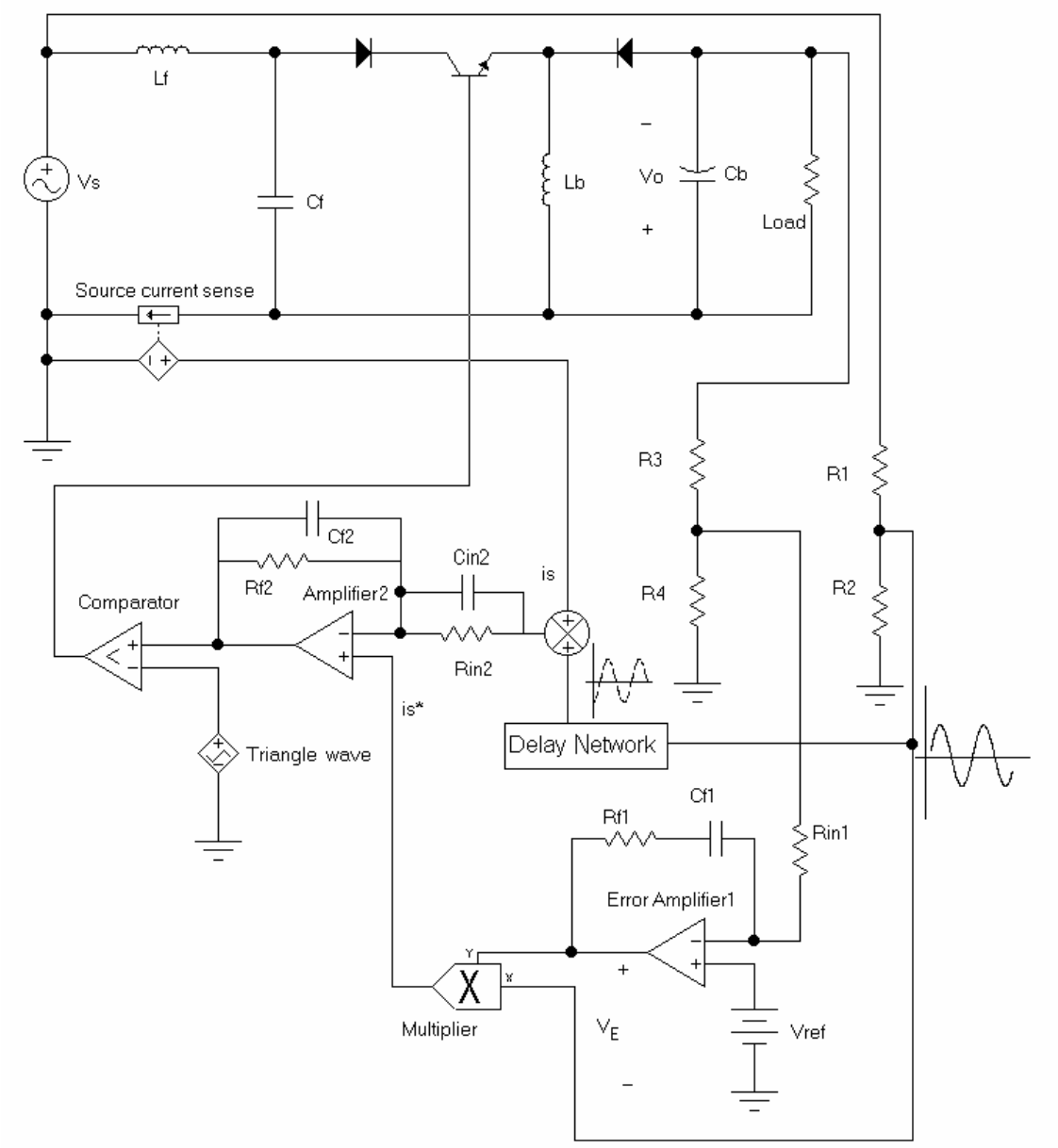

Figure 3.13 Delayed signal injection into sensed source current for elimination of effect from filter capacitor current

To produce a Delay Network with a voltage 90 degrees ahead of input voltage, a differentiation circuit is a good choice. Figure 3.14 shows a basic differentiation circuit. Its output is

$$vo = -RC\frac{dvs}{dt}$$

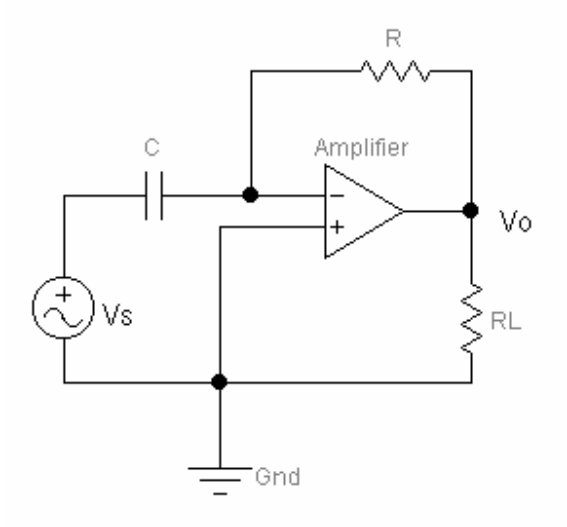

Figure 3.14 Differentiation circuit

If $vs = \cos(\omega t)$, then $vo = \omega RC \sin(\omega t)$. Figure 3.15 shows the input and output waveforms, when R=10 K, and C=1 uF. Its transfer function is

$$H(s) = -sRC \tag{3.4}$$

Obviously, magnitude of the output is linearly proportional to the frequency of its input. So, this circuit is very sensitive to electronic noise of high frequencies. In worst case, the useful information could be overwhelmed by high frequent noises.

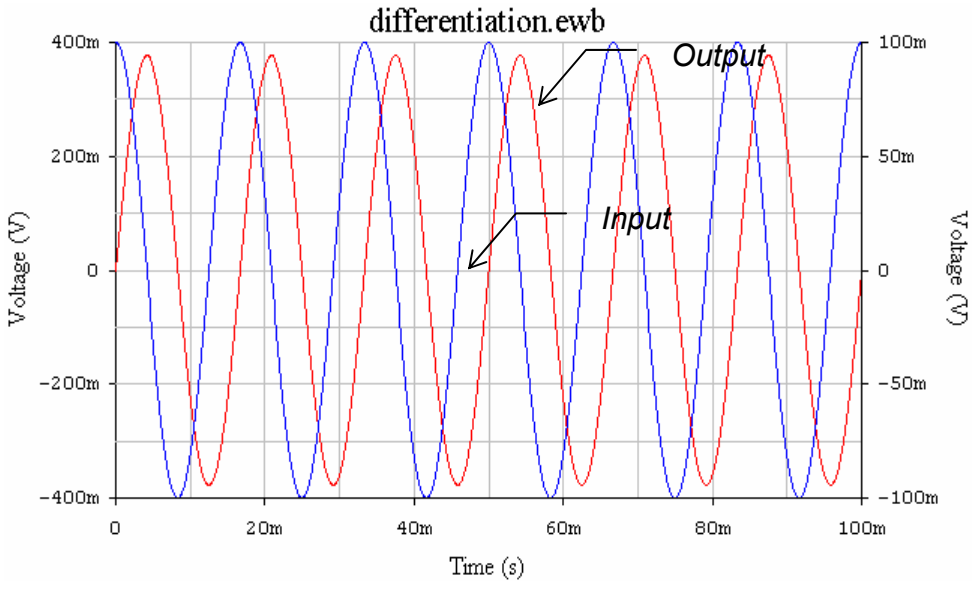

Figure 3.15 Input and output waveforms of differentiation circuit

To make the current injection idea applicable, the basic differentiation circuit must be modified to suppress high frequency harmonics. Figure 3.16 shows an improved differentiation circuit to avoid the shortcoming of the circuit in Figure 3.14. The input impedance Z_{in}, feedback impedance Z_f, and the resulting transfer function H(s) are formed.

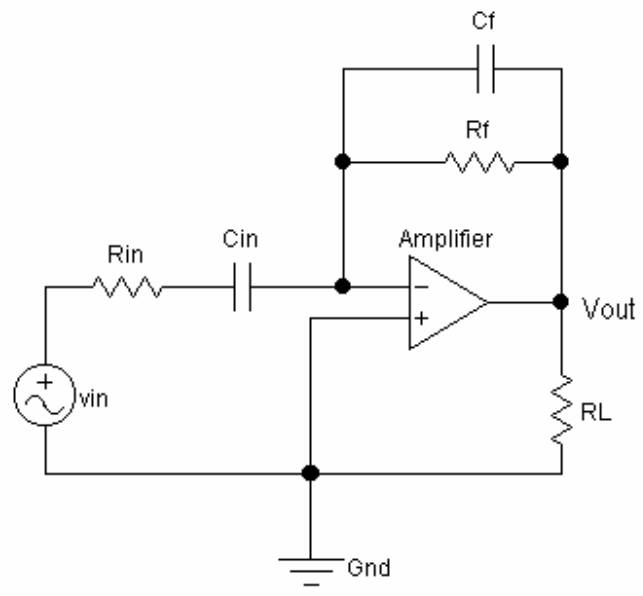

Figure 3.16 Modified differentiation circuit to reduce noise

$$Z_{in} = R_{in} + \frac{1}{sC_{in}} = \frac{1 + sR_{in}C_{in}}{sC_{in}}$$

$$Z_f = \frac{R_f \frac{1}{sC_f}}{R_f + \frac{1}{sC_f}} = \frac{R_f}{1 + sR_fC_f}$$

$$H(s) = -\frac{Z_f}{Z_{in}} = -\frac{\frac{R_f}{1 + sR_fC_f}}{\frac{1 + sR_{in}C_{in}}{sC_{in}}} = -\left(\frac{R_f}{1 + sR_fC_f}\right)\left(\frac{sC_{in}}{1 + sR_{in}C_{in}}\right) \qquad (3.5)$$

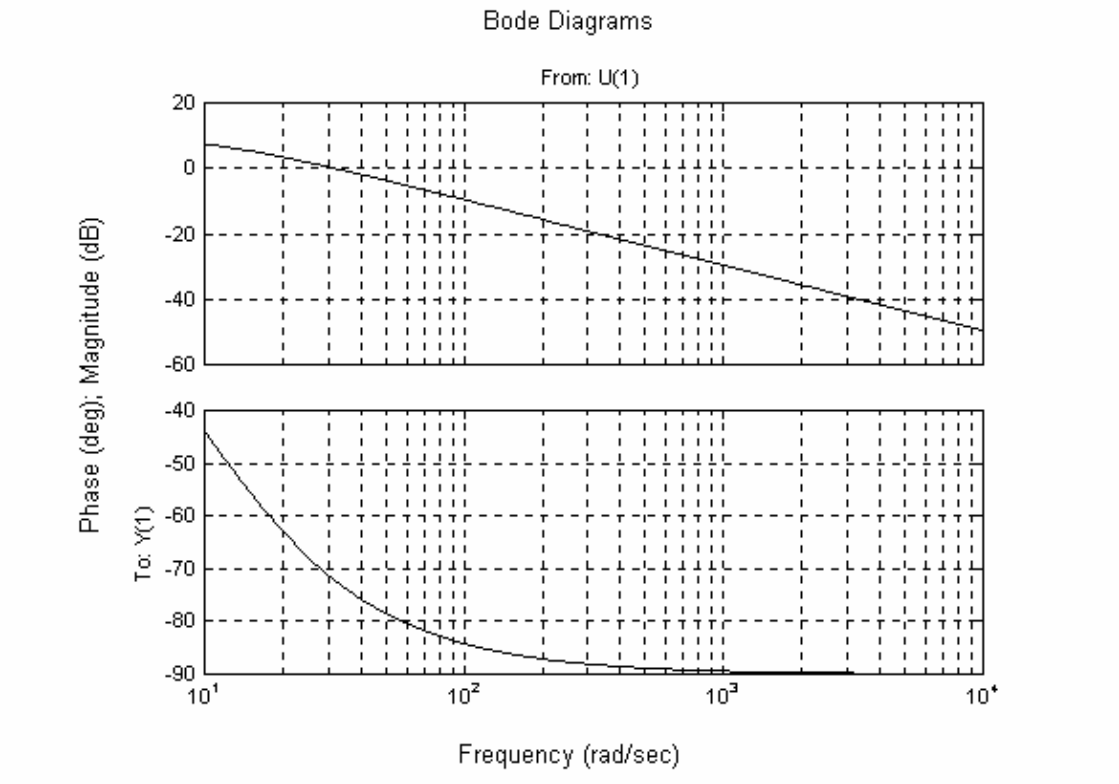

Figure 3.17 Characteristic bode plot of modified differentiation circuit

Figure 3.17 is the characteristic bode plot of the differentiator circuit. It is obvious that noises of high harmonic frequencies are suppressed.

To size the components in the Delay Network, it is noted that we want the injected signal to offset the current through the filter capacitor C_f, when the source current leads the line voltage. So, the component can be chosen by letting amplitude of the output of the Delay Network equal to amplitude of the scaled voltage due to current through the filter capacitor according to the scale of the current sensor.

Because of a very low voltage drop on the filter inductor, voltage across the filter capacitor is approximately equal to the source voltage. Current through the filter capacitor is

$$\bar{I}_c = \frac{\bar{V}_s}{-j\frac{1}{\omega C}} \tag{3.6}$$

Denote the scaling factor of the current transducer as k_i, and the voltage divider scaling factor as k_v. Then we have the following equation

$$k_i I_c = k_v |H| V_s \tag{3.7}$$

From Equation 3.7, the magnitude of the transfer function $H(s)$ at line frequency can be obtained as

$$|H(s)| = \frac{k_i I_c}{k_v V_s} \tag{3.8}$$

To assure that no remnant harmonic of switching frequency exists, components for the Delay Network is chosen so that more than 60 dB attenuation is obtained at switching frequency.

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9. J. Sun, “Demystifying zero-crossing distortion in single-phase PFC converters,” in Records of 2002 IEEE Power Electronics Specialists Conference, June 2002, pp1109-1114.
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4. Design, Simulation, and experimental results

The design of a 300-Watt, 45-volt DC output voltages, buck-boost based, unity power factor, half-bridge, dual output converter is presented in this chapter. Its simulation and physical implementation is discussed.

4.1 Power stage design

Specifications of the converter are given as follows,
Input voltage: 110 ± 20 V RMS
Output voltage: ±45 V
Switching frequency: 20 kHz
Inductor current ripple: 20% of peak current
Output voltage ripple: 5% of DC voltage
Output Power 300 W
Efficiency: 90%

Maximum input RMS current occurs when the input voltage is 90 V RMS. Assuming a unity input power factor,

$$I_{\max RMS} = \frac{P_{out}}{\eta V_{\min}} = \frac{300}{0.9 \quad 90} = 3.7 \text{ A}$$

Assuming a fundamental frequency input current waveform, the maximum input peak current is $I_{\max peak}$ = 5.23 A.

For a buck-boost converter, the switch current is pulse series of switching frequency. The peak switch current is significantly larger than the line peak

current. The largest peak to peak currents through the power switch and the inductor occur at the peak value of the line current, when the input voltage to the converter is at its peak value. And, at this time point, the CCM instantaneous duty ratio for the gating signal is follows from (2.2.7) as

$$d = \frac{1}{1+\frac{V_m}{V_o}} = \frac{1}{1+\frac{90\times\sqrt{2}}{45}} = 0.261$$

Letting the largest peak-to-peak inductor current ripple be equal to 20 percent of the fundamental peak of the inductor current gives

$$\Delta I_{L\max} = \frac{V_m}{L} DT_s \sin(k\omega T_s)\Big|_{k\omega T_s=\frac{\pi}{2}} = 0.2\, I_{\max peak}$$

Solving the equation, we can obtain the necessary value of the buck boost converters inductance as

$$L = \frac{V_m DT_s}{0.2\times I_{\max peak}} = \frac{60\times\sqrt{2}\times 0.261}{0.2\times 4.25\times 20\times 10^3} = 1.3 \text{ mH}$$

Selection of output filter capacitance follows from the procedure of section 2.2.5, using Equations 2.2.17 and 2.2.18,

$$T_{off} = \mathrm{Re}\{1-\frac{1}{2\sqrt{1-(\frac{V_m}{V_o})^2}}+\frac{\tan^{-1}[\frac{V_m}{V_o\sqrt{1-(\frac{V_m}{V_o})^2}}]}{\pi\sqrt{1-(\frac{V_m}{V_o})^2}}\}T$$

$$= \mathrm{Re}\{1-\frac{1}{2\sqrt{1-(\frac{179}{45})^2}}+\frac{\tan^{-1}[\frac{179}{45\times\sqrt{1-(\frac{179}{45})^2}}]}{\pi\sqrt{1-(\frac{179}{45})^2}}\}\times\frac{1}{60}$$

= 0.0136 sec

$$C_f = \frac{I_o T_{off}}{\Delta V_o}$$

$$= \frac{3.33 \times 0.0136}{45 \times 0.05}$$

= 20.1 mF

Equation 2.2.13, 2.2.14, and 2.2.15 are used to appropriately select a transistor, diode, and inductor of adequate current ratings.

$$I_{RMS}^{sw} = I_{\max RMS}^{src} \sqrt{\frac{1}{2} + \frac{V_m}{V_o} \frac{4}{3\pi}}$$

$$= 3 \times \sqrt{\frac{1}{2} + \frac{120 \times \sqrt{2}}{45} \frac{4}{3\pi}}$$

= 4.35 A

$$I_{RMS}^{d} = I_{\max RMS}^{src} \sqrt{\frac{V_m}{V_o}(\frac{4}{3\pi} + \frac{V_m}{V_o} \frac{3}{8})}$$

$$= 3 \times \sqrt{\frac{120 \times \sqrt{2}}{45}(\frac{4}{3\pi} + \frac{120 \times \sqrt{2} \times 3}{45 \times 8})}$$

= 7.9 A

$$I_{RMS}^{ind} = I_{\max RMS}^{src} \sqrt{\frac{1}{2} + \frac{8V_m}{3V_o\pi} + \frac{3{V_m}^2}{8{V_o}^2}}$$

$$= 3 \times \sqrt{\frac{1}{2} + \frac{120 \times \sqrt{2}}{45}(\frac{8}{3\pi} + \frac{120 \times \sqrt{2} \times 3}{45 \times 8})}$$

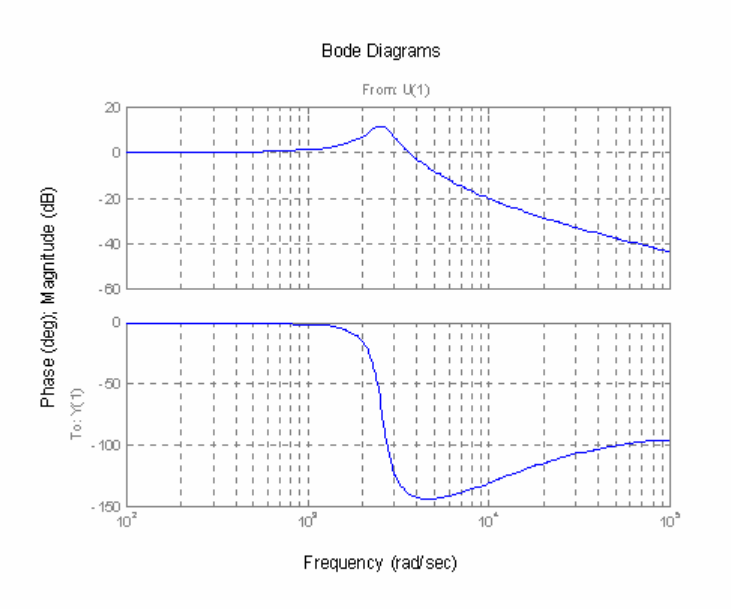
= 9.02 A

The input filter is connected between the AC source and the converter to reduce the AC line harmonics. It is designed to provide an attenuation of more than 20dB at switching frequency while offering negligible attenuation to the source frequency. The somewhat arbitrarily selected values of the filter components are listed below:

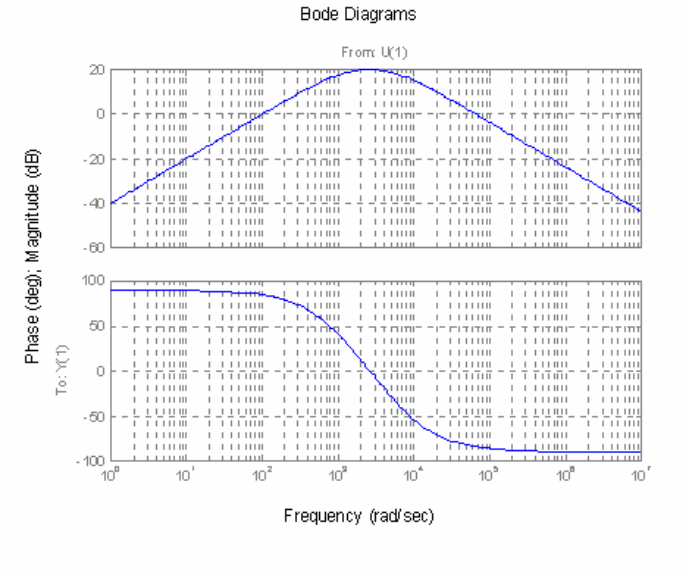
L_f = 1.5 mH

C_f = 15 uF

R_f = 20 ohms



(a)



(b)

Figure 4.1 Bode plots; (a) filter current transfer function, (b) filter output impedance

Bode plots of the filter current transfer function and its output impedance, as discussed in section 2.3, are displayed as Figure 4.1. At switching frequency, attenuation of -30 dB is obtained. And, the output impedance of the filter is -5 dB or 0.56 ohm.

4.2 Control loop designs

Figure 4.2 illustrates the specific realization of the outer (voltage) loop configuration discussed in section 3.2.1. The output voltage is inverted and compared with its reference V_{ref}. A PI controller is added to remove any error between output voltage reference and its actual value. The resulting error signal is amplified and multiplied with the scaled line voltage. A low-pass filter is added to the line voltage divider to remove any electromagnetic interference from the power stage. A wide bandwidth precision analog multiplier MPY634 is used to obtain the source current reference available from pin 12.

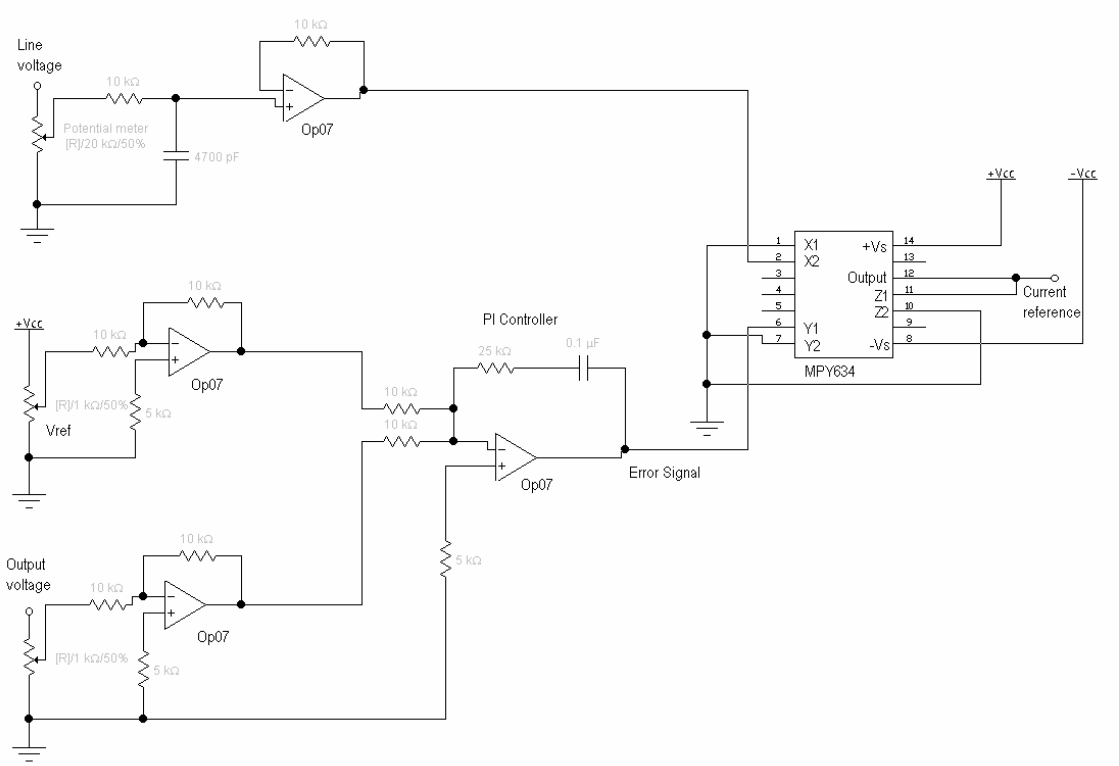


Figure 4.2 Outer (voltage) control loop configuration

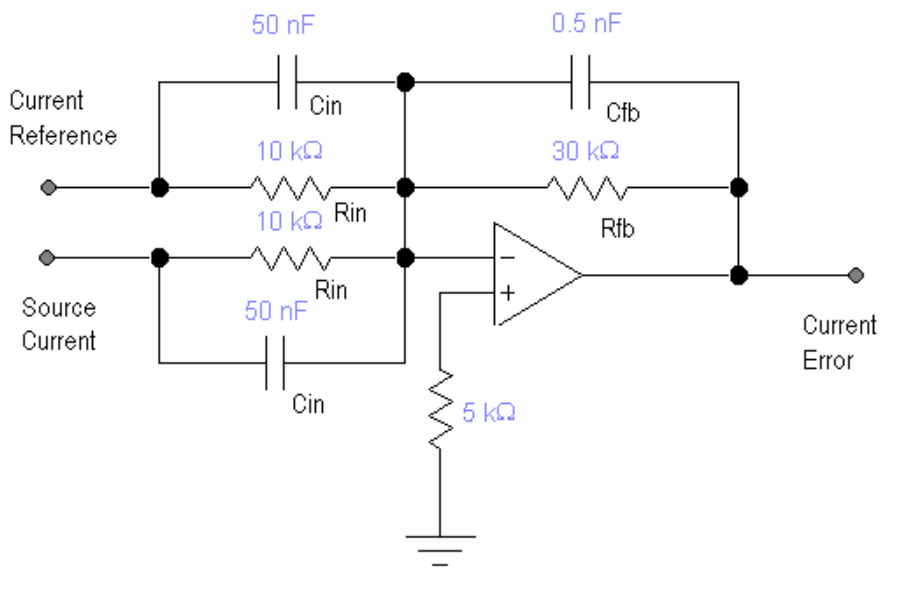


Figure 4.3 Inner (current) loop configuration

The source current reference is fed to the inner (current) loop configuration as discussed in section 3.2.1. The realization of the inner loop control is displayed by Figure 4.3. The transfer function of the circuit is

$$H(s) = \frac{R_{fb}}{R_{in}} \frac{1 + sR_{in}C_{in}}{1 + sR_{fb}C_{fb}}$$

Choice of $\frac{1}{R_{in}C_{in}}$ = 2000 s^{-1}, $\frac{1}{R_{fb}C_{fb}}$ = 60000 s^{-1} provide proper compensation to stabilize the system. Figure 4.4 illustrates the bode plot of the resulting control-to-input-current transfer function with compensation as discussed in section 3.2.2.

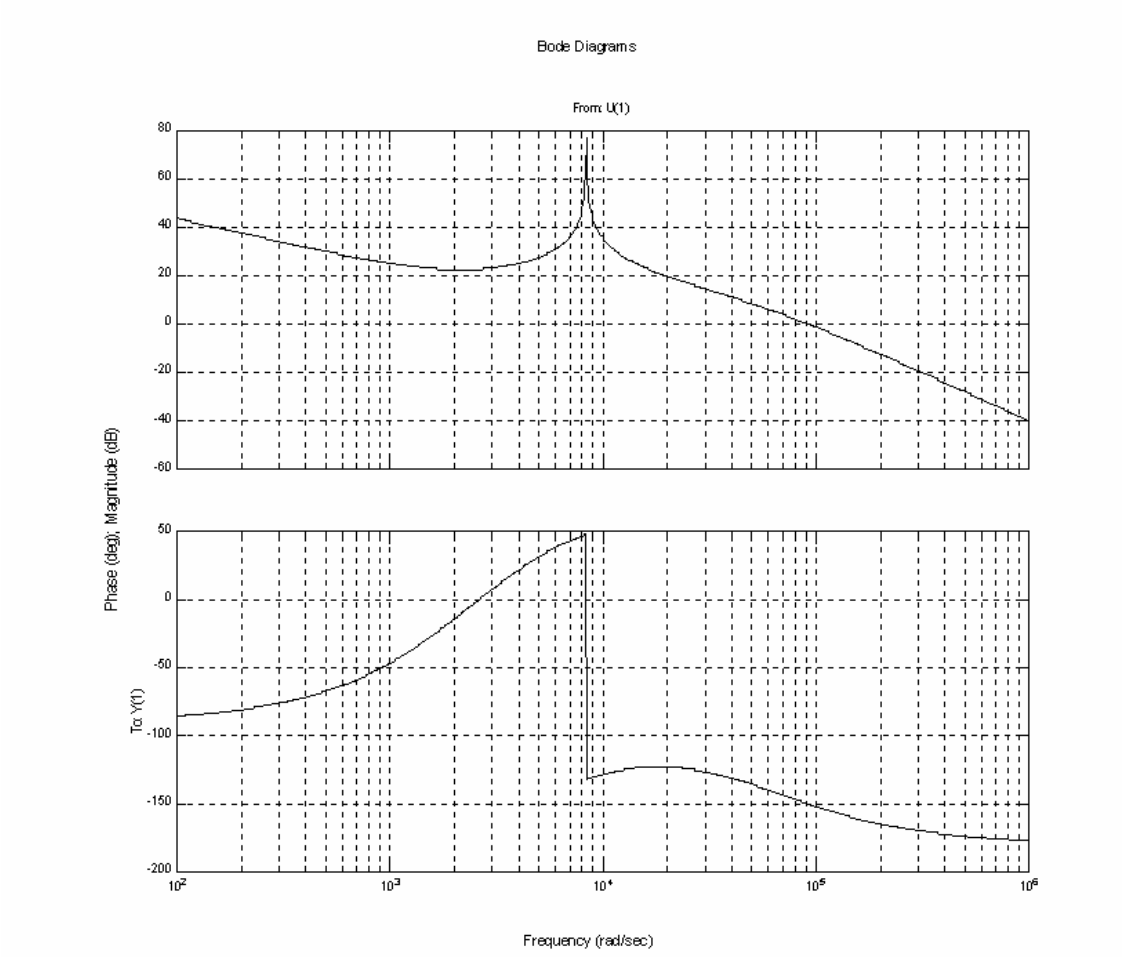


Figure 4.4 Bode plot of control-to-input-current transfer function with compensation

4.3 Simulation Results

The complete closed-loop system is simulated using MultiSIM 2000 software. Figure 4.5 illustrates the resulting line voltage and line current without the filter delay signal injection discussed in section 3.3. Figure 4.6 illustrates the line voltage and line current with the delay signal injection active. The improvement in quality of the input current waveform is apparent.

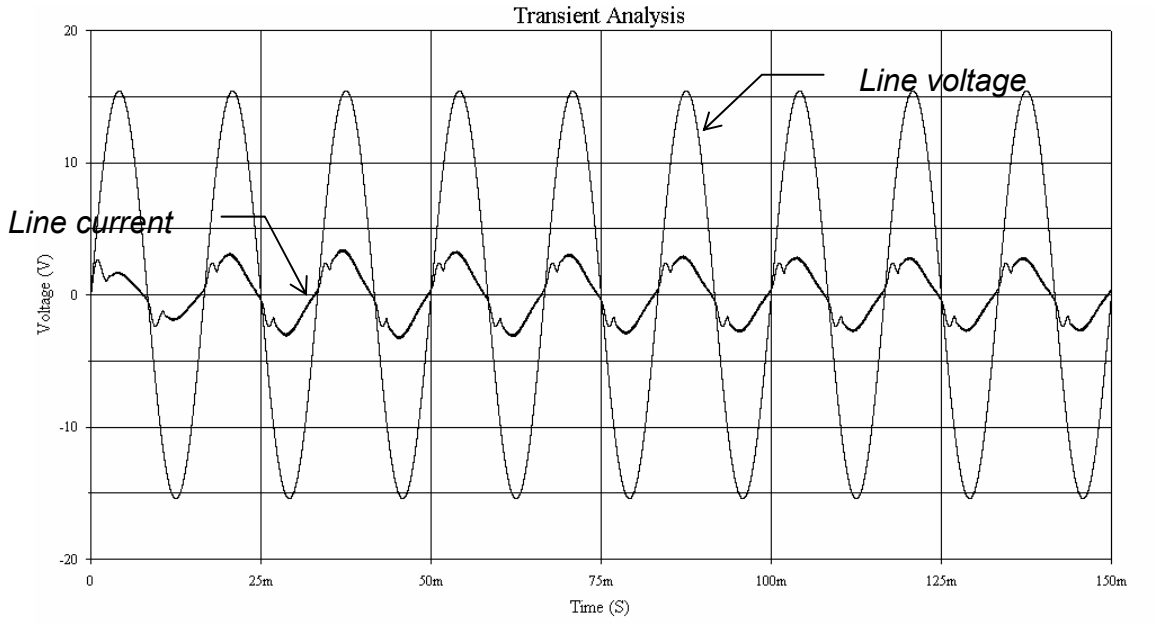


Figure 4.5 Simulation result of line voltage and line current without delay signal injection

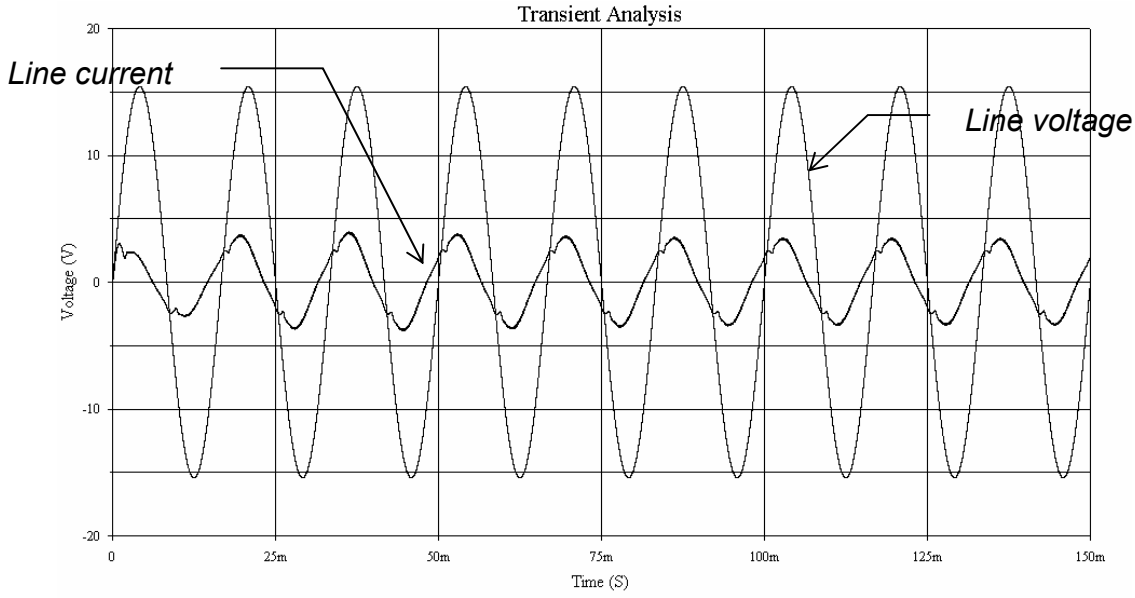


Figure 4.6 Simulation result of line voltage and line current with delay signal injection

Figure 4.7 shows the two DC output resulting from the simulation. DC component of the output voltages is 45 volts. The peak-to-peak AC ripple in the voltages is about 2 volts, which is 4.5% of the specific DC value.

Figure 4.8 and 4.9 illustrate the source current error signal without and with the delay network active. Without the delay network active, there is a small dead area in every positive half line cycle, during which the line voltage cross zero. After the delay network works actively, the dead area is significantly shortened. It decrease the zero-crossing distortion in the line current, and thus, improve the line current waveform.

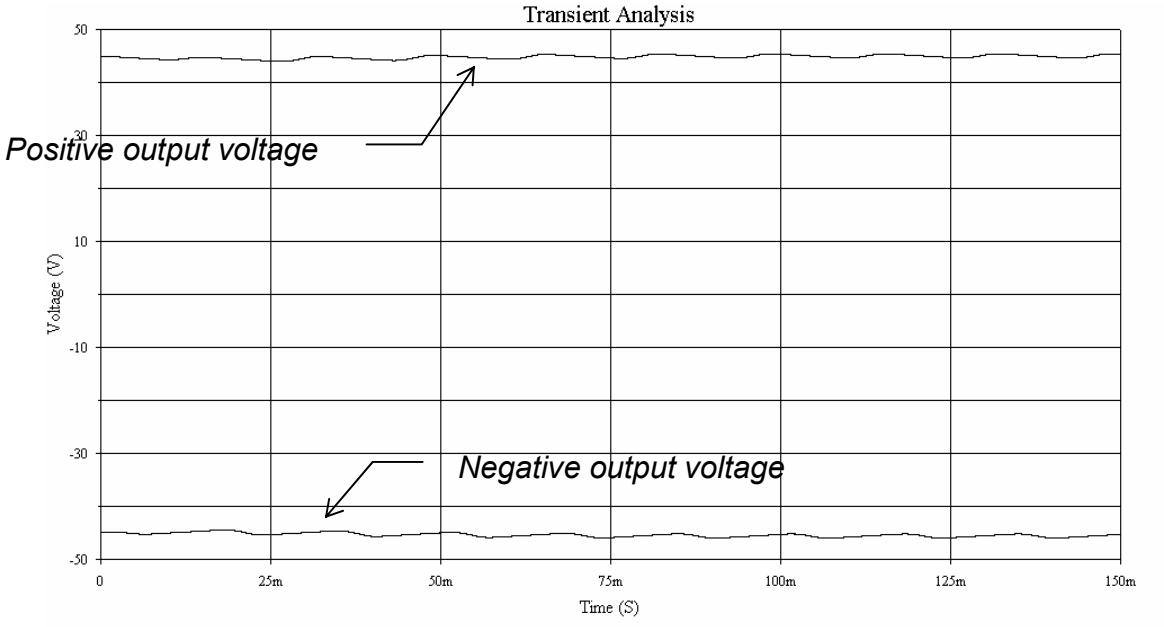


Figure 4.7 DC output voltages

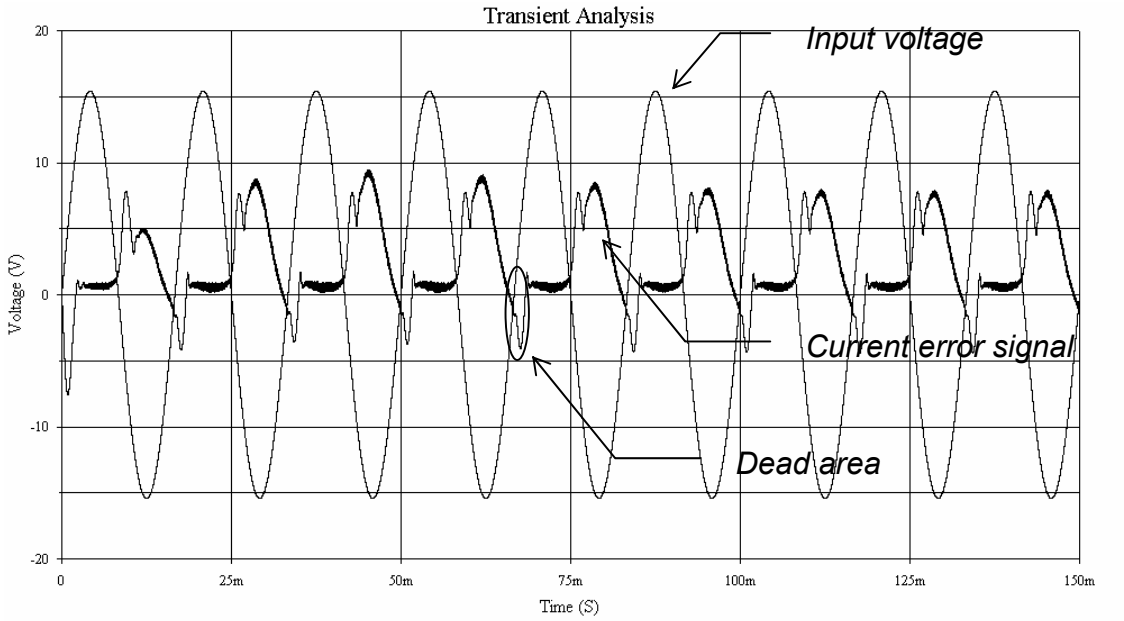


Figure 4.8 Outer loop current error signal without delay signal injection

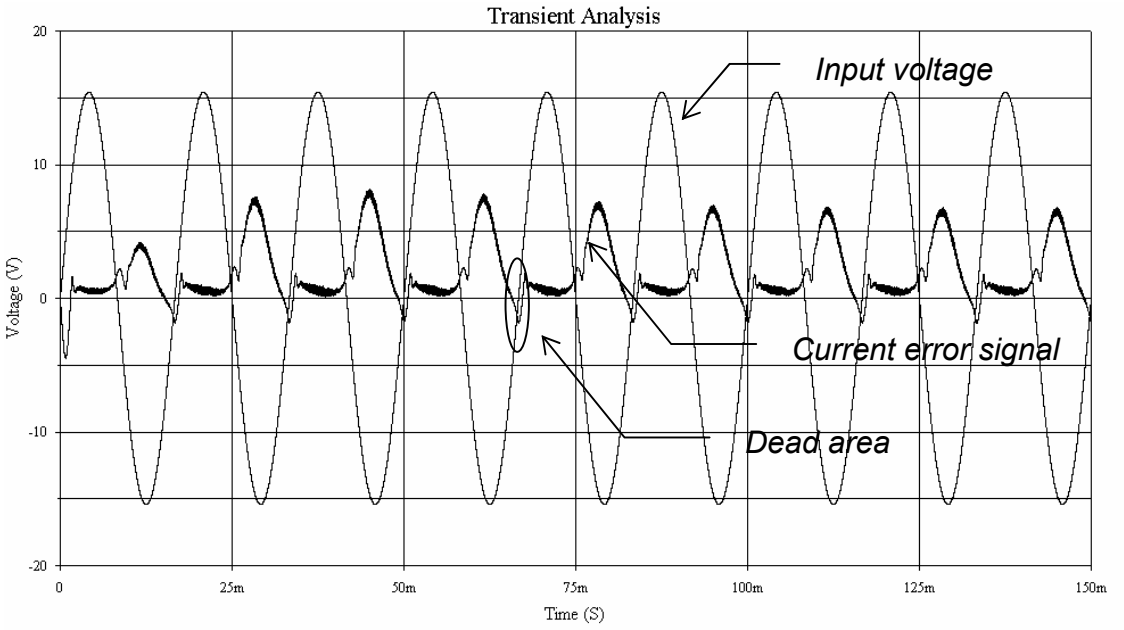


Figure 4.9 Outer loop current error signal with delay signal injection

4.4 Experimental buildup and data

The buck-boost based, unity power factor, half-bridge, dual output converter is built up using the component values identical to the simulation. It is anticipated that the dual output converter will later utilize the high blocking voltage, low forward voltage drop, fast switching CVD diamond triode as switching devices. The technology has not yet advanced to the point that these devices are ready for test application. Hence, the converter proof-of-principle development work at this point must use available switching devices.

4.4.1 Power circuit

The power level circuit of the converter is shown in Figure 4.10. An IRG4PF50W (V_{CES} = 900V, $V_{CE(on)typ.}$ = 2.25V I_C =28A) IGBT from International Rectifier is selected as the switching device, due to its low switching and conduction losses. The turn-off snubber circuits, each consisting of a diode, a resistor, and a capacitor, are connected parallel with the switching components. Turn-on snubber circuits, each consisting of a diode, a resistor and an inductor, are connected in series with the IGBTs. Fast recovery diodes DSEI60-06A (V_{RSM} = 600 V, V_{RRM} = 600 V, I_{RM} = 21 A, t_{rr} = 50ns) from IXYS Semiconductor are selected as free-wheeling diodes (D_2, D_4). Snubber circuits consisting of resistor and capacitor are connected across the free-wheeling diodes.

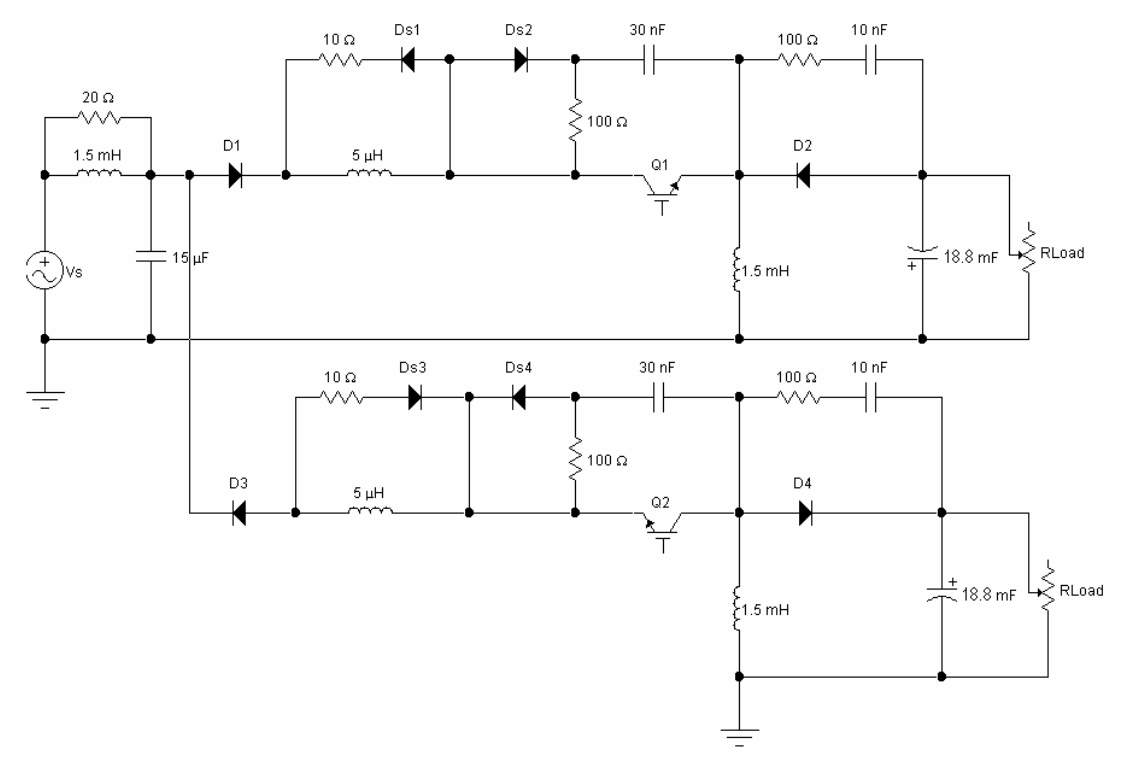


Figure 4.10 Main circuit of the buck-boost based, unity power factor, half-bridge, dual output converter

4.4.2 Gate drive circuit

A Mitsubishi hybrid IC M57962L is used as the gate driver for the IGBTs. The M57962L is a hybrid integrated circuit designed for driving n-channel IGBT modules in any gate amplifier application. This device operates as an isolation amplifier for these modules and provides the required electrical isolation between the input and output with an opto-coupler. Short circuit protection is provided by a built in desaturation detector. A fault signal is provided if the short circuit protection is activated. Figure 4.11 presents a block diagram of the M57962L.

The PWM signal from the comparator of Figure 3.13 is impressed between Pin 14 and 15. The IGBT gate driver signal is obtained from Pin 5. The opto-coupler provides isolation between input PWM signal and output gating

signal. Figure 4.12 shows typical application connection as recommended by the manufacture.

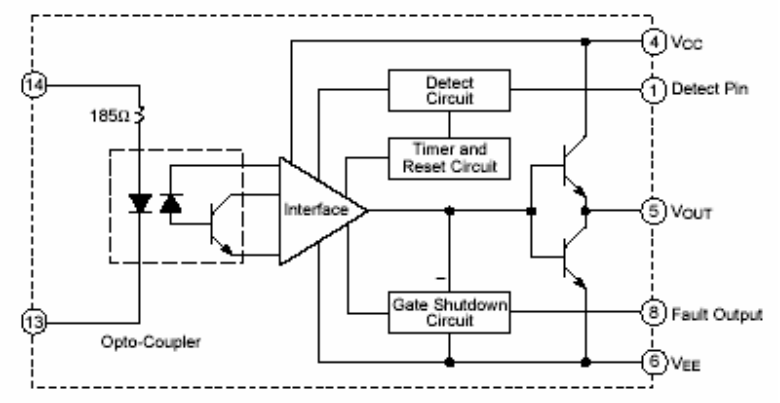


Figure 4.11 Block diagram of IGBT driver M57962L

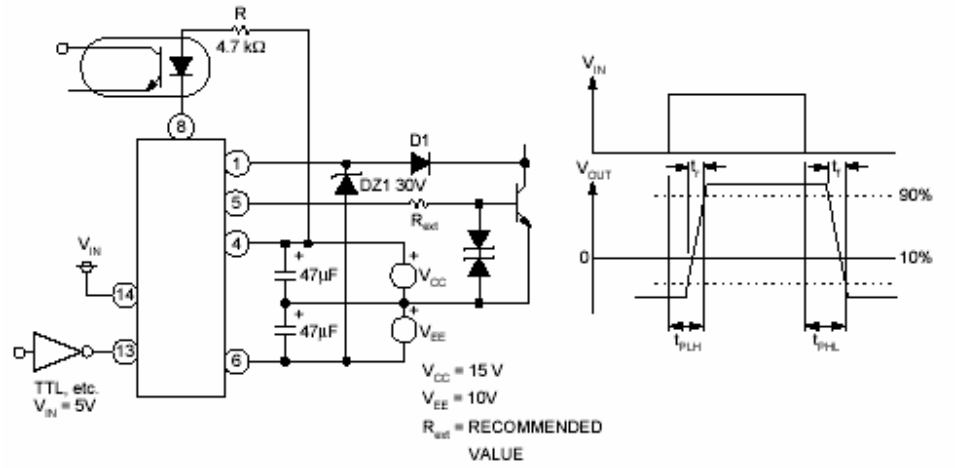


Figure 4.12 Typical application of M57962L

Since the power switch of the buck-boost converter is not grounded, the gate drivers circuit for the switch needs isolated power supplies. The M57962L requires +15 V and -7 V supply voltages to provide an adequate IGBT switching on and off voltage level. Figure 4.13 displays a diagram of the IGBT driver power supply used where the voltage regulators 7815 and 7910 are used to get stable positive and negative driving voltages.

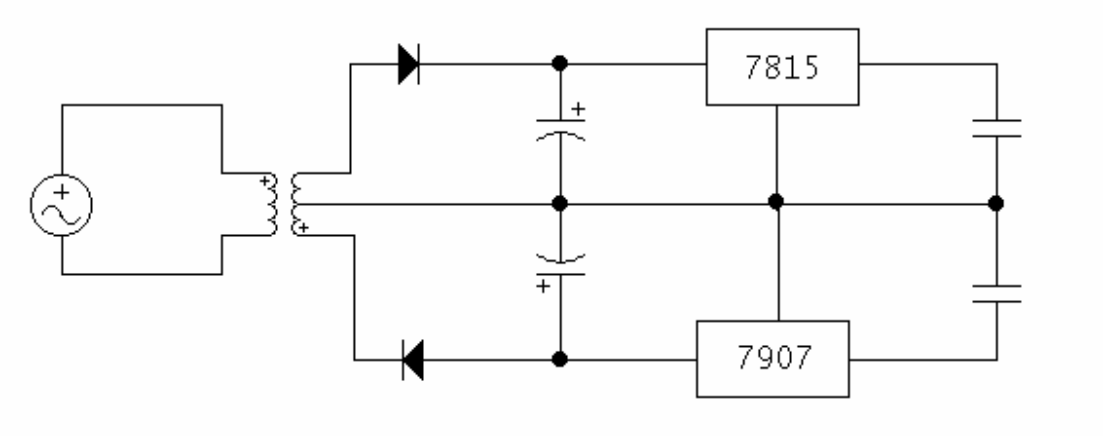


Figure 4.13 IGBT driver power supply diagram

4.4.3 Current sensing

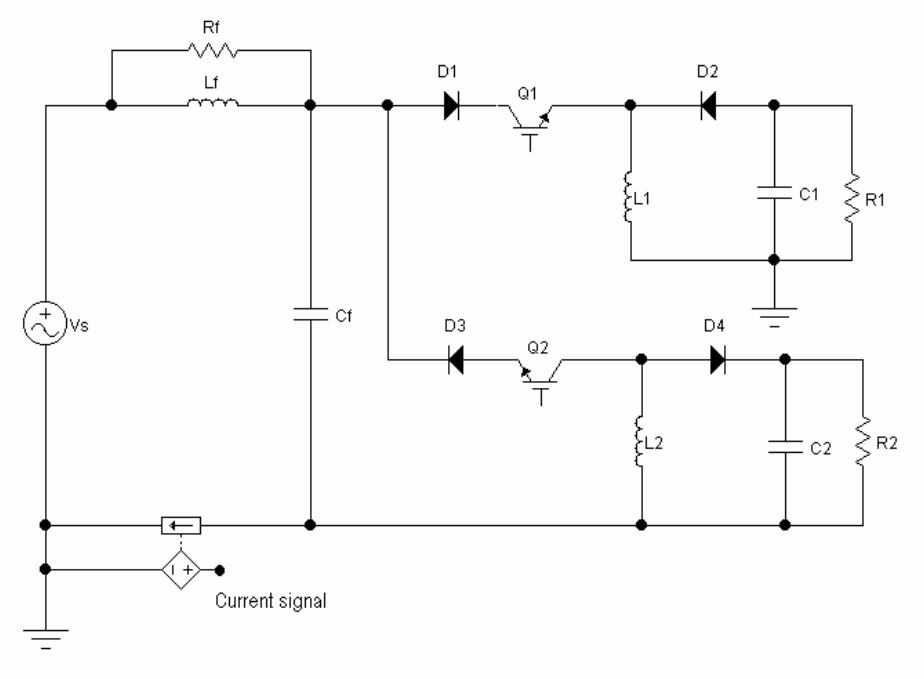
A current transducer LA 05-PB is utilized to sense the source current. This current transducer uses the Hall effect principle. Its output is a voltage signal. The deive is suitable for printed circuit board mounting. It is applicable in AC variable speed drives, servo motor drives, static converters for DC motor drives, uninterruptible power supplies (UPS), and switched mode power supplies (SMPS). [5] Figure 4.14 illustrate the appearance of the transducer. Table 4.1 list the electrical parameters of the current transducer.

Figure 4.14 Appearance of LA 05-PB current transducer

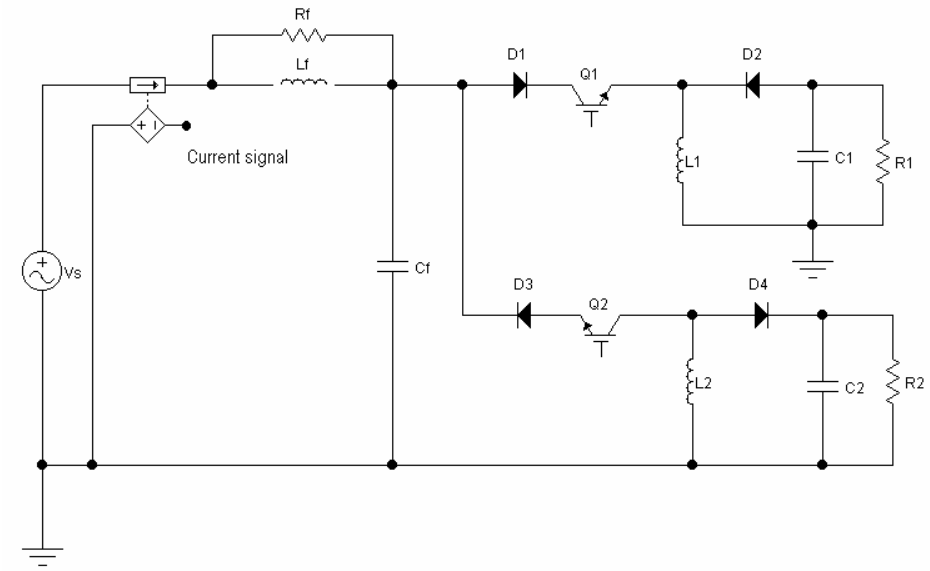
Table 4.1 Electrical parameters of LA 05-PB

V_C	Supply voltage (± 5 %)	± 15	V
I_C	Current consumption	app. 20mA+ I_{PN}/1200	mA
V_d	R.m.s. voltage for AC isolation test, 50/60Hz,1mn	2.5	kV
R_{IS}	Isolation resistance @ 500 VDC	> 500	MΩ
V_{OUT}	Output voltage @ ± I_{PN}, R_L = 10 kΩ, T_A = 25°C	± 4	V
R_L	Load resistance	> 10	kΩ

For this current transducer, the source current can be sensed as indicated in Figure 4.15 (a) or (b). The transducer location of Figure 14(a) is arbitrarily chosen for implementation.



(a)



(B)

Figure 4.15 Source current sensing

4.4.4 Experimental results

After build up of the circuit was completed, test results were recorded. Although no particular problems have been casually observed for transient conditions, formal study of transient operation is considered outside of the scopes of this thesis. Only steady-state operation has been studied. Some key waveforms from experimental operation are illustrated in this section.

Figure 4.16 illustrates the line voltage and the current loop error signal for full-load condition. Despite high frequency harmonics, the current error signal has the basic shape of the expression of duty-cycle in CCM, as derived in section 2.2.1.

Figure 4.17 displays the line voltage and the line current with an output power of 300 W, and 110 V RMS input voltage. As can be seen, the line current is almost in phase with the line voltage. FFT analysis is made for the line input current. Table 4.2 lists the normalized harmonic contents of the line current. Figure 4.18 illustrates the harmonic contents in the line current at rated voltage with full load.

Figure 4.19 shows the line voltage and the line current at rated load while the input is 90 V RMS. Figure 4.20 shows the line voltage and the line current at rated load while the input is 130 V RMS.

Figure 4.21 depicts the line voltage and the positive DC output voltages at rated load. Figure 4.22 shows the two DC output voltages at rated load. When the output voltages were measured, the ground of the oscilloscope is connected to the ground of positive DC output voltage. So, due to electromagnetic interface into the measurement cable, there is some high frequency harmonics in the negative DC output voltage. The average value of the DC voltages are ± 45 V. FFT analysis is made for the output voltage.

Table 4.3 lists the normalized harmonic contents in the line current. Figure 4.23 illustrates the harmonic contents in the line current at full load.

AC ripple voltage in negative DC output is displayed in Figure 4.24. The peak-to-peak AC ripple voltage is about 2.5V, which is 5.6% of the output DC voltage. If larger output filter capacitors are used, the AC ripple voltage should be decreased further.

Figure 4.25 illustrates the inductor current at rated load. The current ripple in the inductor is about 25% of the peak current at its worst case.

Figure 4.26 shows the line voltage and the line current at half rated load. FFT analysis is made for the line input current. Table 4.4 lists the normalized harmonic contents of the line current. Figure 4.27 depicts the harmonic contents of the line current. Figure 4.28 illustrates the line voltage and positive DC output voltage at half rated load. Figure 4.29 depicts the positive and negative DC voltage outputs at half rated load. Figure 4.30 shows the line voltage and AC voltage ripple in negative output. FFT analysis is made for the output voltage. Table 4.5 lists the normalized harmonic contents in the output voltage. Figure 4.31 illustrates the harmonic contents in the output voltage, With lower out power, AC ripple voltage in the output decreases accordingly.

Table 4.6 lists the measured efficiency and power factor at different line voltages with rated load. Figure 4.32 depicts the efficiency at different line voltage. Figure 4.33 shows the source power factor at different line voltage. Lossless snubber circuit and/or other auxiliary circuits could be utilized in the circuit to improve the circuit efficiency.

At light load, the current through the filter capacitor is the main component of the line current. If the Delay Network is not adjusted to exactly eliminate the effect of the filter capacitor current, the line current will display more

distortion. Figure 4.34 shows the line voltage and the line current when the output power is 32 Watts.

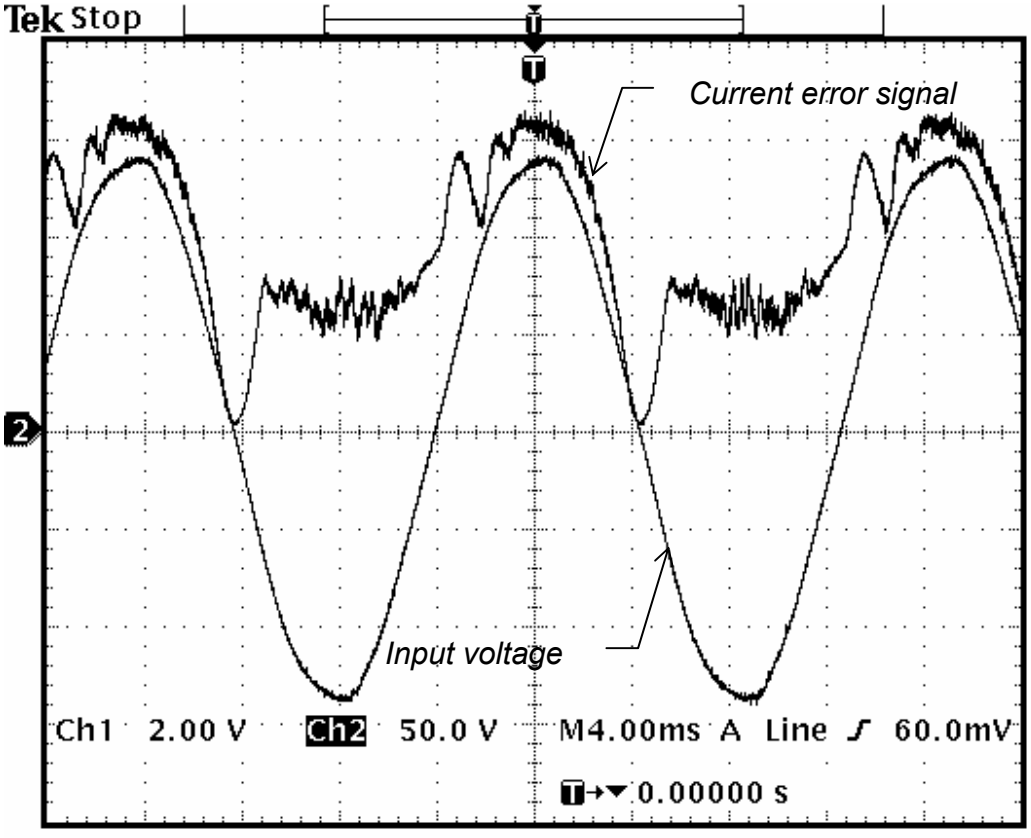


Figure 4.16 Input voltage and outer loop current error signal

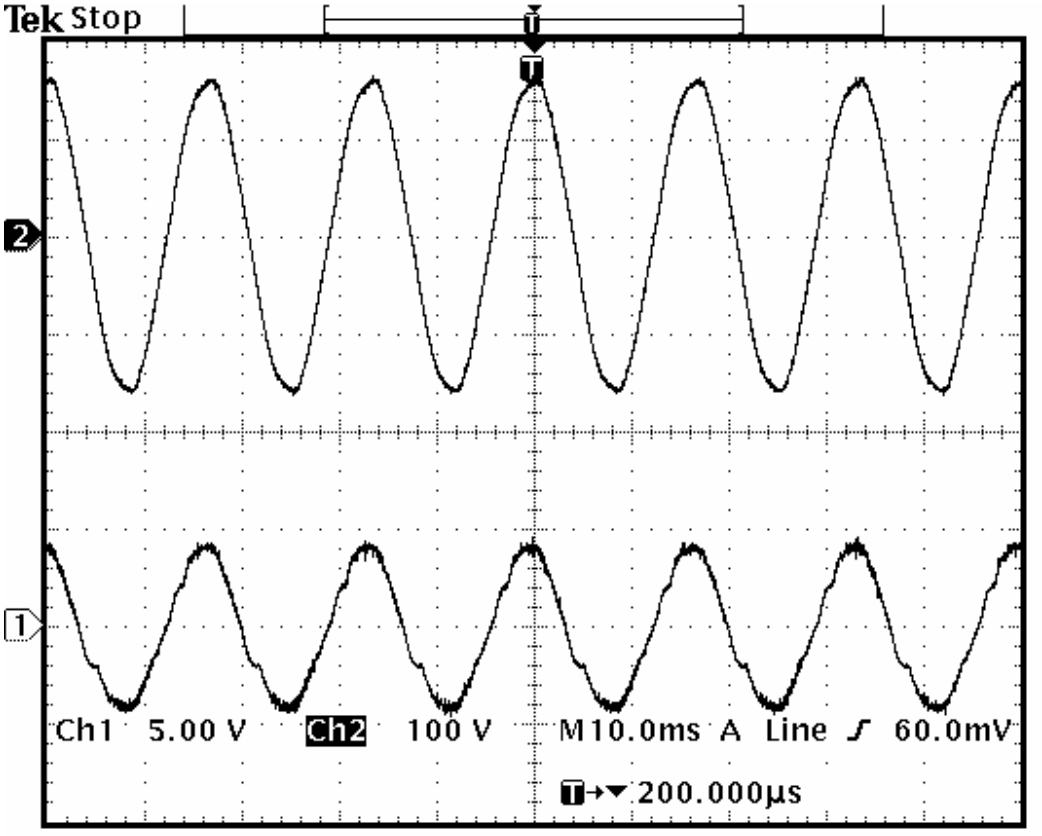


Figure 4.17 Line voltage and line current when line voltage is 110 VRMS with 300 Watts output power

Upper trace : Line voltage (100 V/Division)

Lower trace : Line current (4 A/Division)

Table 4.2 Normalized harmonic contents in the line current at rated load

Frequency (Hz)	**Normalized magnitude**
0	0.035
60	1
120	0.115
180	0.053
240	0.034
300	0.01
360	0.037
420	0.024
480	0.019
THD	0.1443

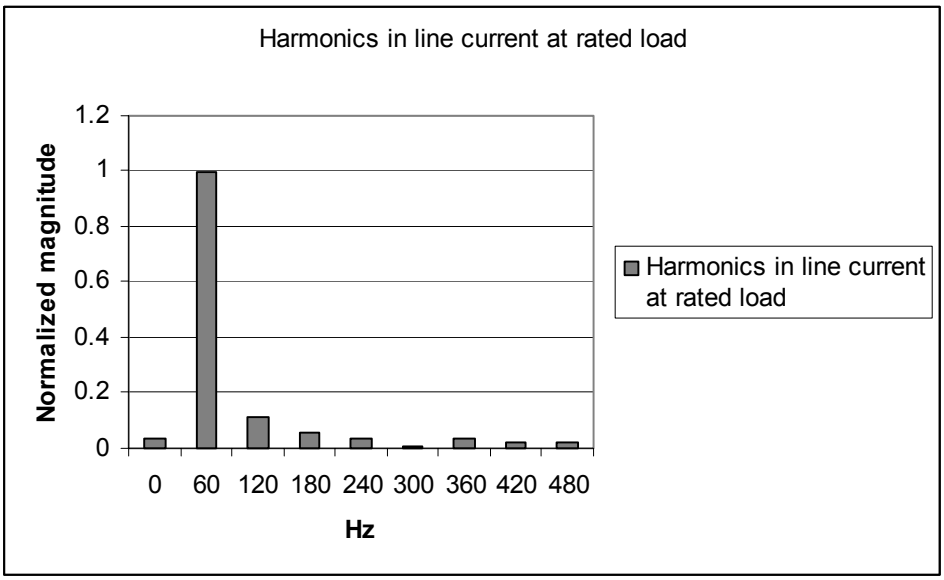


Figure 4.18 Line current harmonics at rated load

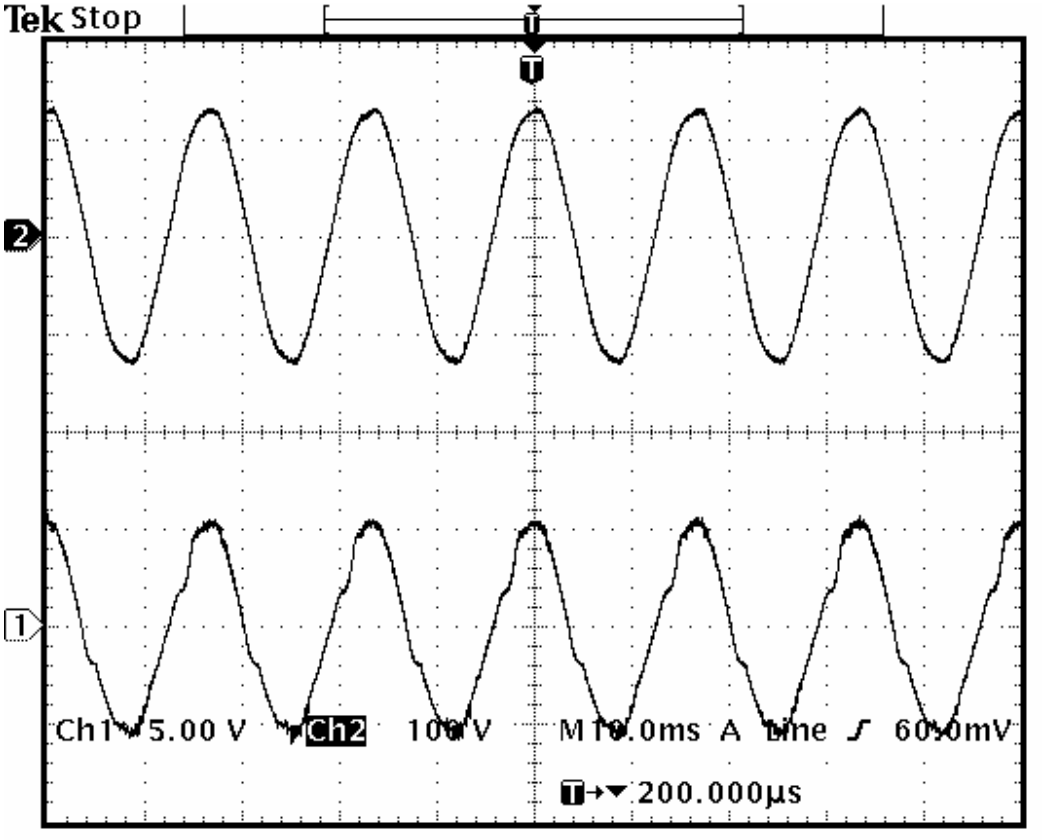


Figure 4.19 Line voltage and line current when line voltage is 90 VRMS with 300 Watts output power

Upper trace : Line voltage (100 V/Division)

Lower trace : Line current (4 A/Division)

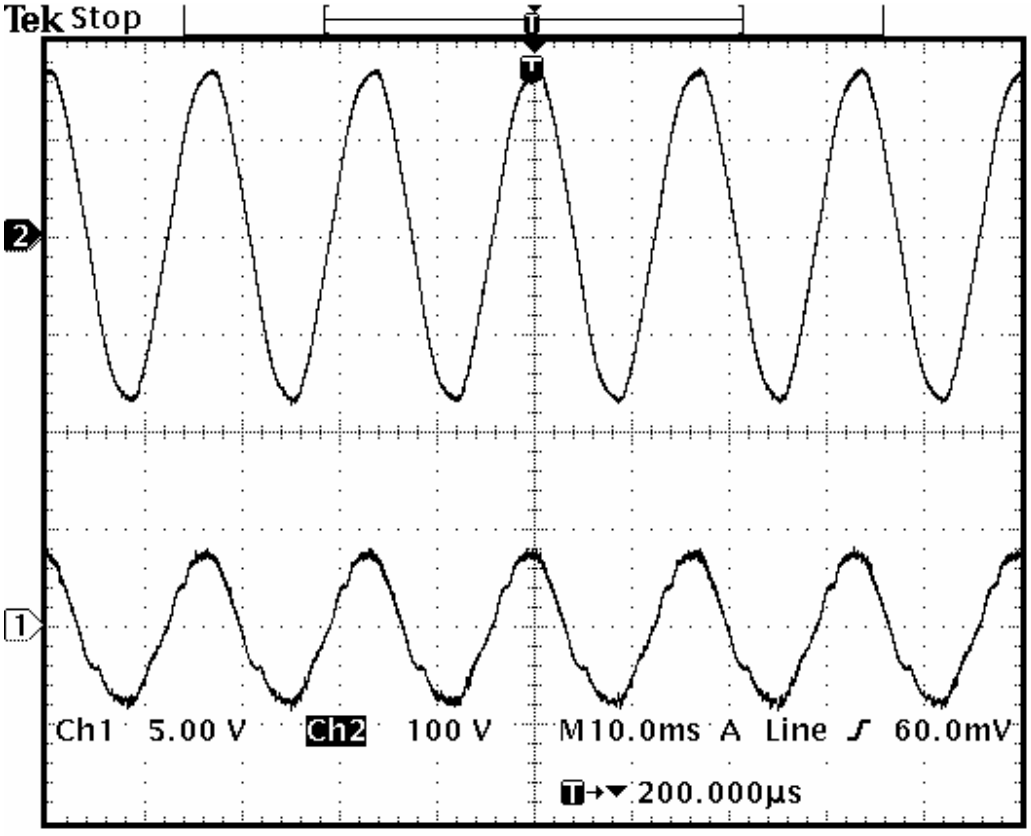


Figure 4.20 Line voltage and line current when line voltage is 130 VRMS with 300 Watts output power

Upper trace : Line voltage (100 V/Division)

Lower trace : Line current (4 A/Division)

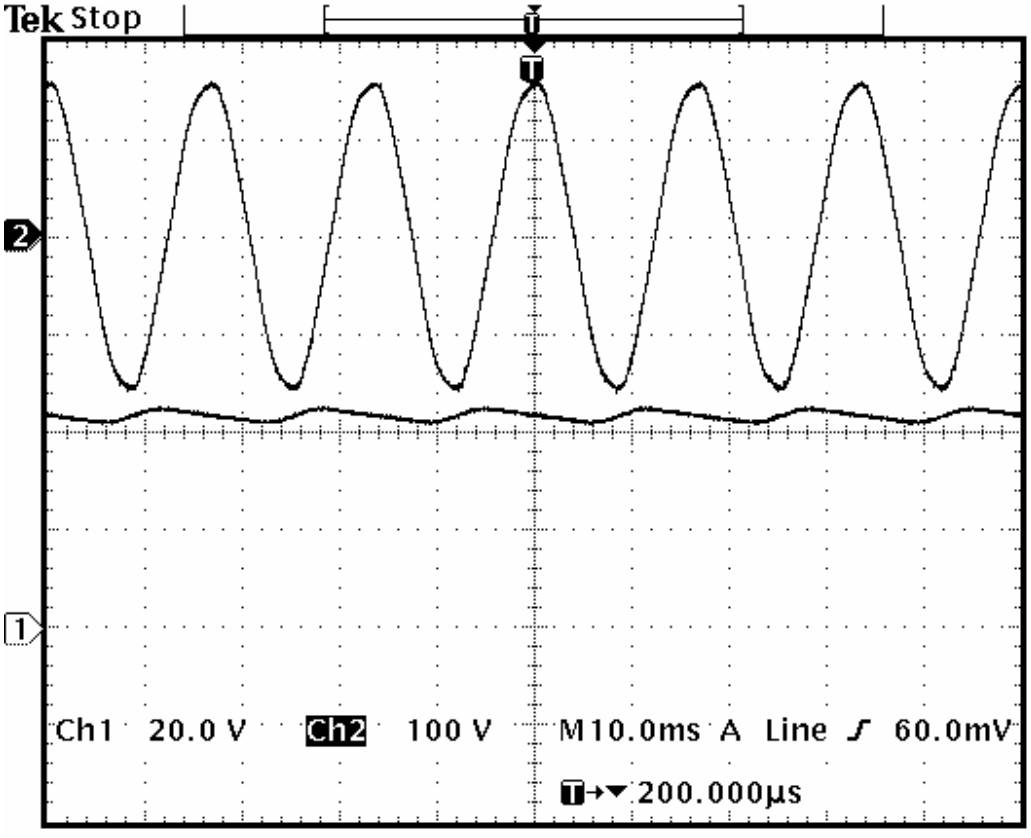


Figure 4.21 Positive DC Output voltage at rated load power

Upper trace : Line voltage (100 V/Division)

Lower trace : Positive DC output voltage (20 V/Division)

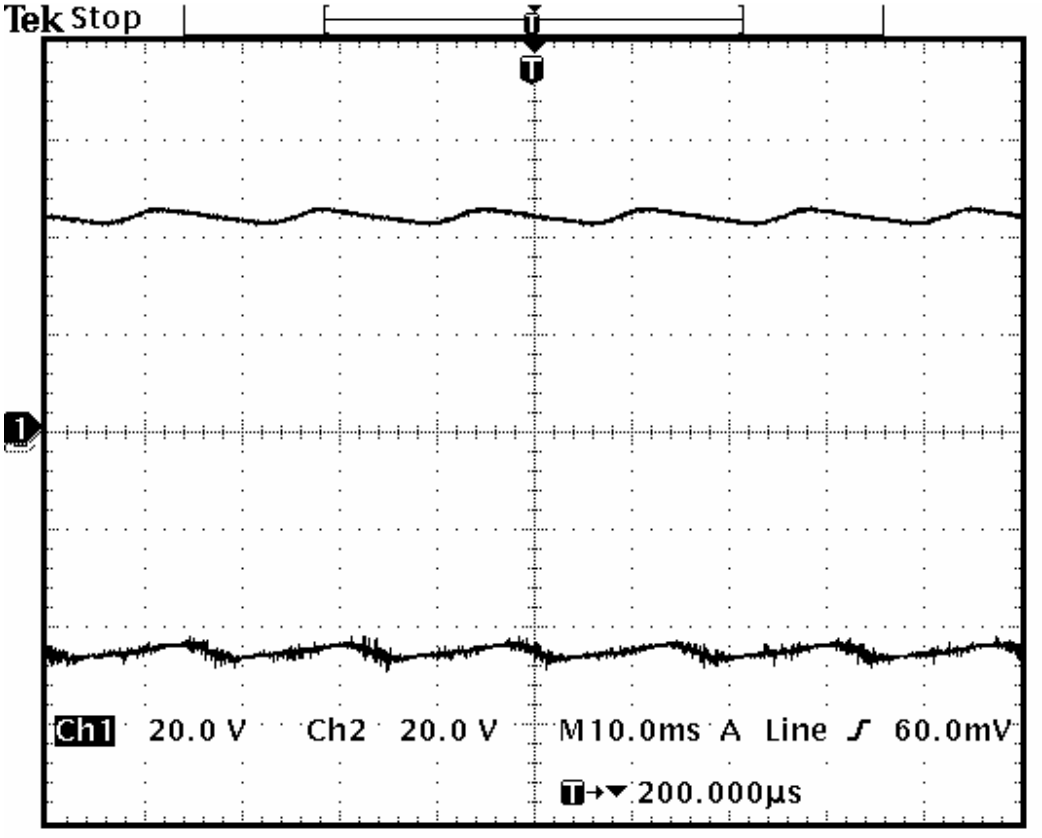


Figure 4.22 Output DC voltages at rated load

Upper trace : Positive output voltage (20 V/Division)

Lower trace : Negative output voltage (20 V/Division)

Table 4.3 Normalized harmonic contents in the output voltage at rated load

Frequency (Hz)	**Normalized magnitude**
0	1
60	0.014
120	0.054
180	0.018

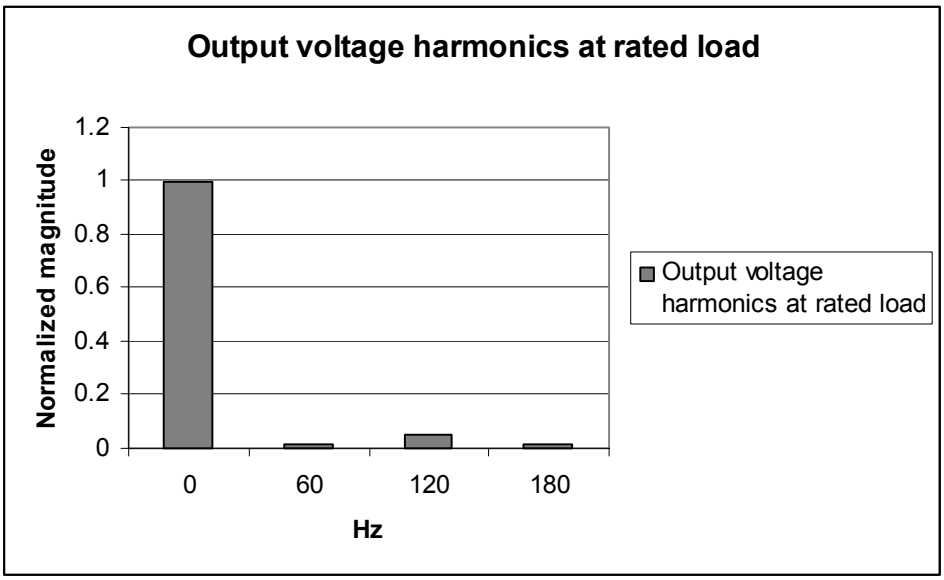


Figure 4.23 Normalized output voltage harmonics

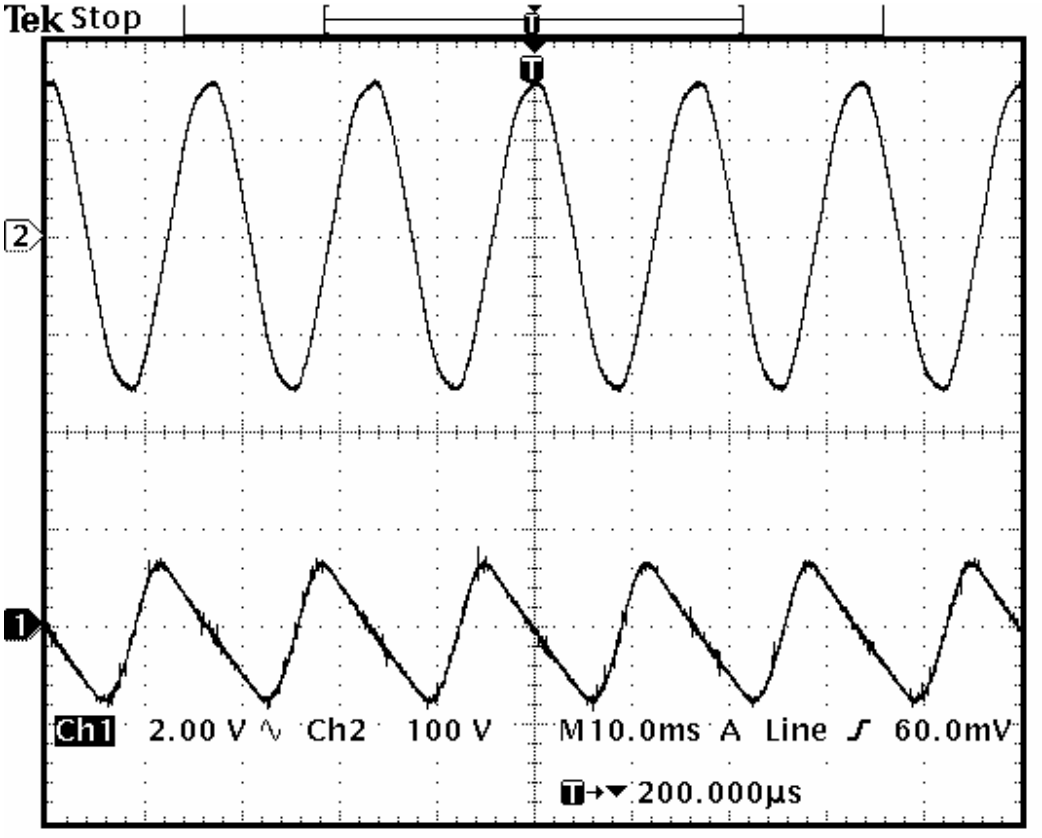


Figure 4.24 AC ripple voltage in negative output voltage at rated load

Upper trace : Source voltage (100 V/Division)

Lower trace : Output voltage ripple (2 V/Division)

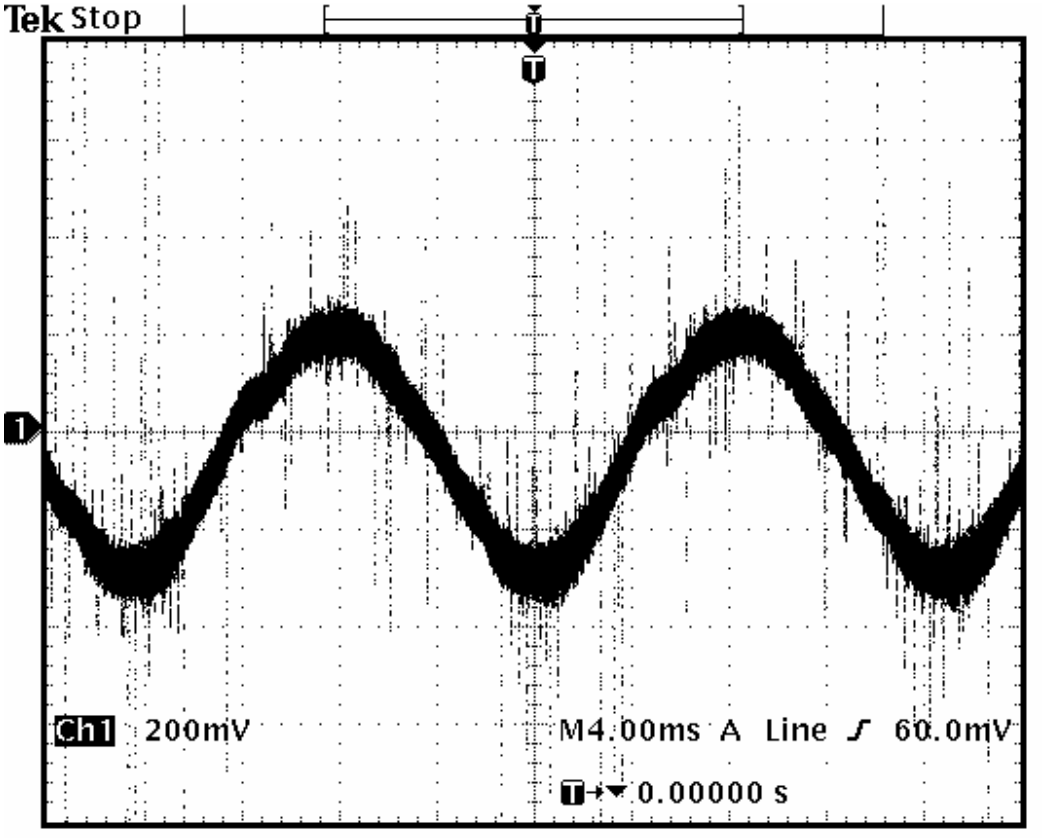


Figure 4.25 AC ripple current for in negative output at rated load
(4 A/Division)

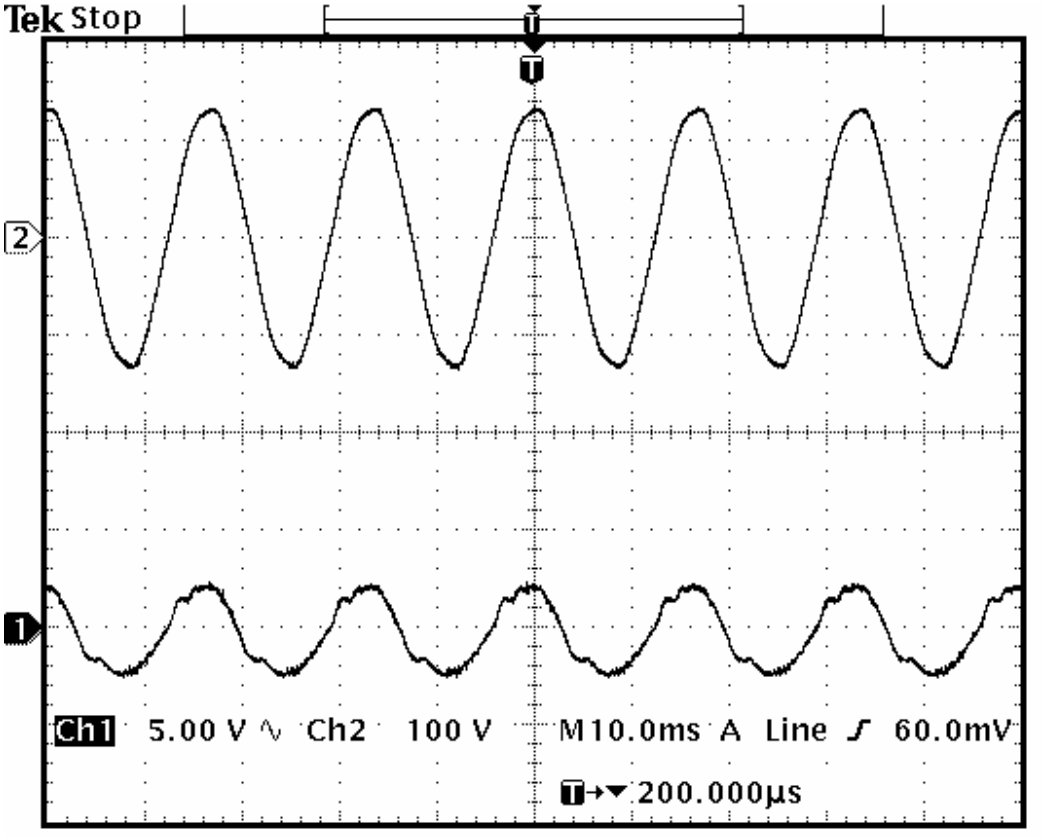


Figure 4.26 Line voltage and line current at rated line voltage and half rated load

Upper trace : Line voltage (100 V/Division)

Lower trace : Line current (4 A/Division)

Table 4.4 Normalized harmonic contents in the line current at half load

Frequency (Hz)	**Normalized magnitude**
0	0.008
60	1
120	0.213
180	0.078
240	0.077
300	0.051
360	0.048
420	0.022
THD	0.251

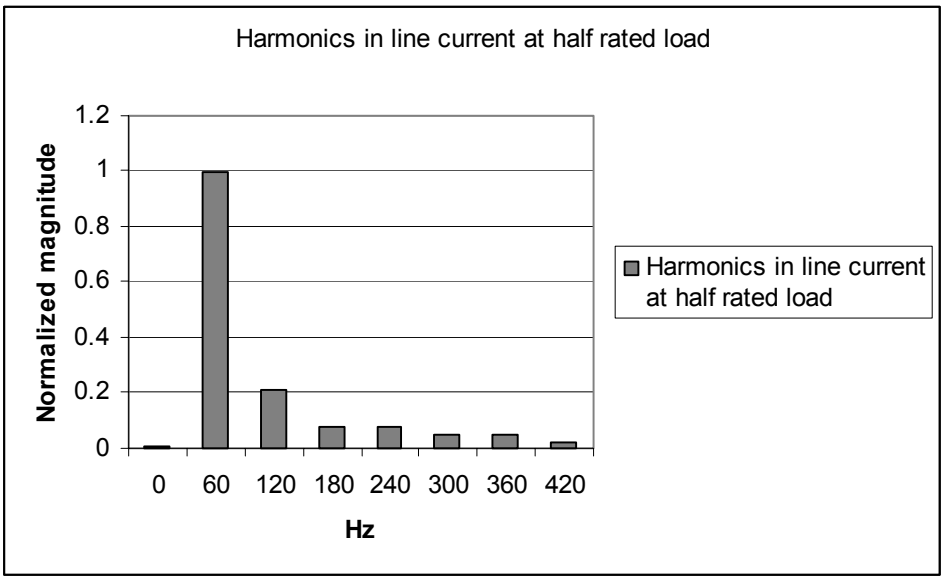


Figure 4.27 Line current harmonics at half load

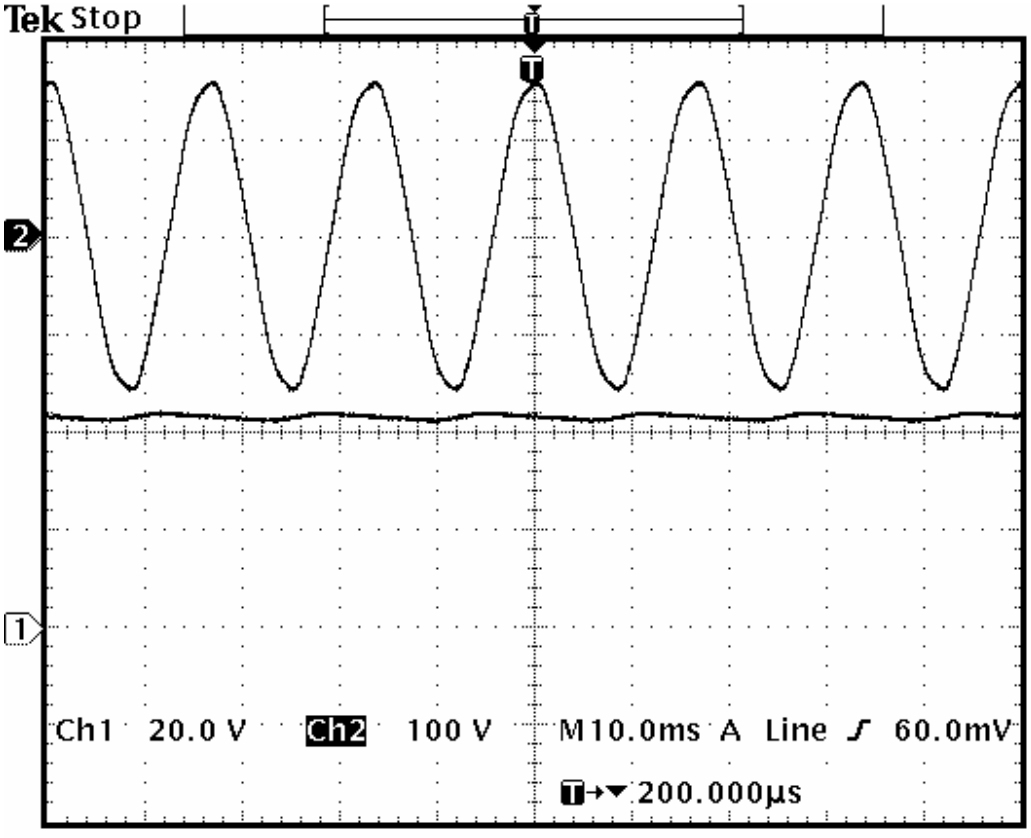


Figure 4.28 Positive DC output at rated line voltage and half rated load

Upper trace : Line voltage (100 V/Division)

Lower trace : Positive DC output voltage (20 V/Division)

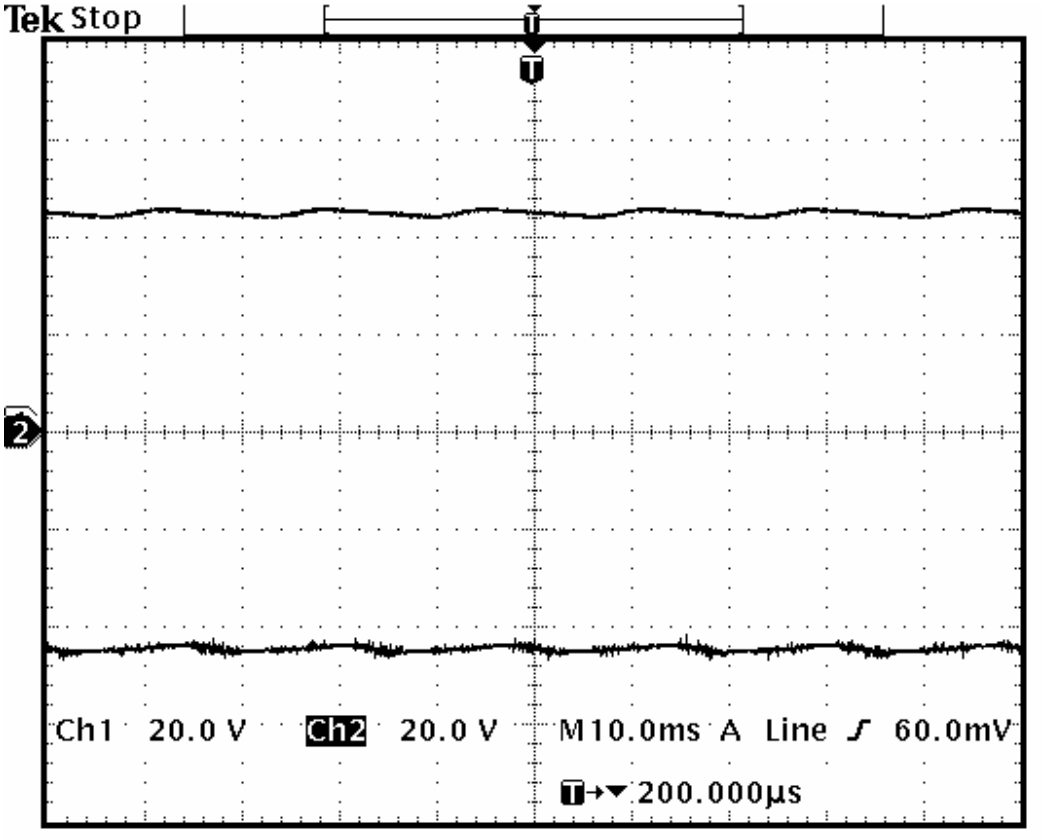


Figure 4.29 DC output voltages at rated line voltage and half rated load

Upper trace: Positive DC output voltage (20 V/Division)

Lower trace : Negative DC output voltage (20 V/Division)

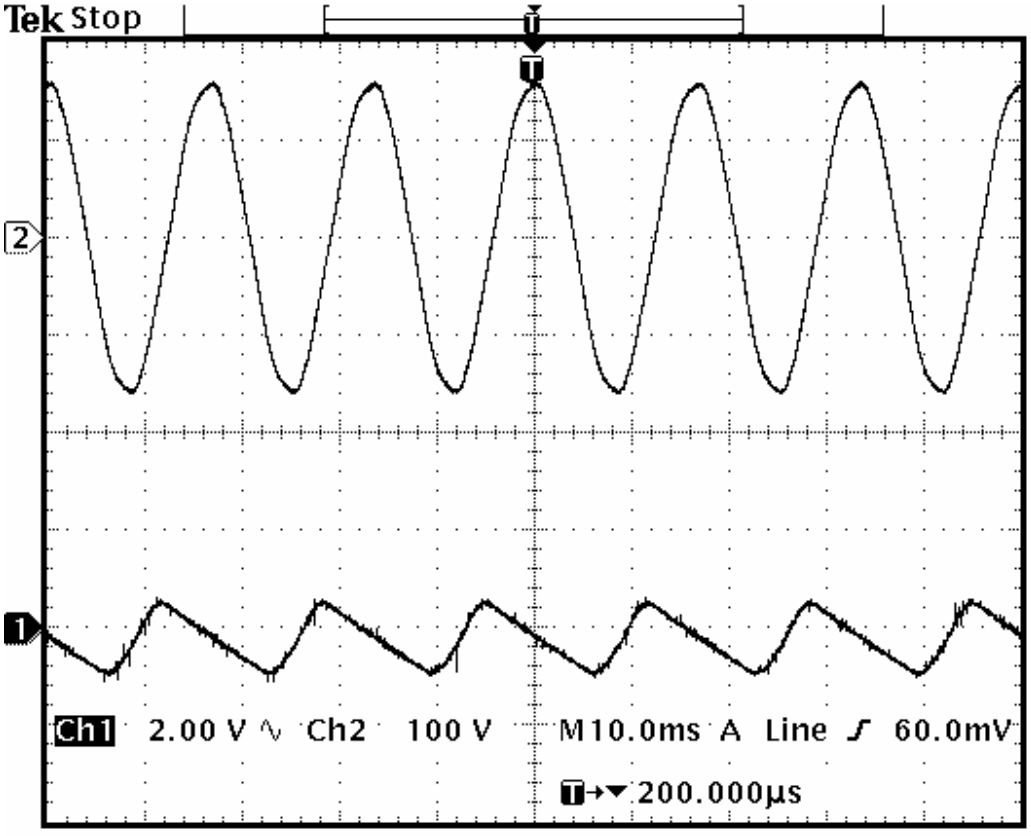


Figure 4.30 AC ripple voltage in negative output voltage at half rated load

Upper trace : Source voltage (100 V/Division)

Lower trace : Output voltage ripple (2 V/Division)

Table 4.5 Normalized harmonic contents in the output voltage at half load

Frequency (Hz)	**Normalized magnitude**
0	1
60	0.005
120	0.024
180	0.009

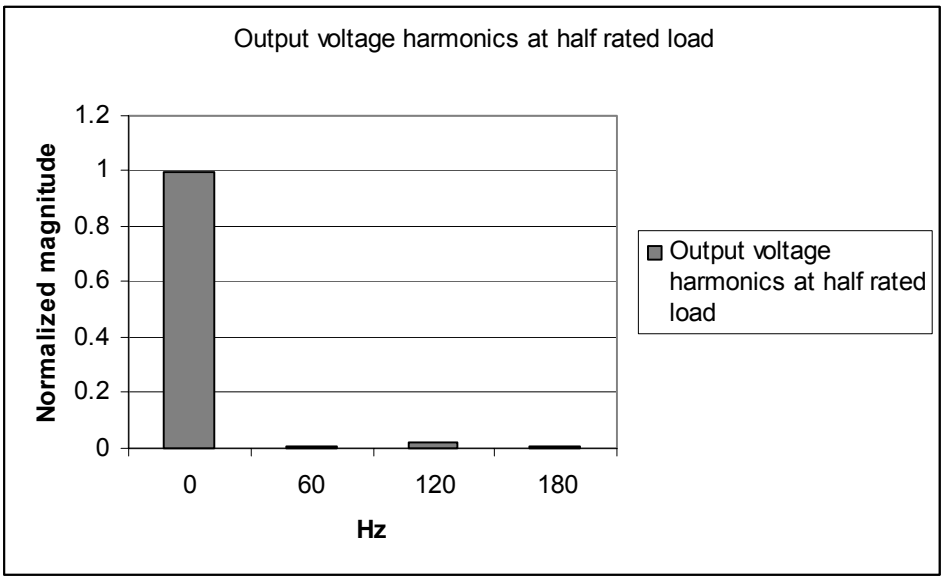


Figure 4.31 Output voltage harmonics at half load

Table 4.6 Efficiency and power factor at different line voltage with rated load

Line voltage (V)	**Line current (A)**	**Input power**	**Efficiency (%)**	**Power factor**
93.5	4.8	448.8	66.8	0.989
100.8	4.35	438.5	68.4	0.988
112.9	3.7	417.73	71.8	0.985
130.9	3.15	412.34	72.76	0.975

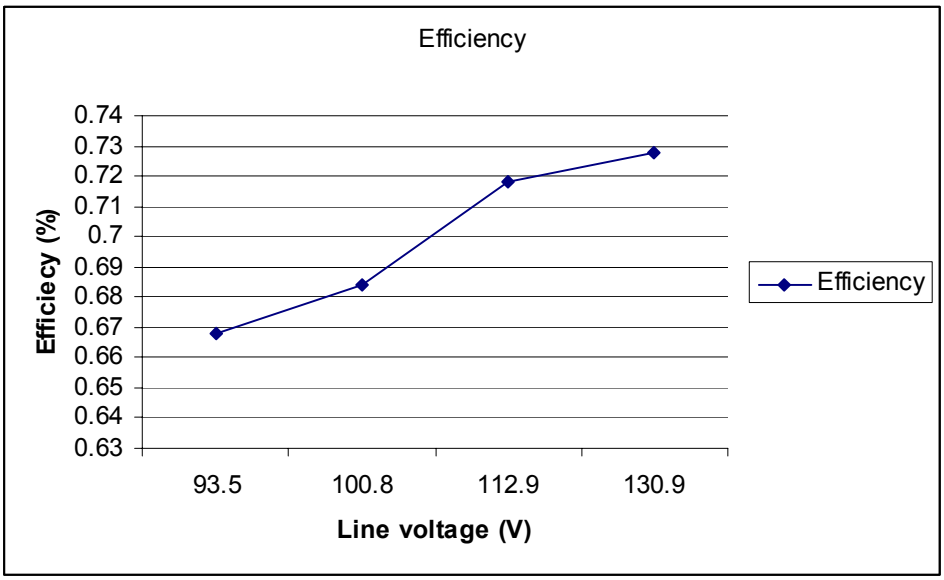


Figure 4.32 Efficiency at rated load

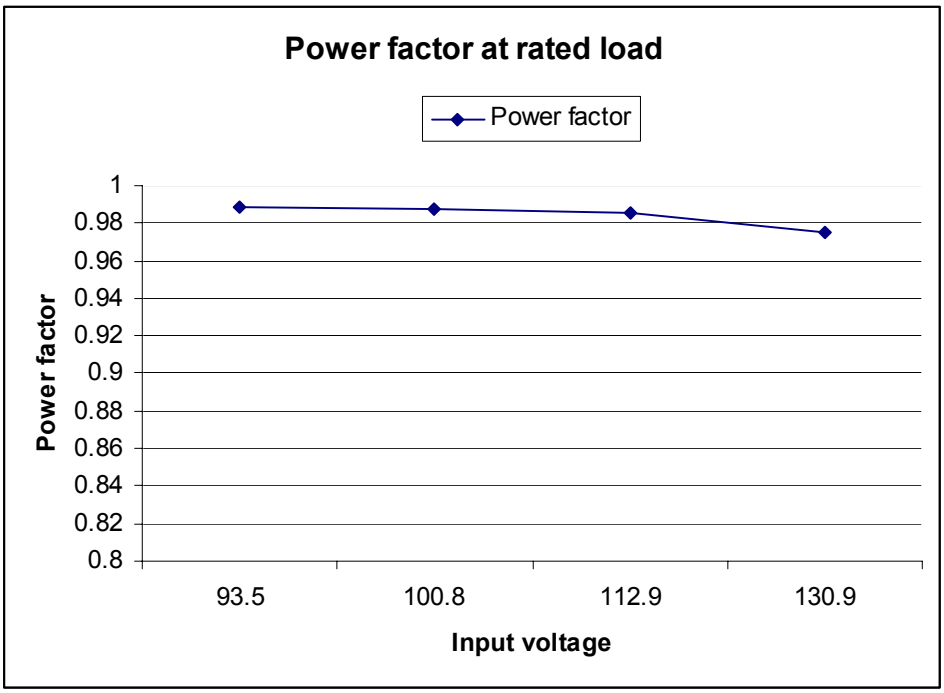


Figure 4.33 Power factor at rated load

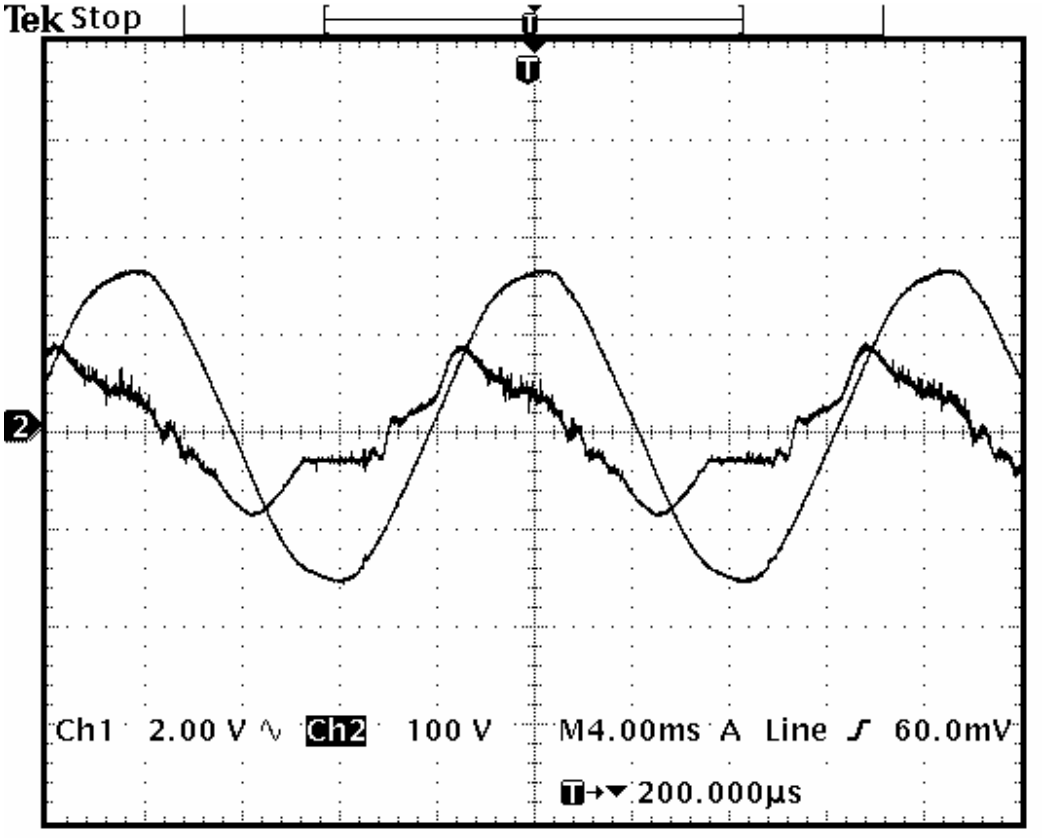


Figure 4.34 Line current waveform at light load

Reference

1. Mitsubishi hybrid IC M57962L technical data sheet.
2. Burr-Brown wide bandwidth precision analog multiplier MPY634 technical data sheet.
3. “Op Amp and Comparators – Don’t confuse them”, Texas Instrument application report SLOA067 – September 2001, http://focus.ti.com/lit/an/sloa067/sloa067.pdf
4. Op07C, Op07D precision operational amplifier technical report.
5. Current transducer LA 03 .. 20-PB, LEM data sheet.

5. Conclusions and future work

5.1 Conclusions

A single-phase, buck-boost based, dual-output converter with ground point shared by both the source and load is analyzed, designed, and implemented in this thesis. Prior study of this converter topology has not been found in the literature. The need for such a topology is driven by plans to design a power electronic transformer that must have a common ground point shared by both the source and load. However, other potential applications of this novel converter topology exist in variable-speed, single-phase motor drives and in multilevel inverters that are currently of interest in high-power level motor drivers and in static VAR compensator circuits. Design equations for the output filter capacitor, and RMS switch, diode and inductor current are derived. The input filter is studied and design guidance is given. The line current to duty cycle ratio transfer function is derived and used to develop a suitable average current control network.

The dual output converter is simulated by use of SPICE. The simulation result shows that the novel Delay Network can significantly improve the line current quality. Further, test results corroborate this finding.

Design of a 300 W, 45 V DC output voltage, buck-boost based, high power factor, dual output converter has been presented in this thesis. A lab model is built up to verify the analysis and design. The experimental results are

satisfactory in that a high power factor, low harmonic content line current results for steady-state operation.

5.2 Future work

Line current distortion at light load has been found as shown in Figure 4.33. A load sensitive adaptive Delay Network is proposed as an addition to the circuit to improve the line current waveform at light load.

In power stage analysis, a quasi-static approximation is employed. The validity of the approximation depends on the assumption that the rectifier system dynamics are sufficiently fast. This approximation needs further justification.

As listed in table 4.6, efficiency of the circuit is lower than desired. A lossless snubber, or other auxiliary devices, could be utilized to improve the efficiency of the dual output converter. However, the future product is to utilize the CVD diamond triode as the switching devices. Thus, it is not judged to be a judicious use of time to work toward reduction of the switching losses for a switch that will not be used in the future product. In anticipation of less switching losses at higher switching frequency with the CVD diamond triode, the efficiency improvement is anticipated. Further, the input filter size can be reduced. Because of a totally different physical mechanism from the solid-state device, the CVD diamond triode is projected to have superior features, such as fast switching frequency (more than 100kHz), high blocking voltage (about 25 kV) and low forward drop (about 1V). The capacity of handling high operation temperature is another feature of the CVD diamond material. The application problems of the new device would be part of the future work.

Appendix A State space average modeling

The positive half of the buck-boost converter with input filter is shown in Figure A.1.

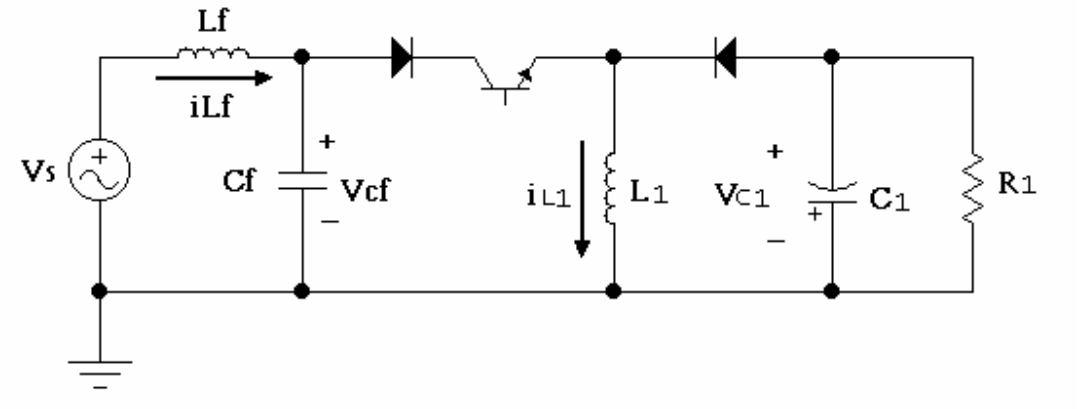


Figure A.1 Positive half of buck-boost based, unity power factor, half bridge, dual output converter with input filter

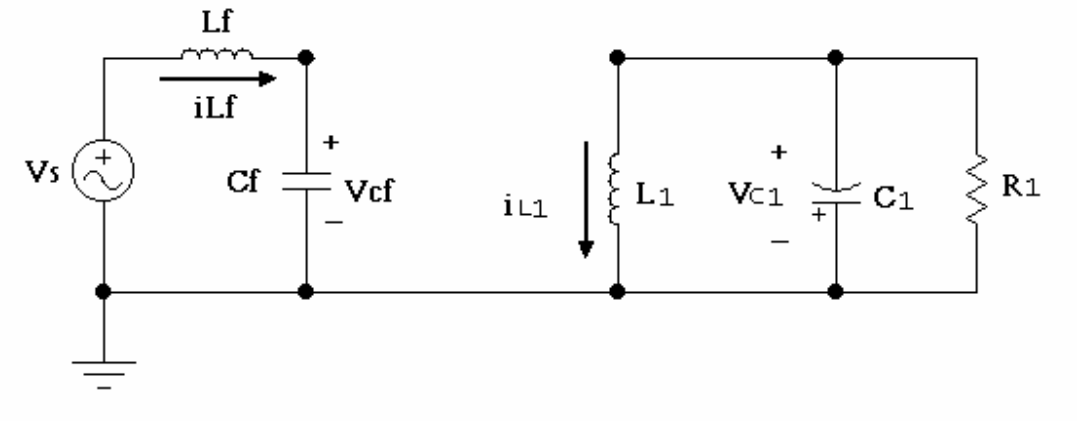


Figure A.2 Circuit while the switch is on

When the switch is on, the circuit is shown in Figure A.2. We have the following state equations:

$$\frac{di_{Lf}}{dt} = -\frac{v_{Cf}}{L_f} + \frac{v_s}{L_f} \tag{A.1}$$

$$\frac{dv_{Cf}}{dt} = \frac{i_{Lf}}{C_f} - \frac{i_{L1}}{C_f} \tag{A.2}$$

$$\frac{di_{L1}}{dt} = \frac{v_{cf}}{L_1} \tag{A.3}$$

$$\frac{dv_{C1}}{dt} = -\frac{v_{c1}}{C_1 R_1} \tag{A.4}$$

$$i_s = i_{Lf} \tag{A.5}$$

Write these equations in state-space form to yield

$$\frac{d}{dt}\begin{bmatrix} i_{Lf} \\ v_{Cf} \\ i_{L1} \\ v_{C1} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{L_f} & 0 & 0 \\ \frac{1}{C_f} & 0 & -\frac{1}{C_f} & 0 \\ 0 & \frac{1}{L_1} & 0 & 0 \\ 0 & 0 & 0 & -\frac{1}{C_1 R_1} \end{bmatrix} \begin{bmatrix} i_{Lf} \\ v_{Cf} \\ i_{L1} \\ v_{C1} \end{bmatrix} + \begin{bmatrix} \frac{1}{L_f} \\ 0 \\ 0 \\ 0 \end{bmatrix} v_s \tag{A.6}$$

$$i_s = \begin{bmatrix} 1 & 0 & 0 & 0 \end{bmatrix} i_{Lf} + \begin{bmatrix} 0 \end{bmatrix} v_s \tag{A.7}$$

We denote,

$$[X] = \begin{bmatrix} i_{Lf} \\ v_{Cf} \\ i_{L1} \\ v_{C1} \end{bmatrix},$$

$$[A_1] = \begin{bmatrix} 0 & -\frac{1}{L_f} & 0 & 0 \\ \frac{1}{C_f} & 0 & -\frac{1}{C_f} & 0 \\ 0 & \frac{1}{L_1} & 0 & 0 \\ 0 & 0 & 0 & -\frac{1}{C_1 R_1} \end{bmatrix},$$

$$[B_1] = \begin{bmatrix} \frac{1}{L_f} \\ 0 \\ 0 \\ 0 \end{bmatrix},$$

$$[C_1] = \begin{bmatrix} 1 & 0 & 0 & 0 \end{bmatrix},$$

$[H_1] = [0]$,

When the switch is off, the circuit is shown in Figure A.3. We have the state equations

$$\frac{di_{Lf}}{dt} = -\frac{v_{Cf}}{L_f} + \frac{v_s}{L_f} \quad \text{(A.8)}$$

$$\frac{dv_{Cf}}{dt} = \frac{i_{Lf}}{C_f} \quad \text{(A.9)}$$

$$\frac{di_{L1}}{dt} = \frac{v_{C1}}{L_1} \quad \text{(A.10)}$$

$$\frac{dv_{C1}}{dt} = -\frac{i_{L1}}{C_1} - \frac{v_{c1}}{C_1 R_1} \quad \text{(A.11)}$$

$$i_s = i_{Lf} \quad \text{(A.12)}$$

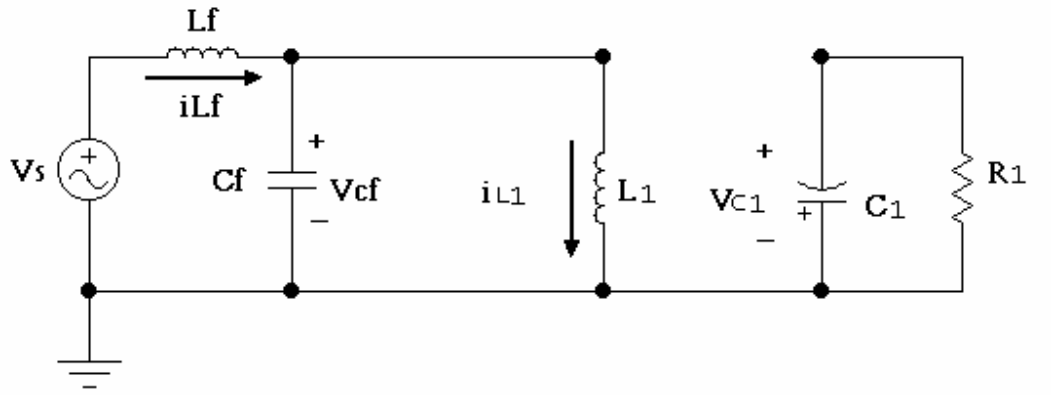


Figure A.3 Circuit while the switch is off

Write the above equations in state space form to give

$$\frac{d}{dt}\begin{bmatrix} i_{Lf} \\ v_{Cf} \\ i_{L1} \\ v_{C1} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{L_f} & 0 & 0 \\ \frac{1}{C_f} & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{L_1} \\ 0 & 0 & -\frac{1}{C_1} & -\frac{1}{C_1 R_1} \end{bmatrix} \begin{bmatrix} i_{Lf} \\ v_{Cf} \\ i_{L1} \\ v_{C1} \end{bmatrix} + \begin{bmatrix} \frac{1}{L_f} \\ 0 \\ 0 \\ 0 \end{bmatrix} v_s \quad \text{(A.13)}$$

$$i_s = \begin{bmatrix} 1 & 0 & 0 & 0 \end{bmatrix} i_{Lf} + [0]\, v_s \quad \text{(A.14)}$$

We denote

$$[A_2] = \begin{bmatrix} 0 & -\frac{1}{L_f} & 0 & 0 \\ \frac{1}{C_f} & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{L_1} \\ 0 & 0 & -\frac{1}{C_1} & -\frac{1}{C_1 R_1} \end{bmatrix}$$

$$[B_2] = \begin{bmatrix} \frac{1}{L_f} \\ 0 \\ 0 \\ 0 \end{bmatrix},$$

$$[C_2] = [1 \quad 0 \quad 0 \quad 0],$$

$$[H_2] = [0],$$

We assume that during k_{th} switching period, the source voltage can be treated as a constant with value $V(kT_s) = V_m(\omega kT_s)$. The duty cycle for the power switch is $D(kT_s)$. And let $D'(kT_s) = 1 - D(kT_s)$. Apply state-space average [1] to the above equations to find the average coefficient matrices for the k_{th} switching period by the following procedure:

$[\overline{A}] = D[A_1] + D'[A_2]$,

$[\overline{B}] = D[B_1] + D'[B_2]$,

$[\overline{C}] = D[C_1] + D'[C_2]$,

$[\overline{H}] = D[H_1] + D'[H_2]$,

The resulting coefficient matrices are

$$\left[\overline{A}(kT_s)\right] = \begin{bmatrix} 0 & -\frac{1}{L_f} & 0 & 0 \\ \frac{1}{C_f} & 0 & -\frac{D(kT_s)}{C_f} & 0 \\ 0 & \frac{D(kT_s)}{L_1} & 0 & \frac{D'(kT_s)}{L_1} \\ 0 & 0 & -\frac{D'(kT_s)}{C_1} & -\frac{1}{C_1R_1} \end{bmatrix},$$

$$\left[\overline{B}(kT_s)\right] = \begin{bmatrix} \frac{1}{L_f} \\ 0 \\ 0 \\ 0 \end{bmatrix},$$

$$\left[\overline{C}(kT_s)\right] = \begin{bmatrix} 1 & 0 & 0 & 0 \end{bmatrix},$$

$$\left[\overline{H}(kT_s)\right] = \begin{bmatrix} 0 \end{bmatrix},$$

Hence, the average value state equations can be written as

$$\left[\dot{\overline{X}}\right] = \left[\overline{A}\right]\left[\overline{X}\right] + \left[\overline{B}\right] v_s \qquad \text{(A.14)}$$

$$\bar{i}_s = \left[\overline{C}\right]\left[\overline{X}\right] + \left[\overline{H}\right] v_s \qquad \text{(A.15)}$$

where $\left[\overline{X}\right]$ and $\bar{i}_s$ are the sum of a steady-state value and a small perturbation component given by

$$\left[\overline{X}\right] = \begin{bmatrix} I_{Lf} + \hat{i}_{Lf} \\ V_{Cf} + \hat{v}_{Cf} \\ I_{L1} + \hat{i}_{L1} \\ V_{C1} + \hat{v}_{C1} \end{bmatrix}$$

$$\bar{i}_s = I_s + \hat{i}_s$$

After replacing D with D + $\hat{d}$ in (A.14), neglecting product of perturbation variables, and substituting (A.18) and (A.19), respectively, from (A.14) and (A.15), the state-space equations with small perturbation can be written as

$$\dot{\hat{x}} = \left[\overline{A}\right]\left[\overline{X}\right] + \left[\overline{B}\right] v_s + [\,(\left[\overline{A}_1\right] - \left[\overline{A}_2\right])\left[\overline{X}\right] + (\left[\overline{B}_1\right] - \left[\overline{B}_2\right]) v_s\,]\,\hat{d} + \left[\overline{A}\right]\hat{x} + \left[\overline{B}\right]\hat{v}_s \qquad \text{(A.16)}$$

$$I_s + \hat{i}_s = [\overline{C}][\overline{X}] + [\overline{H}]v_s + [([\overline{C}_1] - [\overline{C}_2])[\overline{X}] + ([\overline{H}_1] - [\overline{H}_2])v_s]\hat{d} + [\overline{C}]\hat{x} + [\overline{H}]\hat{v}_s \quad \text{(A.17)}$$

In the above two equations, the argument (kT_s) is omitted to reduce the cumbersome appearance of the equations.

Set $\hat{x} = \hat{v}_s = \hat{d} = 0$ in A.16 and A.17 to yield the steady-state equation during k_{th} switching period,

$$\begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{L_f} & 0 & 0 \\ \frac{1}{C_f} & 0 & -\frac{D(kT_s)}{C_f} & 0 \\ 0 & \frac{D(kT_s)}{L_1} & 0 & \frac{D'(kT_s)}{L_1} \\ 0 & 0 & -\frac{D'(kT_s)}{C_1} & -\frac{1}{C_1R_1} \end{bmatrix} \begin{bmatrix} I_{Lf}(kT_s) \\ V_{Cf}(kT_s) \\ I_{L1}(kT_s) \\ V_{C1}(kT_s) \end{bmatrix} + \begin{bmatrix} \frac{1}{L_f} \\ 0 \\ 0 \\ 0 \end{bmatrix} V_s(kT_s) \quad \text{(A.18)}$$

$$I_s(kT_s) = \begin{bmatrix} 1 & 0 & 0 & 0 \end{bmatrix} I_{Lf}(kT_s) + [0]V_s(kT_s) \quad \text{(A.19)}$$

Solving (A.18) for the steady-state currents and voltages, we get

$$I_{Lf}(kT_s) = -\frac{D(kT_s)^2}{D'(kT_s)^2}\frac{V_s(kT_s)}{R_1} \quad \text{(A.20)}$$

$$V_{Cf}(kT_s) = V_s(kT_s) \quad \text{(A.21)}$$

$$I_{L1}(kT_s) = -\frac{D(kT_s)V_s(kT_s)}{D'(kT_s)^2 R_1} \quad \text{(A.22)}$$

$$V_{C1}(kT_s) = -\frac{D(kT_s)}{D'(kT_s)}V_s(kT_s) \quad \text{(A.23)}$$

The small-signal ac state equations are determined by subtracting (A.18) and (A.19) from (A.16) and (A.17), respectively

$$\frac{d}{dt}\begin{bmatrix}\hat{i}_{Lf}\\ \hat{v}_{Cf}\\ \hat{i}_{L1}\\ \hat{v}_{C1}\end{bmatrix} = \begin{bmatrix}0 & -\frac{1}{L_f} & 0 & 0\\ \frac{1}{C_f} & 0 & -\frac{D(kT_s)}{C_f} & 0\\ 0 & \frac{D(kT_s)}{L_1} & 0 & \frac{D'(kT_s)}{L_1}\\ 0 & 0 & -\frac{D'(kT_s)}{C_1} & -\frac{1}{C_1R_1}\end{bmatrix}\begin{bmatrix}\hat{i}_{Lf}\\ \hat{v}_{Cf}\\ \hat{i}_{L1}\\ \hat{v}_{C1}\end{bmatrix} + \begin{bmatrix}\frac{1}{L_f}\\ 0\\ 0\\ 0\end{bmatrix}\hat{v}_s + \begin{bmatrix}0\\ -I_{L1}\\ V_{Cf}-V_{C1}\\ I_{L1}\end{bmatrix}\hat{d} \tag{A.24}$$

$$\hat{i}_s = \begin{bmatrix}1 & 0 & 0 & 0\end{bmatrix}\hat{i}_{Lf} + \begin{bmatrix}0\end{bmatrix}\hat{v}_s + \begin{bmatrix}0\end{bmatrix}\hat{d} \tag{A.25}$$

In scalar form, the above state equation are

$$L_f\frac{d\hat{i}_{Lf}}{dt} = -\hat{v}_{Cf} + \hat{v}_s \tag{A.26}$$

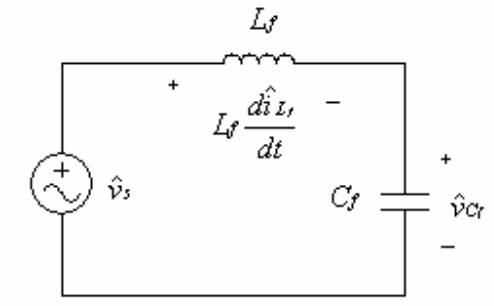
$$C_f\frac{d\hat{v}_{Cf}}{dt} = \hat{i}_{Lf} - D(kT_s)\hat{i}_{Lb} - I_{Lb}(kT_s)\,\hat{d} \tag{A.27}$$

$$L_1\frac{d\hat{i}_{L1}}{dt} = D(kT_s)\hat{v}_{cf} + D'(kT_s)\hat{v}_{c1} + \left(Vs(kT_s) - V_{C1}(kT_s)\right)\hat{d} \tag{A.28}$$

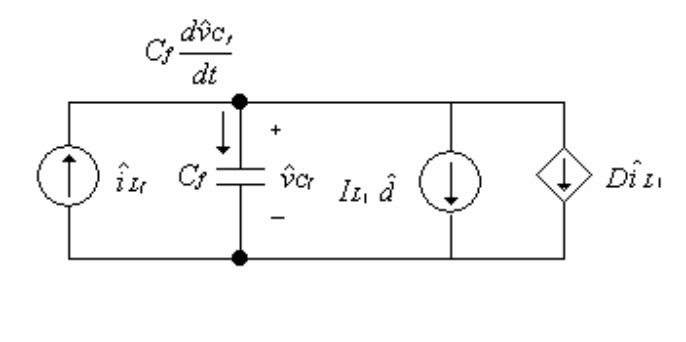
$$C_1\frac{d\hat{v}_{C1}}{dt} = -D'(kT_s)\hat{i}_{L1} - \frac{\hat{v}_{c1}}{R_1} + I_{L1}(kT_s)\,\hat{d} \tag{A.29}$$

$$\hat{i}_s = \hat{i}_{Lf} \tag{A.30}$$

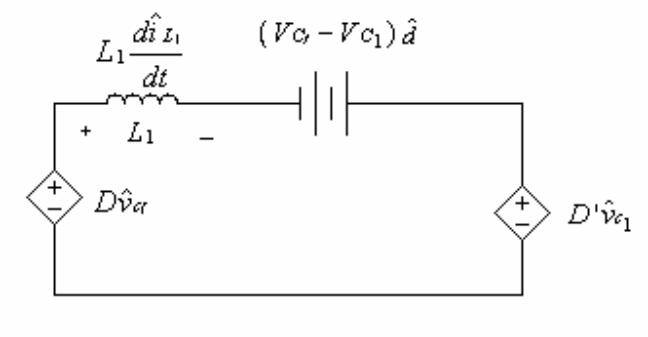
Circuits that satisfy (A.26) – (A.30) are shown in Figure A.4. These circuits can be combined into the complete small-signal ac equivalent circuit model of Figure A.5.



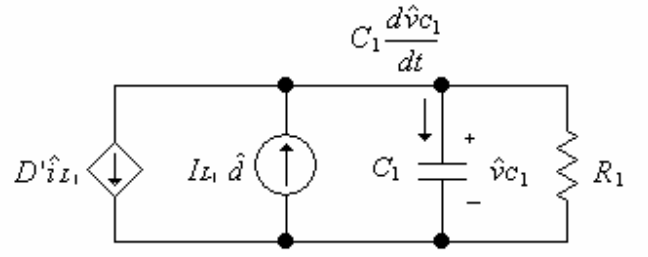
(a) Filter inductor loop



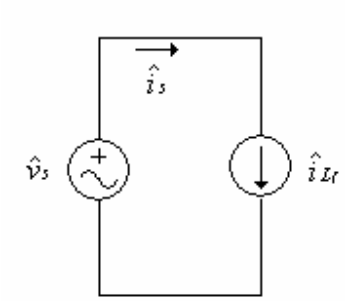
(b) Filter capacitor node



(c) Buck-boost inductor loop



(d) Buck-boost capacitor node



(e) Buck-boost capacitor node

Figure A.4 Circuit equivalent to the small-signal converter equations

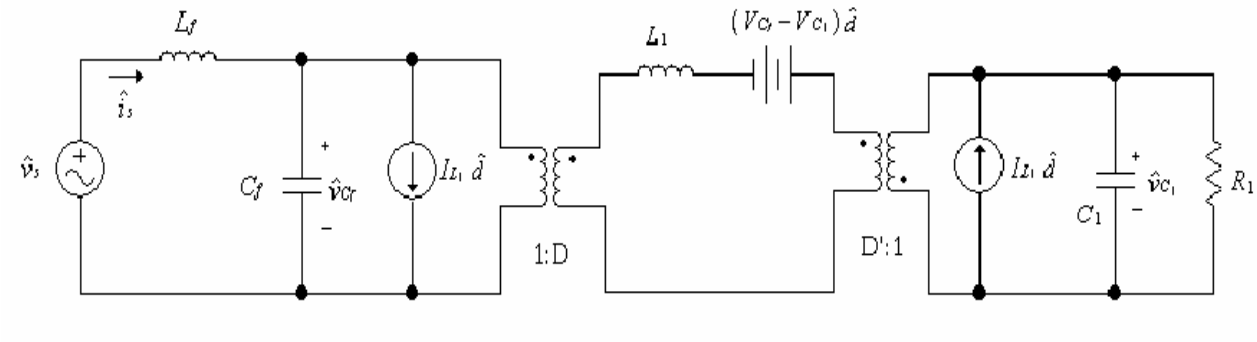


Figure A.5 Complete small-signal ac equivalent circuit model

Proceeding to determine the control-to-input-current transfer function $H(s)$ = $\hat{i}_{Lf}(s)/d(s)$, we set the independent voltage source $\hat{v}_s$ to zero. Then, we take the zero initial condition Laplace transformations of equation (A.26) – (A.30)

$$sL_f\hat{i}_{Lf}(s) = -\hat{v}_{Cf}(s) \qquad \text{(A.31)}$$

$$sC_f\hat{v}_{Cf}(s) = \hat{i}_{Lf}(s) - D(kT_s)\hat{i}_{Lb}(s) - I_{Lb}(kT_s)\,\hat{d}(s) \qquad \text{(A.32)}$$

$$sL_1\hat{i}_{L1}(s) = D(kT_s)\hat{v}_{Cf}(s) + D'(kT_s)\hat{v}_{C1}(s) + (Vs(kT_s) - V_{C1}(kT_s))\,\hat{d}(s) \qquad \text{(A. 33)}$$

$$sC_1\hat{v}_{C1}(s) = -D'(kT_s)\hat{i}_{L1}(s) - \frac{1}{R_1}\hat{v}_{C1}(s) + I_{L1}(kT_s)\,\hat{d}(s) \qquad \text{(A. 34)}$$

$$\hat{i}_s(s) = \hat{i}_{Lf}(s) \qquad \text{(A. 35)}$$

From (A.31),

$$\hat{v}_{Cf}(s) = -sL_f\hat{i}_{Lf}(s) \qquad \text{(A. 36)}$$

From (A.34),

$$\hat{v}_{C1}(s) = \frac{1}{sC_1 + \frac{1}{R_1}}\left(-D'(kT_s)\hat{i}_{L1}(s) + I_{L1}(kT_s)\,\hat{d}(s)\right) \qquad \text{(A.37)}$$

Substitute (A.37) into (A.33) and solve for $\hat{i}_{L1}(s)$ in terms of $\hat{v}_{Cf}(s)$ and $\hat{i}_{Lf}(s)$. The argument is omitted in the work that follows:

$$\hat{i}_{L1}(s) = \frac{sRC_1+1}{sL_1 + s^2RL_1C_1 + R_1D'^2}\left(D\hat{v}_{cf}(s)\right) + \frac{D'R_1}{1+sRC_1}I_{L1} + \left(Vs - V_{C1}\right)\hat{d}(s)\Big) \qquad \text{(A.38)}$$

Substitute (A.36) into (A.38) and the resulting equation into A.32,

$$\left(1 + s^2L_fC_f + \frac{sL_fD^2(sRC_1+1)}{sL_1 + s^2RL_1C_1 + RD'^2}\right)\hat{i}_{Lf}(s)$$

$$= \left(\frac{DD'R_1I_{L1} + (\mathrm{V_s} - V_{C1})D(sR_1C_1+1)}{sL_1 + s^2R_1C_1L_1 + R_1D'^2} + I_{L1}\right)\hat{d}(s)$$

So,

$$H(s) = \frac{\hat{i}_{Lf}(s)}{\hat{d}(s)} = \frac{\frac{DD'RI_{L1} + (\mathrm{V_s} - V_{C1})D(sR_1C_1+1)}{sL_1 + s^2R_1C_1L_1 + R_1D'^2} + I_{L1}}{1 + s^2L_fC_f + \frac{sL_fD^2(sR_1C_1+1)}{sL_1 + s^2R_1L_1C_1 + R_1D'^2}}$$

$$= \frac{\frac{DD'R_1I_{L1} + (\mathrm{V_s} - V_{C1})D(sR_1C_1+1)}{sL_1 + s^2R_1C_1L_1 + R_1D'^2} + I_{L1}}{1 + s^2L_fC_f + \frac{sD^2L_f(sR_1C_1+1)}{sL_1 + s^2R_1L_1C_1 + R_1D'^2}}$$

$$= \frac{s^2R_1C_1L_1I_{L1} + s[(\mathrm{V_s} - V_{C1})DR_1C_1 + L_1I_{L1}] + DD'R_1I_{L1} + D(V_{Cf} - V_{C1}) + R_1D'^2\,I_{L1}}{s^4R_1L_fC_fL_1C_1 + s^3L_fC_fL_1 + s^2(R_1L_1C_1 + R_1D^2L_fC_1 + R_1L_fC_fD^2) + s(L_1 + D^2L_f) + R_1D'^2} \qquad \text{(A.39)}$$

In application, the output capacitor is a large valued component in the circuit, which is used to remove both the switching frequency harmonic and the harmonic of double the line frequency. We assume the output capacitor approaches infinity, so that, the variation of the output voltage is negligibly small. Thus, in the above transfer function, we divide both the nominator and the denominator by C_1 to yield

$$H(s) = \frac{s^2 R_1 L_1 I_{L1} + s[(V_s - V_{C1})DR_1 + \frac{L_1 I_{L1}}{C_1}\} + \frac{DD' R_1 I_{L1} + D(V_s - V_{C1}) + R_1 D'^2 I_{Lb}}{C_1}}{s^4 R_1 L_f C_f L_1 + s^3 \frac{L_f C_f L_1}{C_1} + s^2 (R_1 L_1 + R_1 D^2 L_f + \frac{R_1 L_f C_f D^2}{L_f C_f L_1}) + s \frac{L_1 + D^2 L_f}{C_1} + \frac{RD'^2}{C_1}}$$

By omitting the infinitely small values, that result when $C_1 \to \infty$, we get

$$H(s) = \frac{sL_1 I_{L1} + D(V_s - V_{C1})}{s^3 L_f C_f L_1 + s[L_1 + D^2 L_f]}$$

$$= \frac{1}{L_f C_f} \frac{sI_{L1} + \frac{D}{L_1}(V_s - V_{C1})}{s(s^2 + \frac{1}{L_f C_f} + \frac{D^2}{L_1 C_f})} \qquad \text{(A.40)}$$

which has the same form as in the literature [2].

If we assume the input filter is small enough to be omitted, then the transfer function can be simplified further by letting the input filter inductance be equal to zero.

$$H(s) = \frac{sL_1 I_{L1} + D(V_s - V_{C1})}{sL_1}$$

$$= I_{L1} + \frac{D(V_s - V_{C1})}{sL_1}$$

Using $V_{C1} = -\frac{DV_s}{D'}$,

we can get $D(V_s - V_{Cb}) = D(V_s + \frac{D}{D'}V_s) = \frac{D(kT_s)V(kT_s)_s}{D'(kT_s)} = V_{C1}$

Then, the transfer function can be expressed as

$$H(s) = I_{Lb} + \frac{V_{Cb}}{sL_b}$$

which has the same form as in the literature [3]. This is the case for buck-boost converter in which line input current is sensed after the filter.

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