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MITIGATION OF REFLECTED OVERVOLTAGE IN WIND-TURBINE GENERATOR-CONVERTER SYSTEMS WITH A SMART COIL CONCEPT

THESIS

A thesis submitted in partial fulfillment of the requirements for the degree of Master of Science in Electrical Engineering in the College of Engineering at the University of Kentucky

By

Lulu Wei

Lexington, Kentucky

Director: Dr. JiangBiao He

Department of Electrical and Computer Engineering

2024

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ABSTRACT OF THESIS

MITIGATION OF REFLECTED OVERVOLTAGE IN WIND-TURBINE GENERATOR-CONVERTER SYSTEMS WITH A SMART COIL CONCEPT

In the recent decade, ultra-fast wide bandgap switching devices such as Silicon Carbide (SiC) Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) have been increasingly utilized in power electronic converters for renewable energy power generation systems due to their advantages of enabling high energy efficiency and high power density. However, the much higher voltage slew rate (i.e., dv/dt) with SiC power converters may induce voltage reflection and reliability concerns in machine-converter systems, especially for medium-voltage systems with long cable connections. In wind-turbine power generation systems, generators are typically located in the nacelles, and medium-voltage power converters are mostly placed at the bottom of the tower for the convenience of maintenance, resulting in long cables (e.g., 200-300 feet) interconnected between generators and power converters. Consequently, the high dv/dt caused by fast-switching SiC devices coupled with the long cables induces high-frequency overvoltage ringing across the generator's stator windings. To mitigate such reflected overvoltage across the generator windings and improve the reliability of the wind turbine system, an innovative mitigation solution will be developed and presented in this thesis.

In this thesis, the voltage reflection mechanism with its main formation factors, including high dv/dt caused by fast-switching SiC devices, long cables interconnected between the generator and power converter, and high-frequency surge impedance mismatch between the cables and the generator are thoroughly investigated. The conventional methods to mitigate the reflected overvoltage will be reviewed, including surge impedance matching, dv/dt mitigation, and integrated machine-drive solutions. Furthermore, high-frequency modeling for generator-converter systems is indispensable to studying the voltage reflection phenomenon versus different cable lengths and semiconductors' rise time. The surge impedance measurements for cables and generators are carried out to accurately model the high-frequency distributed circuit models. The uneven voltage distribution across different coils is investigated, confirming that the first few coils withstand most of the reflected voltages. Targeting mitigating the surge voltage stress across the first few coils, an innovative solution named the smart coil concept is developed, simulated, and tested to verify its efficacy. This proposed

smart coil solution mainly includes a bi-directional Gallium Nitride (GaN) transistor, capacitors, diodes, and the related control logic. Therefore, it can be conveniently integrated into the generator junction box due to its ultra-compact footprint. Based on a lab-scale generator-cable-converter system, the proposed mitigation solution is thoroughly verified in the simulation studies.

KEYWORDS: wind-turbine generator, reflected surge voltage, SiC power converters, long cables, high-frequency model, smart coils.

Lulu Wei

May 13, 2024

MITIGATION OF REFLECTED OVERVOLTAGE IN WIND-TURBINE GENERATOR-CONVERTER SYSTEMS WITH A SMART COIL CONCEPT

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TABLE OF CONTENTS

Acknowledgments iii

List of Tables vi

List of Figures vii

Chapter 1 Introduction 1
1.1 Fundamentals of Transient Surge Overvoltage 3
1.1.1 Voltage Reflection Theory 4
1.1.2 Critical Cable Length and Travelling Time 9
1.2 Wind-Turbine Generator-Converter Systems with Long Cables 12
1.3 SiC-MOSFET Modules for MVDC Power Converters 14
1.4 Thesis Organization 16

Chapter 2 Review of Existing Overvoltage Mitigation Strategies 19
2.1 Surge Impedance Matching Solutions 19
2.1.1 RC Filter 19
2.1.2 RLC Filter 21
2.2 Mitigation Solutions by Reducing dv/dt 22
2.2.1 Passive Filter Solutions 23
2.2.2 Enhanced Gate Driver Solutions 26
2.2.3 Soft-Switching Solutions 28
2.2.4 Mitigation with Multi-level Power Converter Typologies . . . 30
2.3 Active PWM Control Solutions 33
2.3.1 3-Voltage-Step PWM Scheme 33
2.3.2 PWM Scheme with n Voltage Steps 35
2.4 Integrated Machine-Drive Solutions 37

Chapter 3 High-Frequency Modeling of Wind-Turbine Generator-Converter Systems 39
3.1 High-Frequency Modeling of Electric Machines 39
3.1.1 Review of the Existing High-Frequency Model 39
3.1.2 High-Frequency Parametric Measurement 44
3.2 High-Frequency Modeling of Power Converters 49
3.3 High-Frequency Modeling of Power Cables 50
3.3.1 Review of Existing High-Frequency Models 51
3.3.2 High-Frequency Parametric Measurement 54

Chapter 4 Proposed Smart Coil Solution 64
4.1 Operating Principle of the Smart Coil Concept 64
4.2 Control of the Smart Coil Circuit 68

4.3 Parametric Sizing of the Smart Coil Circuit 70

Chapter 5 Simulation Results 76
5.1 Baseline Simulation of the Generator-Converter System 76
5.2 Overvoltage Mitigation with the Proposed Smart Coil Concept 79
5.3 Conclusion 83

Chapter 6 Conclusion and Future Work 88
6.1 Conclusion 88
6.2 Future Work 90
6.2.1 Experimental Verification 90
6.2.2 Develop an Adaptive Control Scheme for the Smart Coil . . . 91
6.2.3 Develop a Design Automation Software Tool 92
6.2.4 Develop a Self-Powered Gate Driver DC Supply Circuit 92

Bibliography 93

LIST OF TABLES

1.1 The hub heights from different manufacturers. 14

3.1 The matched parameters of the proposed high-frequency per coil model. 47
3.2 The coils to ground resistance and capacitance. 48
3.3 The parameters of SiC switching device C2M0045170D. 50
3.4 The parameters of selected cable(29m). 55
3.5 The parameters of RL ladder circuit. 58
3.6 The parameters of RC ladder circuit. 60
3.7 The optimized cable parameters 61

4.1 The parameters of the smart coil 68

LIST OF FIGURES

1.1 Global wind energy historic development of total installations [1]. 1
1.2 The location of the converter. 2
1.3 General power converter, cable and electric machine system. 4
1.4 The transient voltage reflection and transmission diagram. 6
1.5 The transient surge overvoltage on an electric machine terminal. 8
1.6 Piecewise analysis of surge voltage reflection. 11
1.7 Downtime percentage of wind-turbine components. [6] 13
1.8 The wind turbine generator-converter system. 13
1.9 The comparisons of total switching losses between Si IGBT and SiC MOSFET [11]. 15

2.1 The RC filter at the generator terminal. 20
2.2 The RLC filter at the generator terminal. 22
2.3 The LCR filter at the power converter terminal (only one phase shown). 23
2.4 The LC-DRC clamp filter at the power converter terminal. 24
2.5 Gate driver based dv/dt limitation topology with changing gate resistor. 26
2.6 Enhanced gate driver based dv/dt limitation topology with additional capacitor. 27
2.7 Transient voltage and current in hard switching process. 28
2.8 Transient voltage and current in soft switching process. 28
2.9 The ARCP soft-switching circuit [17]. 29
2.10 The ARSEP soft-switching circuit [23]. 30
2.11 The three-level T type inverter topology. 31
2.12 The five-level diode clamped inverter topology. 32
2.13 PWM voltage pattern having $V_{DC}/2$ level at each pulse transition [26]. . 32
2.14 The voltage pulse at the inverter and motor terminals [27]. 34
2.15 Active reflected wave canceller circuit topology [29]. 35
2.16 Multi-steps PWM scheme [30]. 36
2.17 Single phase schematics of a multi-voltage steps converter [30]. 36

3.1 High-frequency model of electric machines (per phase). 40
3.2 High-frequency model of electric machines (per coil per phase). 41
3.3 High-frequency model of electric machines (per turn per coil). 42
3.4 Proposed high-frequency per coil equivalent circuit of the generator . . . 43
3.5 Experimental generator with taps for each coil 45
3.6 The HIOKI LCR meter IM3536 46
3.7 The tapped generator used for high-frequency modeling 46
3.8 6 coils impedance measurement data of experimental generator 47
3.9 Proposed equivalent circuit impedance matched with the measurement data. 48
3.10 The power converter with SiC MOSFETs 51
3.11 The equivalent circuit of the transmission line 52

3.12 The high-frequency cable model considering dielectric losses 53
3.13 The high-frequency cable model considering dielectric losses, skin and proximity effects 53
3.14 The high-frequency cable model considering resonance and anti-resonance frequency 54
3.15 The high-frequency cable model with RL and RC ladder circuits 55
3.16 The high-frequency cable model chosen for generator-converter system . 56
3.17 Power cables with 12-AWG and a length of 1-meter 56
3.18 The matching of the impedance magnitude 57
3.19 The matching of the impedance magnitude 57
3.20 The ratio of impedance from the lab measurement and RL ladder circuit 58
3.21 The matching of the impedance magnitude for RC ladder circuit 59
3.22 The matching of the impedance phase for RC ladder circuit 59
3.23 The ratio of impedance from measurement and RC ladder circuit 60
3.24 The magnitude matching of the short-circuit and open-circuit impedance in differential mode. 61
3.25 The phase angle matching of the short circuit and open circuit impedance in differential mode 62
3.26 The magnitude matching of the short circuit and open circuit impedance in common mode 62
3.27 The phase angle matching of the short circuit and open circuit impedance in common mode 63
3.28 The cable common-mode impedance measurement 63
3.29 The cable DM impedance measurement 63

4.1 The proposed smart coil circuit applied to the first coil 65
4.2 The impedance of the first coil with different capacitors 65
4.3 The proposed smart coil circuit applied to the first two stator coils . . . 67
4.4 The coil voltages comparisons with different circuit typologies 68
4.5 The control logic for the smart coil circuit 69
4.6 The controlled coil voltages 70
4.7 The coil voltages with different fixed capacitors 71
4.8 The coil voltages with different parameters of the first smart coil 72
4.9 The coil voltages with different parameters of the second smart coil . . . 73
4.10 The coil voltages with different parameters of the second smart coil . . . 74

5.1 The line-to-line voltage comparisons between the converter and generator terminals 77
5.2 The uneven voltage distribution on different coils 78
5.3 The line-to-line voltage across the generator terminal with different cable length and rise time 79
5.4 The first coil voltage with different cable length and rise time 80
5.5 The coil voltages with smart coil on the first coil 81
5.6 The coil voltages with smart coil on the first and second coils 82

5.7 Comparisons of the coil voltages with and without the smart coils (cable length = 29 m, rise time = 40 ns). 82
5.8 The coil voltages with smart coil connected across the first coil. 83
5.9 The coil voltages with smart coil connected across the first and second coils. 84
5.10 Comparison of the coil voltages with and without the smart coils (cable length = 60 m, rise time = 20 ns). 84
5.11 The coil voltages with smart coil connected across the first and second coils. (threshold voltage = 160 V) 85
5.12 The coil voltages comparisons with and without the smart coils (cable length = 60 m, rise time = 20 ns, threshold voltage = 160 V). 85
5.13 The coil voltages with smart coil connected across the first coil. 86
5.14 The coil voltages with smart coil connected across on the first and second coils. 87
5.15 Comparison of the coil voltages with and without the smart coils (cable length = 120 m, rise time = 20 ns). 87

Chapter 1 Introduction

In 2022, the global wind power capacity experienced a rapid increase of 77.6 GW connected to the power grids, resulting in a total installed wind capacity of 906 GW, marking a 9% increase compared to the previous year [1]. Fig. 1.1 presents the worldwide wind energy historic development of total installations, and approximately 358% growth has been observed from 2010 to 2022 and its capacity still keeps increasing. As a clean energy source, wind energy has a promising contribution to the reduction of greenhouse gas emissions and the enhancement of energy sustainability. Considering this background, the technologies of wind-turbine systems have been significantly developed, such as initiatives of developing medium-voltage SiC power converters for wind power applications [2]. As a safety-critical application, securing the high reliability of wind generators, cables, and power converters is of paramount importance.

In both high-power onshore or offshore wind power generation systems, generators

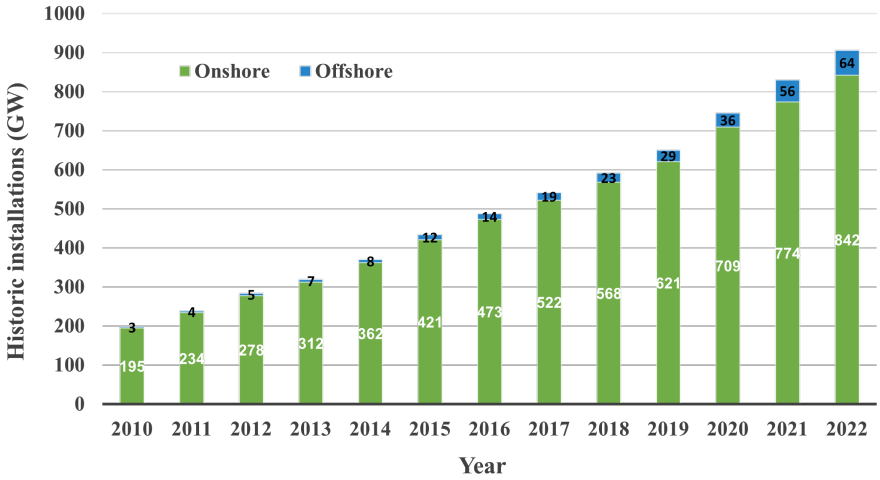


Figure 1.1: Global wind energy historic development of total installations [1].

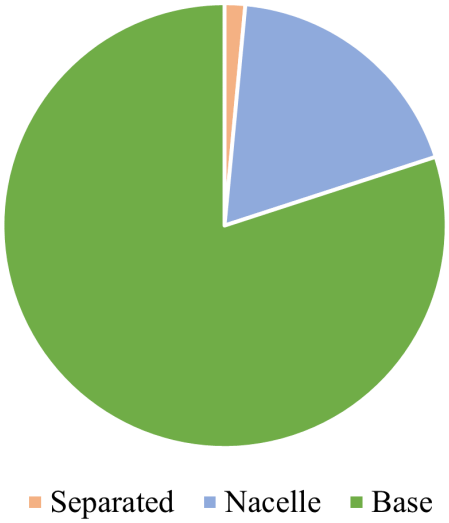


Figure 1.2: The location of the converter.

are generally located in the nacelle of the tower, while power converters are located on the bottom of the tower due to the nacelle space constraint and maintenance convenience [3]. Fig. 1.2 shows that more than 75% of the wind turbine systems have the power converter installed at the base [3]. Consequently, long power cables are needed to connect the generator to the power electronic converters, which may unfortunately induce high-frequency reflected overvoltage across the generator stator windings, due to mismatch of the surge impedance and the short rise time of semiconductor switching. Such high-frequency overvoltage spikes occurring across the generator stator windings can easily damage the dielectric insulation of the generator, which may lead to cascaded system faults or even massive power outages. There are three major factors related to the occurrence of the reflected overvoltage issue: high dv/dt in the converter output line voltages, surge impedance mismatch, and long cables interconnected between the generator and power converter. Firstly, the high dv/dt is caused by the utilization of fast-switching semiconductor devices such as SiC MOSFETs in the power converters. The short rise time with SiC MOSFETs is beneficial for reduc-

ing the switching losses of the power converters, but unfortunately, it results in high dv/dt in the line-to-line voltages, posing increased stress on the dielectric insulation of generator windings. Secondly, at high frequencies, the inductance in the generators will exhibit an open circuit resulting in very high impedance. The voltage wave will be reflected when the impedance of the generator is much higher than that in the cables or converters during the propagation process. Such reflected voltages will be superposed to the incident voltage waves and induce surge overvoltages on the generator stator windings. The last factor is the long power cables connected between generators and power converters, which can be up to 500 feet for wind power applications, easily causing voltage reflection and surge overvoltages. To guarantee reliable and safe operation of wind-turbine systems, this thesis will focus on the investigation and mitigation of the reflected overvoltage in the wind-turbine generator-converter systems.

1.1 Fundamentals of Transient Surge Overvoltage

Electrification stands at the forefront of the global movement towards environmentally friendly and sustainable development. It has been a significant driver behind the research and development of adjustable-speed-drive (ASD) application technologies.

Pulse width modulation (PWM) is broadly utilized in the power conversions of ASD systems due to its advantages of efficiency and precise control. However, the phenomenon of voltage on the electric machine terminal being higher than the converter input has been observed and addressed researcher's attention since the early 1990s. Dr. Daugherty and engineer Carl have given an example of higher voltage measured from a motor than the output of a PWM control in their paper, and they emphasized that there is a need for industry standards for AC induction motors

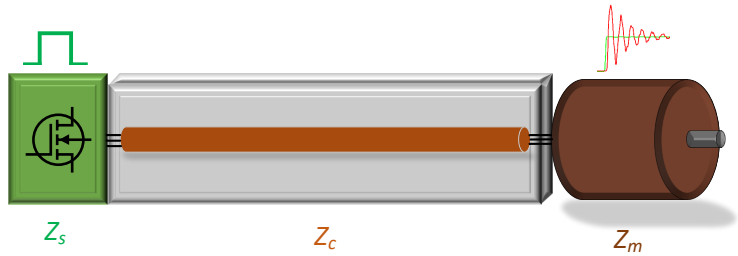


Figure 1.3: General power converter, cable and electric machine system.

regarding this overvoltage issue [4].

1.1.1 Voltage Reflection Theory

In wind-turbine generator-converter systems, steep voltage pulses from the fast-switching power converter will be reflected to the generator due to a mismatch of the surge impedance. Based on the principles of electromagnetic wave propagation in different mediums, the incident wave from the source will propagate towards the terminal and a portion of this incident wave will be reflected towards the source as the reflected wave. Simultaneously, the transmitted wave to the terminal is the sum of the incident wave and the reflected wave. To be specific, in a general power conversion system that consists of a power converter, cables, and an electric machine, the steep voltage pulses generated from the power converter will propagate to the electric machine through power cables, as shown in Fig. 1.3. There are three different mediums with three different surge impedances in such a system: the source impedance Z_s can be seen as low as zero, and the cable impedance Z_c is generally much lower than the machine impedance Z_m. The voltage reflection and transmission coefficient can be written as Equations (1.1) to (1.3). The steep voltage pulses transmitted to the machine stator terminals can be calculated by Equation (1.4) when there is only one reflection based on the electromagnetic wave propagation principles.

$$\Gamma_m = \frac{Z_m - Z_c}{Z_m + Z_c} \tag{1.1}$$

$$\Gamma_s = \frac{Z_s - Z_c}{Z_s + Z_c} \tag{1.2}$$

$$T_m = \frac{2Z_m}{Z_m + Z_c} = 1 + \Gamma_m \tag{1.3}$$

$$V_m = V_s * T_m = V_s * (1 + \Gamma_m) \tag{1.4}$$

where:

- Γ_m: reflection coefficient when an incident wave propagates towards an electric machine
- Γ_s: reflection coefficient when an incident wave propagates towards a power source
- T_m: transmission coefficient when an incident wave propagates towards an electric machine
- Z_m: impedance of an electric machine
- Z_c: impedance of cables
- Z_s: impedance of a power source
- V_m: voltage on a machine terminal
- V_s: voltage on a source(converter) terminal

However, in the transient analysis, there is more than one reflection that happened in the process of pulse propagation from the converter to the machine, as shown in Fig. 1.4. First of all, based on the aforementioned different impedances of the three mediums, the reflection coefficient Γ_m can be close to 1, and Γ_s can be close to -1. t_t is the traveling time of a voltage pulse traveling once between two terminals. When the voltage pulse arrives at the machine terminal for the first time, the transmission

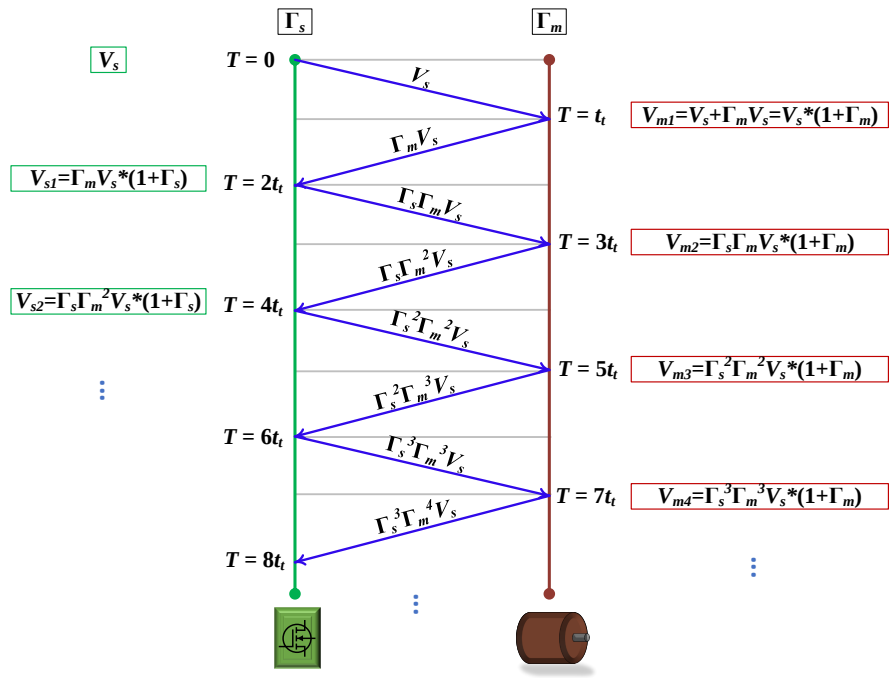


Figure 1.4: The transient voltage reflection and transmission diagram.

and reflection will happen simultaneously which results in the the fact that reflected voltage is V_{m_r1} and the voltage transmitted to the machine is V_{m1}. Afterwards, the reflected voltage V_{m_r1} will travel back to the source and result in the reflected voltage V_{s_r1} and transmitted voltage V_{s1}. The same procedure will continue, and at time $T = 7t_t$ the total voltage transmitted to the electric machine can be calculated by Equation (1.14), and the total voltage transmitted to the source can be obtained by Equation (1.15). On the power converter side, since the value of Γ_s is close to -1, so the value of V_{s1} and V_{s2} derived from Equations (1.12) and (1.13) are approximately zero. This leads to the value of V_{s_total} approximately equal to V_s, which is why no severe overvoltage occurs on the converter side. Similar to the electric machine side, the transmitted voltage V_{m1} is almost twice V_s in case Γ_m is near to 1 when the first reflection happens. This is also the time point when the voltage peak value occurs. Moving to the second reflection time point, the value of V_{m2} is negative since the

negative factor Γ_s is involved but the absolute value of V_{m2} is still smaller than V_{m1} in the real scenario. Then it will lead to the total voltage waveform at this time point reaching a trough. At the third reflection time point, the value of V_{m3} is positive which leads to the total voltage being higher than the source voltage again. In this way, the voltage waveform on the machine terminal will exhibit the surge overvoltage phenomenon as shown in Fig. 1.5. The time between the crest and the trough is the same as the time between adjacent reflections which is $2t_t$ and the half of one oscillation period of an overvoltage wave. Afterwards, the overvoltage wave oscillation frequency can be shown as Equation (1.16), which is also combined with Equation (1.5). Thus, the oscillation frequency is closely related to the cable length.

The first wave reflection determines the peak overvoltage value, and eventually, this overvoltage will mostly pose insulation stress on the first few coils in the machine which may cause a rapid aging of the machine or a collapse of the machine operation if there is no mitigation solution available. Fig. 1.5 shows that the value of the electric machine voltage will be converted to the source voltage after a while, which is because the value of Γ_m and the absolute value of Γ_s are both lower than one in the real-world applications.

$$t_t = \frac{l_c}{v_t} \tag{1.5}$$

$$V_{m_r1} = \Gamma_m V_s \tag{1.6}$$

$$V_{s_r1} = V_{m_r1} * \Gamma_s = \Gamma_s \Gamma_m V_s \tag{1.7}$$

$$V_{m_r2} = V_{s_r1} * \Gamma_m = \Gamma_s \Gamma_m^2 V_s \tag{1.8}$$

$$V_{s_r2} = V_{m_r2} * \Gamma_s = \Gamma_s^2 \Gamma_m^2 V_s \tag{1.9}$$

$$V_{m1} = V_s + V_{m_r1} = V_s + \Gamma_m V_s = V_s * (1 + \Gamma_m) \tag{1.10}$$

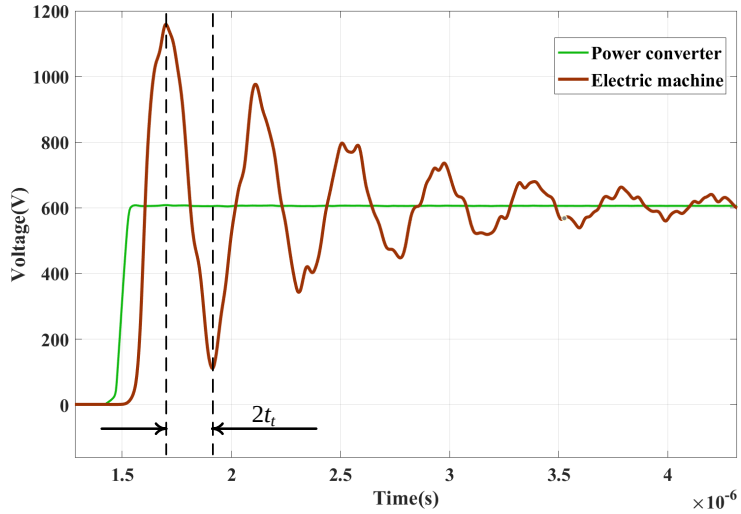


Figure 1.5: The transient surge overvoltage on an electric machine terminal.

$$V_{m2} = V_{s_r1} + V_{m_r2} = \Gamma_s \Gamma_m V_s + \Gamma_s \Gamma_m^2 V_s = \Gamma_s \Gamma_m V_s * (1 + \Gamma_m) \tag{1.11}$$

$$V_{s1} = V_{s_r1} + V_{m_r1} = \Gamma_s \Gamma_m V_s + \Gamma_m V_s = \Gamma_m V_s * (1 + \Gamma_s) \tag{1.12}$$

$$V_{s2} = V_{s_r2} + V_{m_r2} = \Gamma_s^2 \Gamma_m^2 V_s + \Gamma_s \Gamma_m^2 V_s = \Gamma_s \Gamma_m^2 V_s * (1 + \Gamma_s) \tag{1.13}$$

$$V_{m_total} = \sum_{i=1}^{n} V_{mi},\ i = 1, 2 \ldots n,\ at\ T = (2i - 1)t_t \tag{1.14}$$

$$V_{s_total} = \sum_{i=1}^{n} (V_s + V_{si}),\ i = 1, 2 \ldots n,\ at\ T = 2i * t_t \tag{1.15}$$

$$f_{osc} = \frac{1}{4t_t} = \frac{v_t}{4l_c} \tag{1.16}$$

where:

- t_t: the traveling time of a voltage pulse traveling once between a power converter and an electric machine

- l_c: the cable length

- v_t: the pulse traveling speed which is approximately half of the light speed [5]

- V_{m_ri}: the ith time reflected voltage on the electric machine terminal

- V_{s_ri}: the ith time reflected voltage on the converter terminal

- V_{mi}: the transmitted voltage on the electric machine terminal when the ith time reflection happens

- V_{si}: the transmitted voltage on the converter when the ith time reflection happens

- V_{m_total}: the total transmitted voltage on the electric machine terminal at $T = (2i-1)t_t$

- V_{s_total}: the total transmitted voltage on the converter terminal at $T = 2i * t_t$

- f_{osc}: the oscillation frequency of the overvoltage standing wave

1.1.2 Critical Cable Length and Travelling Time

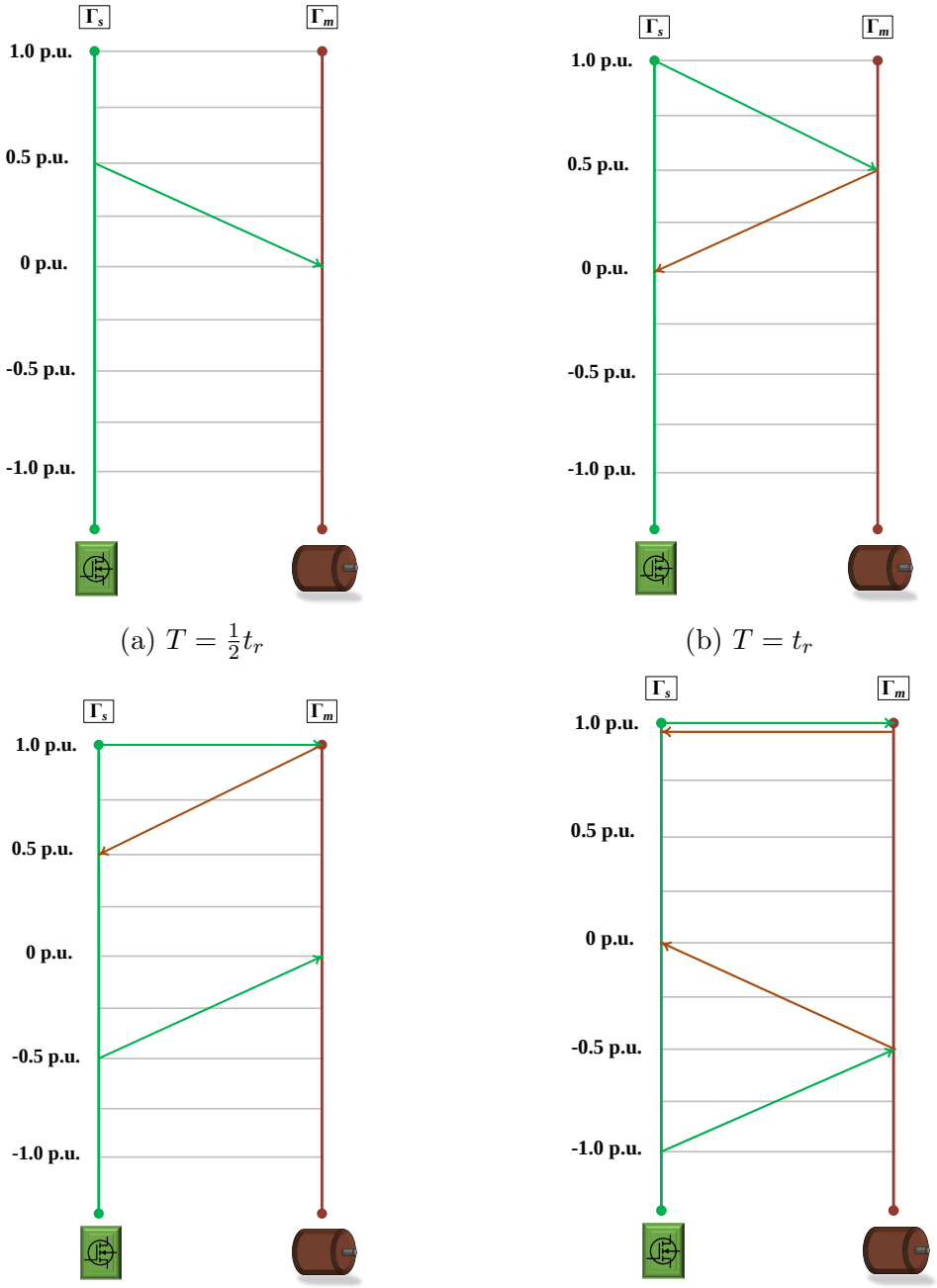
The above descriptions and the surge voltage phenomenon shown in Fig. 1.4 and 1.5 have an assumption that the pulse traveling time is much longer than the pulse rise time, which indicates that there is a long cable connected between the power converter and electric machine. In Fig. 1.4, the pulse rise time is ignored since it is far shorter compared to the traveling time. However, in the case that the pulse rise time is comparable to the pulse traveling time, the voltage will not be doubled on the machine terminals. Thus, one question that is being answered is what is exactly the critical value of traveling time?

There are two characteristics of voltage pulses that can not be neglected: the voltage pulse traveling speed and the pulse rise time. The pulse traveling speed determines the traveling time when the cable length is given, and the relationship between pulse rise time and pulse traveling time will determine whether the pulse will be doubled on the machine terminal. The author Erik Persson addressed two important points regarding the transient pulses transmission process: the voltage

pulses will travel at approximately half of the speed of the light; if the pulses take longer than half of the rise time to travel from the power converter to the electric machine, the pulse amplitude will approximately be doubled on the machine terminal [5]. In the case of $t_t \geq \frac{1}{2}t_r$, where t_r is the pulse rise time, the peak voltage can be calculated by Equation (1.10) and it is nearly twice the source voltage. In the case that the critical cable length is defined as the value whenever the cable length is longer than that value, the overvoltage on the machine terminal is nearly doubled. With this precondition, the critical cable length can be approximately obtained by Equation (1.17) when the pulse rise time is determined by the semiconductor switches. This equation can provide a basic design principle about how to tune the semiconductor gate circuit for an appropriate rise time and the cable length regarding the overvoltage issues.

$$l_c \geq \frac{v_t t_r}{2} \tag{1.17}$$

Here is a question still not answered yet, why it is the condition of $t_t \geq \frac{1}{2}t_r$ that will cause the maximum overvoltage? As discussed above, the first peak value of the surge voltage is the point that needs to be paid attention. A voltage reflection starts before the voltage pulse peak value arrives at the machine terminal. In the case of $t_t = \frac{1}{2}t_r$, every point of the pulse starts from zero to the peak value will need a duration of t_t traveling to the machine terminal, and the piecewise analysis is shown in Fig. 1.6. Assuming that the voltage pulse is linearly rising by the time, Fig. 1.6a shows the pulse rising to 0.5 p.u. when $T = t_t$ on the converter side, and the starting point (which is zero) of the pulse just arrives at the machine side, so the reflection does not start yet at this moment. After another t_t period, the voltage pulse across



(a) $T = \frac{1}{2}t_r$

(b) $T = t_r$

(c) $T = \frac{3}{2}t_r$

(d) $T = 2t_r$

Figure 1.6: Piecewise analysis of surge voltage reflection.

the converter side rises to 1.0 p.u., which rises to 0.5 p.u. on the machine side, and at the same time the reflection already happened and the starting point of the reflected voltage V_{m_r1} just arrives at the converter side. At this moment, the total voltage transmitted to the machine is $0.5 + 0.5 = 1.0$ p.u. Moving to the next stage, at $T = \frac{3}{2}t_t$, the pulse rises to 1.0 p.u. on the machine side, and the reflected voltage V_{m_r1} rises to 0.5 p.u. on the converter side. Additionally, the first reflected voltage from the converter side V_{s_r1} is -0.5 p.u. and this reflected pulse's starting point just arrived at the machine side. At this moment, the total voltage on the machine side is 2.0 p.u. which is the maximum voltage it could reach on the machine side. Since the negative voltage value reflected from the converter side V_{s_r1} still does not arrive at the machine terminal yet, it makes the first peak voltage value of 2.0 p.u. on the machine side occur. In the case of $t_t > \frac{1}{2}t_r$, the starting point of the V_{s_r1} even can not arrive at the machine terminal. In the case of $t_t < \frac{1}{2}t_r$, the negative value of V_{s_r1} already arrived at the machine terminal which makes the total voltage value on the machine side less than 2.0 p.u. This also answers the question from the beginning and explains why the condition of $t_t \geq \frac{1}{2}t_r$ will cause maximum overvoltage. Fig. 1.6d shows that, at $T = 2t_t$, the total voltage on the machine terminal is $1 + 1 - 0.5 - 0.5 = 1.0$ p.u. and the surge voltage phenomenon will occur over time.

1.2 Wind-Turbine Generator-Converter Systems with Long Cables

Wind-turbine technologies are advancing rapidly and wind power installation has been significantly growing in worldwide. During this development process, many technical challenges are occurring at the same time. Fig. 1.7 shows the downtime percentage caused by different components of wind turbine systems. Specifically, gears, power converters, generators, and control systems are the most vulnerable

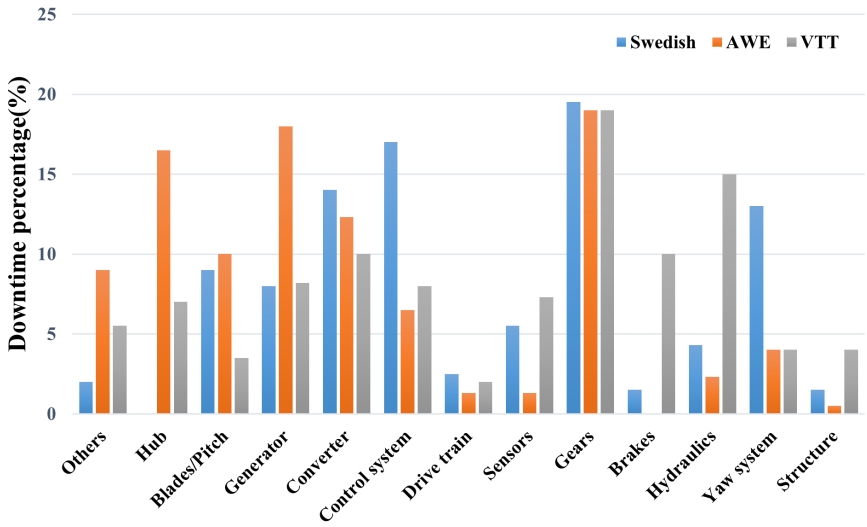


Figure 1.7: Downtime percentage of wind-turbine components. [6] [7]) [8].

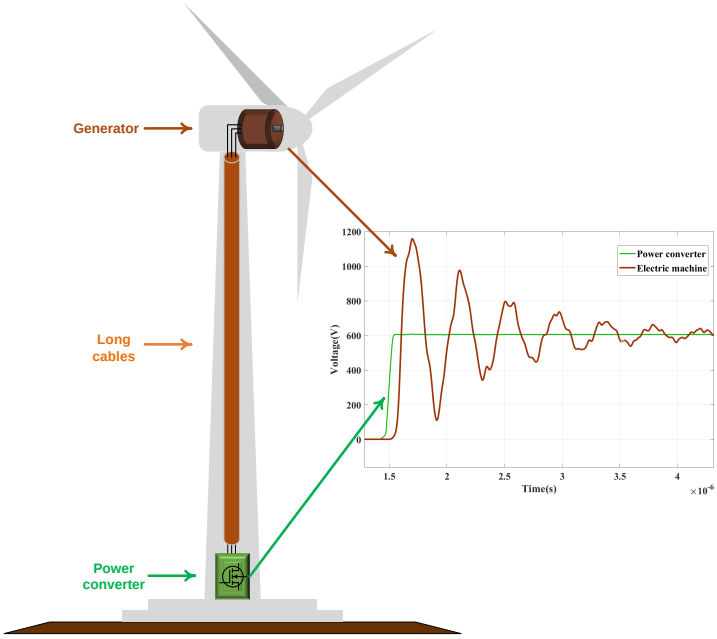


Figure 1.8: The wind turbine generator-converter system.

components contributing to systematic faults and downtime costs.

The aforementioned reflected overvoltage issue will break down the machine's stator winding insulation and result in generator failures. Since the power converter also has a relatively high failure rate, power converters are generally placed on the

Table 1.1: The hub heights from different manufacturers.

	Vestas	GE	Goldwind	Envision	Siemens
Model number	V174-9.5	Haliade-X	GW 140	EN-156	SG 7.0-170
Power(MW)	9.5	14	3.4	3.3	7
Hub height(m)	110	150	100/110	140.5	115-185
Application	Off-shore	Off-shore	On-shore	On-shore	On-shore

bottom of the turbine tower in most of the high-power wind turbine systems, as shown in Fig. 1.8. Such hardware physical configuration is convenient for the maintenance of the power converters, which also helps save space for the nacelle of the tower. However, the long cables connected between the generator and converter will result in a steep voltage pulse traveling time much longer than the pulse rise time, which may cause severe overvoltage across the stator windings of the generator. The hub height of the wind turbine system is typically in the range of 80–165m according to the products' specifications from different manufacturers, as shown in Table 1.1. Even in the case that the cables are not too long such as shorter than 100 feet, the overvoltage issue may still exist, posing a reliability concern for the generator. For example, in the case that the rise time $t_r = 100ns$ and the pulse traveling speed is half of the light speed, with a critical cable length of 7.5m, the voltage will reach 1.2 p.u. on the generator stator windings side even when the cable length is just 1.5m. Therefore, the solution to mitigate the surge voltage transmitted to the generator terminal is indispensable to avoid downtime and maintenance costs.

1.3 SiC-MOSFET Modules for MVDC Power Converters

Pursuing high efficiency and high power density are two driving factors motivating the research and advancement of fast-switching semiconductor devices for power converters. The performance of conventional Silicon (Si) based semiconductor devices

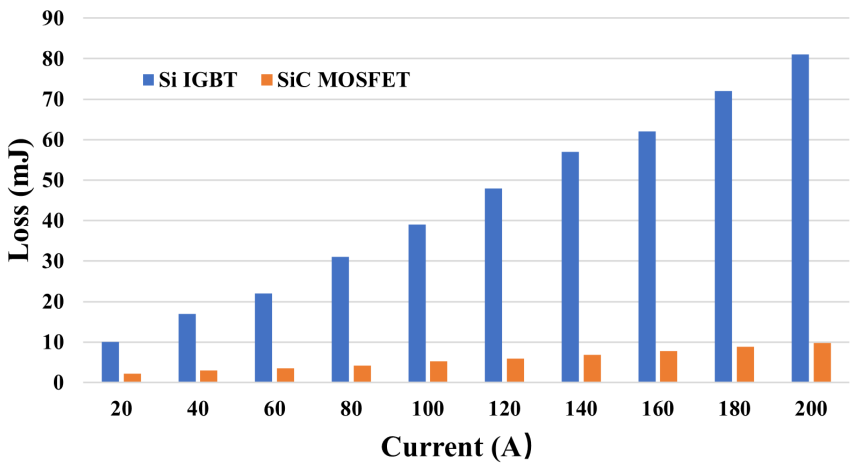


Figure 1.9: The comparisons of total switching losses between Si IGBT and SiC MOSFET [11].

is almost approaching their limits due to the inherent characteristics of the material [9] [10]. The advent of wide-bandgap semiconductors such as Silicon Carbide (SiC) and Gallium Nitride (GaN) has opened up significant possibilities to expand the voltage, power, frequency, and operation temperature of next-generation power converters [11].

Compared with the conventional Si IGBTs, SiC MOSFETs possess lower switching losses since the switching voltage and current overlapping area are much smaller during the turn-on and turn-off transient process. Such performance enables higher efficiency and higher switching frequency. The double pulse test results for both the Si IGBT module (FF200R17KE3, 1700 V/310 A, Infineon) and SiC MOSFET module (CAS300M17BM2, 1700 V/325 A Cree/Wolfspeed) have been compared and presented in paper [11]. Fig. 1.9 shows the comparison between the total switching losses of these two semiconductor devices, where the SiC MOSFET has much lower losses.

However, along with many advantages of SiC MOSFET devices, one of the chal-

lenges is that the shorter rise time will cause much higher dv/dt which will make the overvoltage issue more severe for machine-converter applications. Section 1.2 shows an example of critical cable length calculation under the condition of $t_r = 100ns$, while the state-of-the-art semiconductor technologies even can achieve lower rise time such as $t_r = 50ns$, which makes the critical cable length decrease to 3.75m. Therefore, the latest semiconductor technologies of SiC MOSFET devices will bring more challenges in terms of reflected overvoltage issues. Furthermore, in the case of high switching frequency and high duty cycle at the same time which means that the voltage oscillation may be not fully convergent when the next pulse arrives, then the double pulsing occurs and the overvoltage can reach up to 4 p.u. in one switching event [12]. This is the worst scenario to be considered during the product design and the solution to mitigate the overvoltage is critical.

1.4 Thesis Organization

There are 7 chapters to be presented in this thesis, which are outlined as follows:

Chapter 1 firstly reviews the fundamental theory behind the transient surge overvoltage phenomenon including the voltage reflection mechanism and the critical cable length calculation. The application scenario of the wind-turbine generator-converter system is discussed and the root cause of reflected overvoltage across the generator windings is analyzed. The utilization of the fast-switching SiC MOSFET in power converters is introduced and the reason why it deteriorates the existing surge overvoltage problem is investigated.

Chapter 2 includes a thorough review of the existing solutions to mitigate reflected overvoltage on electric machine terminals. Passive filters at the machine terminals are well-established industrial solutions that aim to match the surge impedance between

power cables and generators. dv/dt mitigation with passive filters at the output of power converters, advanced power converter topologies with staircase line voltage waveforms, and enhanced gate-driver solutions with controllable dv/dt are also effective approaches to reduce overvoltage. Integrated machine-drive solutions have been widely implemented for electric vehicle (EV) industries. The pros and cons of all these solutions are discussed in this chapter.

Chapter 3 describes the process of high-frequency modeling for the wind turbine generator-cable-converter system. The existing high-frequency models are reviewed first and the R-L ladder circuit model with high accuracy is adopted in the research of this thesis. The surge impedance measurements for the cables and machine in a broad frequency range (e.g., up to 8 MHz) are executed. The equivalent R-L ladder circuit parameters are extracted by the optimization method with the impedance measurement data. The high-frequency model of the SiC power converter with Pulse Width Modulation (PWM) control strategy is modeled in the LTspice software environment.

Chapter 4 details the proposed smart coil solution, its operating principles, and components parametric sizing. The smart coil concept considers a fact that uneven distribution across different coils of the reflected surge voltages in the generator stator windings. Specifically, the first one or two coils withstand the majority of the voltage stress and therefore their dielectric insulation property can easily break down. The proposed smart coil mitigation method is to add an ultra-compact mitigation circuit only on the first one or two coils (ideally, only for the first coil) instead of all the stator coils of the machine. The advantages of the proposed smart coil concept in comparison with the existing mitigation solutions are analyzed in this chapter as well.

Chapter 5 presents the simulation results of the voltage reflection occurring in the generator-converter system with different cable lengths and semiconductor rise times.

The line-to-line voltages on the generator terminal change with different cable lengths and rise times, which also verifies the voltage reflection theory presented in Chapter 1. The uneven voltage distribution on different machine coils is shown in the simulation results. Afterwards, the smart coil circuit is implemented in the generator-converter system model and its effectiveness is demonstrated at the end.

Chapter 6 summarizes the findings from the simulation and experimental investigations in terms of the reflected overvoltage issues and the mitigation with the proposed smart coil concept. The future work to consolidate the proposed topic is also presented for further improvement.

Chapter 2 Review of Existing Overvoltage Mitigation Strategies

The voltage reflection issue that exists in machine-converter systems has been investigated by engineers and researchers decades ago, initiated for transmission lines and motor-drive systems [4]. As a result, there are multiple mitigation solutions proposed and implemented in power industries so far. As discussed in Chapter 1, there are three main factors contributing to the voltage reflection problems, namely, the surge impedance mismatch between the cables, converters, and generator, the increasingly high dv/dt due to the short rise time of semiconductor switches and increasing system voltages, and the long cables connected between power converters and electric machines. Accordingly, the existing solutions to avoid such surge overvoltages on the generator terminals can be classified in three directions by targeting these three reasons mentioned above.

2.1 Surge Impedance Matching Solutions

Surge Impedance mismatch between power cables and electric machines is one of the core reasons that results in voltage reflection issues. The surge impedance of the motor is generally much higher than that of the cables [5]. Installing a passive filter in parallel with the machine can effectively reduce the combined surge impedance of the machine, bringing it comparable to the impedance of the cables.

2.1.1 RC Filter

One method to match the cable characteristic impedance is by adding an RC circuit in parallel to the machine as shown in Fig. 2.1 [13]. The cable character-

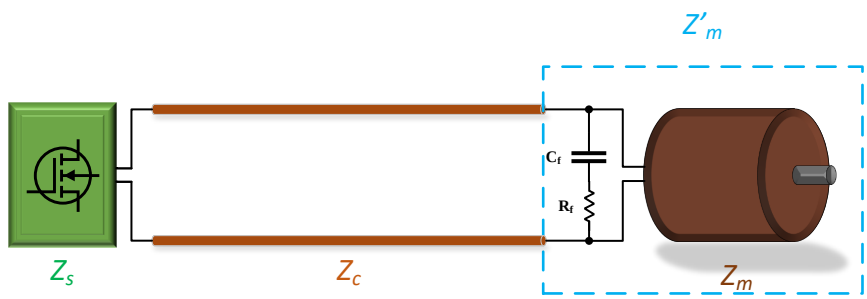


Figure 2.1: The RC filter at the generator terminal.

istic impedance Z_c is given by Equation (2.1) [14], assuming that the transmission line is lossless, and the equivalent impedance of the filter is given by Equation (2.2). Since the generator characteristic impedance is much higher than the impedance of the filters and cables, the combined characteristic impedance of the generator and filter will be close to the value of filter impedance and so to the cable characteristic impedance. Furthermore, the damping resistance R_f should be designed to provide the filter over-damp characteristic to have the minimum overvoltage on the generator terminals [15]. With Equations (2.2) and (2.3), the filter's parameters can be determined with the goal of characteristic impedance matching.

This RC filter can effectively mitigate the overvoltage with a straightforward design of the filter parameters and topology, but the filter power losses might be high and the filter might be bulky. Therefore, the related applications may compromise the systematic efficiency and power density.

$$Z_c = \sqrt{\frac{L_c}{C_c}} \tag{2.1}$$

$$Z_f = \sqrt{R_f^2 + (\frac{1}{\omega_f C_f})^2} = \sqrt{\frac{L_c}{C_c}} = Z_c \tag{2.2}$$

$$R_f > 2\sqrt{\frac{L}{C_f}} \tag{2.3}$$

where:

-Z_c: the cable characteristic impedance

-L_c: the cable inductance per unit length

-C_c: the cable capacitance per unit length

-Z_f: the filter characteristic impedance

-R_f: the resistance of the RC filter

-C_f: the capacitance of the RC filter

-L: the lumped inductance of the cable

2.1.2 RLC Filter

Another type of passive filter that can be added to the generator terminal is the second-order RLC filter, which includes an additional inductor connected in parallel with the resistor in the RC filter, as shown in Fig. 2.2. The equivalent characteristic impedance of the filter is given by Equation (2.4), and similarly, the damping resistance R_f should meet the requirement of over-damp function, as shown by Equation (2.5).

$$Z_f = \sqrt{\left(\frac{R_f\omega_f^2 L_f^2}{R_f^2 + \omega_f^2 L_f^2}\right)^2 + (\frac{R_f^2\omega_f L_f}{R_f^2 + \omega_f^2 L_f^2} - \frac{1}{\omega_f C_f})^2} = \sqrt{\frac{L_c}{C_c}} = Z_c \tag{2.4}$$

$$R_f < \frac{\sqrt{L_f C_f}}{2C_f} \tag{2.5}$$

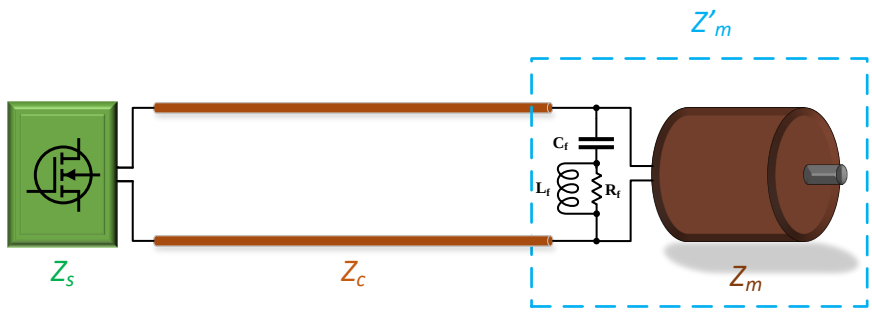


Figure 2.2: The RLC filter at the generator terminal.

where:

-L_f: the inductance of the RLC filter

A system consisting of a 3-phase 460-V 5-hp induction motor fed by 90m cable has been modeled with various types of passive filters in [15]. In the simulation results, the RC filter topology exhibits a voltage overshoot of 13.12%, while the RLC filter topology displays a higher voltage overshoot of 35.02%. The power losses are relatively high for both types of filters.

2.2 Mitigation Solutions by Reducing dv/dt

The high dv/dt of the voltage pulse output from the power converter is another cause of the reflected overvoltage issue. Adding a passive filter at the power converter side can effectively reduce dv/dt, as the rise time of the voltage pulse is significantly prolonged by the filter. Another approach to decrease the rise time is through an enhanced gate-driver solution, featuring a Miller feedback capacitor in combination with increased gate-driver resistances [16]. Soft-switching technology can be used to not only reduce switching power loss but also control the switching rise/fall time by using additional resonant elements [17]. A 3-level power converter topology can

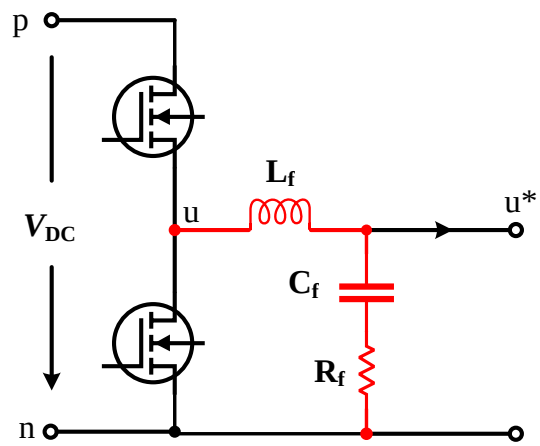


Figure 2.3: The LCR filter at the power converter terminal (only one phase shown).

reduce ΔV from 1.0 p.u. to 0.5 p.u., thereby limiting the maximum overvoltage to 1.5 p.u. All the mentioned solutions aim to reduce dv/dt either by increasing the rise time or decreasing the voltage steps ΔV.

2.2.1 Passive Filter Solutions

Adding a passive filter at the power converter side can reduce the rate of change of the output voltage pulse (dv/dt). Meanwhile, the passive filters do not affect the advantages of low switching losses in the converter semiconductors.

LCR filter

Fig. 2.3 shows the topology of an LCR filter for one phase, which is upgraded from the output reactor and LC filter. The output reactor can effectively mitigate the overvoltage but meanwhile, the voltage drop from the inductor will sacrifice the output torque generation abilities [15][18]. The parametric sizing for the LC filter can be complicated due to the need to avoid the filter resonance frequency [15]. However, the resistor in the LCR filter topology can be used to dampen or eliminate

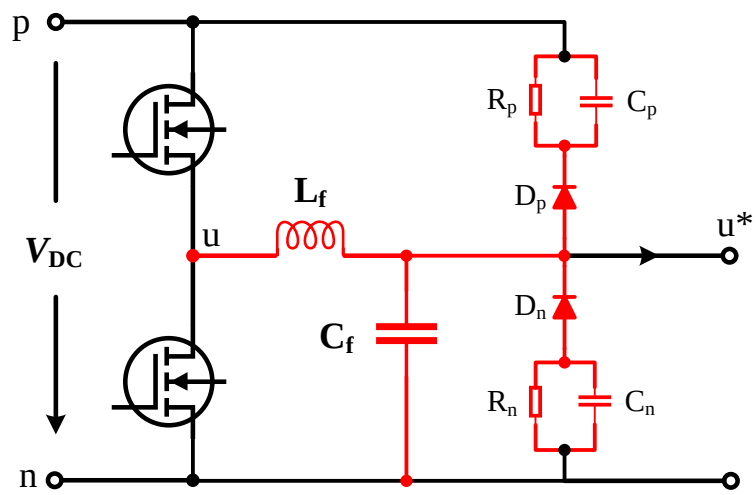


Figure 2.4: The LC-DRC clamp filter at the power converter terminal.

the resonance issue.

An LCR filter was designed based on multi-domain optimization, and the optimization procedures have been presented in [19]. The experimental verification results show the dv/dt can be mitigated from 8 $kV/\mu s$ to 1 $kV/\mu s$ (inverter switching at 40 kHz, gate-off resistance is 5.1 Ω). The mitigation of dv/dt is quite effective as the rise time Δt is increased from 50 ns to 396 ns. However, a slight voltage increase still can be observed and needs to be further suppressed. Moreover, the voltage rise time depends on not only the filter resonance frequency $\omega_0 = 1/\sqrt{L_f C_f}$ but also the selected quality factor $Q = \frac{R_f}{\sqrt{L_f/C_f}}$, which also determines the overshoot [16][20].

LC-DRC clamped damping filter

As the simulation results have been shown in [15], the LCR filter at the inverter side can effectively mitigate the overvoltage but there is still an overshoot of 11.83%. Therefore, the LC filter combined with the DRC damping circuit has been developed, as shown in Fig. 2.4.

In the scenario where the output voltage ranges from 0 V to V_{DC}, the transient process is governed by L_f and C_f, and both diodes are in the blocking condition. When the output voltage either falls below or exceeds the range of 0 V to V_{DC}, diodes D_n or D_p will begin to conduct, and the voltage transient is dampened by resistors R_n or R_p. Additionally, the voltage overshoot can be mitigated during a prolonged discharge time by incorporating capacitors C_n and C_p in parallel with R_n and R_p [20]. The advantage of this filter is the damping effect, and it allows for the decoupling of dv/dt. The voltage rise time and fall time are defined by the desired dv/dt, as shown by Equation (2.6). When the DRC network is disconnected, the transient voltage is defined by the resonance formed with L_f and C_f, as given by Equation (2.7). Subsequently, by substituting the rise time from Equation (2.8), the expression of dv/dt will be obtained, as shown in Equation (2.9) with $\Omega = arccos(0.1) - arccos(0.9) \approx 1.02$. Therefore, the analytical calculation of dv/dt can be determined solely by L_f and C_f when V_{DC} is selected [16].

$$t_r = t_f = \frac{0.8 * V_{DC}}{dv/dt} \tag{2.6}$$

$$v_{u^*n} = V_{DC} * (1 - cos(\omega_0 t)) \tag{2.7}$$

$$t_r = t|_{v_{u^*n(t)=0.9V_{DC}}} - t|_{v_{u^*n(t)=0.1V_{DC}}} \tag{2.8}$$

$$\frac{dv}{dt} = \frac{0.8 * V_{DC}}{(arccos(0.1) - arccos(0.9))/\omega_0} = 0.8 \ * V_{DC} * \frac{\omega_0}{\Omega} \tag{2.9}$$

The simulation results in [20] have shown that the voltage overshoot can be further decreased by the LC-DRC filter compared to the LCR filter. However, the filter characteristic impedance changes when loaded with a motor or even with cable&motor.

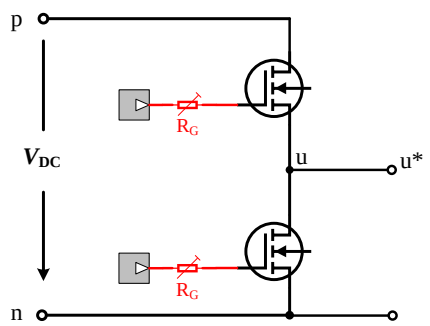


Figure 2.5: Gate driver based dv/dt limitation topology with changing gate resistor.

Therefore, designing this kind of filter becomes challenging due to the uncertainties associated with the electric machine and cable [16].

2.2.2 Enhanced Gate Driver Solutions

Using the gate driver of the semiconductor switches is a more direct approach to reduce the transient changing rate of voltage. Compared to other solution topologies, the gate-driver solution requires a smaller volume of additional elements and, thus, lower cost. The more straightforward and frequently applied topology involves implementing an external gate resistor, as shown in Fig. 2.5. The optimal gate resistance can be determined based on the characteristics of the chosen switching devices [21]. However, this solution has an obvious drawback: the switching losses will increase and converter efficiency will decrease, especially at heavy load or rated load conditions.

The gate driver time constant can be adjusted by the gate resistance. Additionally, to further optimize the transient voltage change process and reduce losses, an extra capacitor can be added. This topology is illustrated in Fig. 2.6, demonstrating that both turn-on and turn-off transitions are slowed down. Detailed analysis of these transitions is provided in [22]. The dv/dt in turn on and turn off conditions can be calculated and determined by the simplified expressions (2.10) and (2.11) [16].

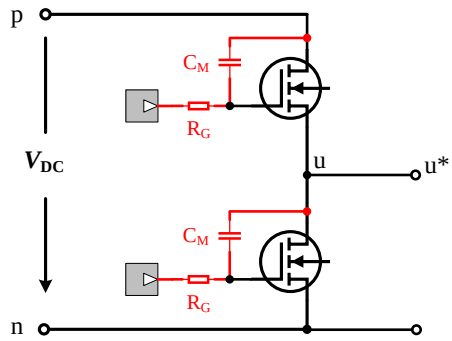


Figure 2.6: Enhanced gate driver based dv/dt limitation topology with additional capacitor.

$$\frac{dv}{dt}|_{on} = \frac{V_{GD,on} - v_{th}}{R_{G,on} * (C_{dQ,GD} + C_M)} \tag{2.10}$$

$$\frac{dv}{dt}|_{off} = \frac{v_{th} + |V_{GD,n}|}{R_{G,off} * (C_{dQ,GD} + C_M)} \tag{2.11}$$

where:

-$R_{G,on}$: the turn on gate resistance

-$R_{G,off}$: the turn off gate resistance

-$C_{dQ,DS}, C_{dQ,GD}$: the charge equivalent linear capacitances for a voltage change between 10% and 90% of V_{DC}

-C_M: Miller capacitor

-v_{th}: the threshold voltage

-$V_{GD,on}$: the gate-drain voltage when switch turn on

-$V_{GD,n}$: the negative gate-driver supply voltage

A comprehensive comparative evaluation of the above-mentioned gate driver solution(with C_M) and LC-DRC filter for SiC-based variable speed motor drive inverters is presented in [16]. The conclusion is summarized as follows: the gate driver solution is better suited for dv/dt-limits above 11 V/ns under both full- and part-load

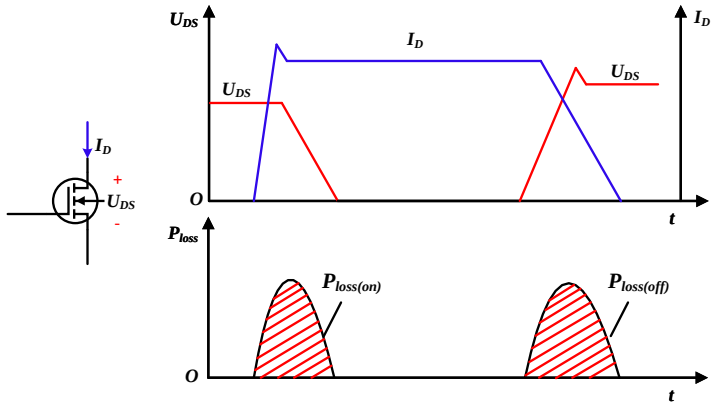
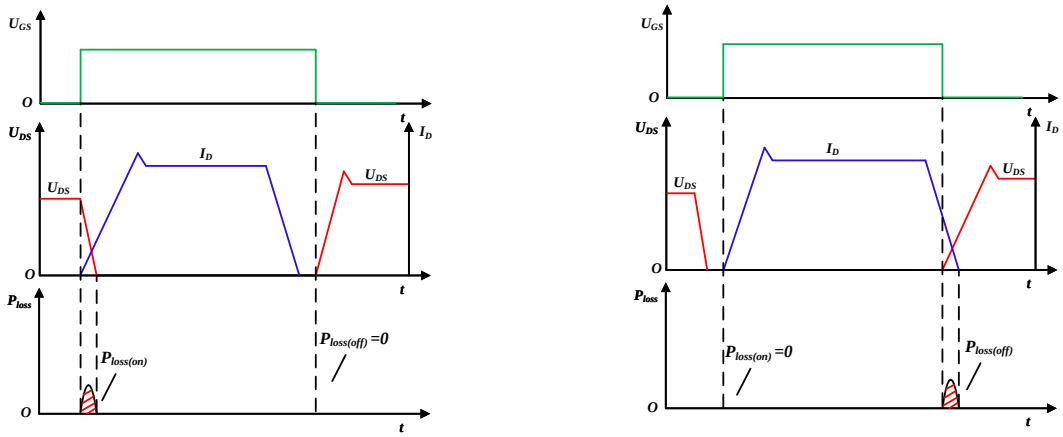


Figure 2.7: Transient voltage and current in hard switching process.



(a) Zero current switching

(b) Zero voltage switching

Figure 2.8: Transient voltage and current in soft switching process.

operation [16].

2.2.3 Soft-Switching Solutions

Soft-switching technologies are developed to further reduce switching losses and improve the converter's efficiency. As depicted in Fig. 2.7 with hard-switching techniques, there is a certain amount of voltage and current overlapping during the turn-on and turn-off transient processes, resulting in power losses. To mitigate these losses, soft-switching techniques control either current or voltage to approach zero before

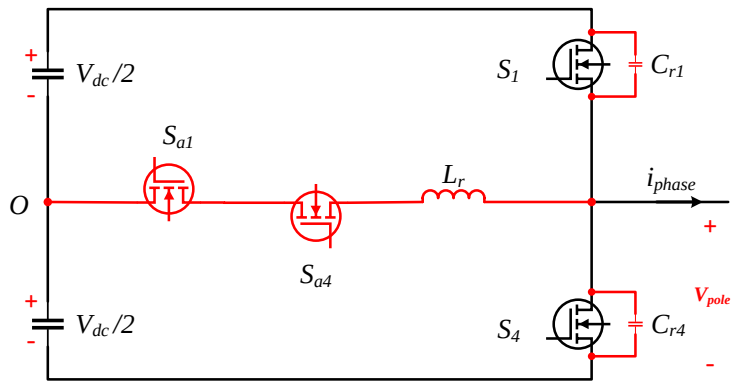


Figure 2.9: The ARCP soft-switching circuit [17].

the actual turn-on or turn-off process, as shown in Fig. 2.8. The power losses with soft-switching are much less than those with hard-switching techniques.

Furthermore, soft-switching techniques offer control over the trajectory of voltage changes by incorporating additional resonant components, allowing for the regulation of dv/dt under a specified limit. The effects of an Auxiliary Resonant Commuted Pole Inverter(ARCP) have been evaluated in [17], as presented in Fig. 2.9. The switching rise time is reported to be 400 ns with a resonance inductance of 2.7 μH and capacitance of 8.2 nF. Experimental results demonstrate nearly zero voltage overshoot on the motor terminal.

Another soft-switching circuit, titled Auxiliary Resonant Soft-Edge Pole (ARSEP), has been demonstrated in [23], as shown in Fig. 2.10. The maximum di/dt and dv/dt can be derived from Equations (2.12) to 2.15 [23]. Simulation and experimental results show that dv/dt can be controlled under a limit of 200 $V/\mu s$, and concurrently, the efficiency of the ARSEP inverter is higher than that of the hard-switching inverter with a dv/dt filter [23]. Furthermore, it has been demonstrated that the ARSEP circuit can help reduce the input DC voltage ripple [23].

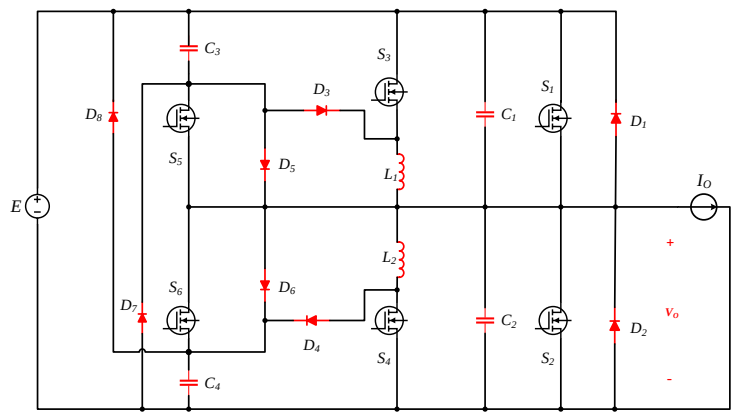


Figure 2.10: The ARSEP soft-switching circuit [23].

$$\frac{di_L}{dt}|_{max} = \frac{E}{L} \tag{2.12}$$

$$\frac{dv_o}{dt}|_{max} = \frac{0.8E\omega_1}{\Delta\theta_{S2D}(\bar{Z}_1)} \tag{2.13}$$

$$\Delta\theta_{S2D}(\bar{Z}_1) = \cos^{-1}\frac{0.1}{\sqrt{\bar{Z}_1^2+1}} - \cos^{-1}\frac{0.9}{\sqrt{\bar{Z}_1^2+1}} \tag{2.14}$$

$$\bar{Z} = \frac{I_p Z}{E} \tag{2.15}$$

2.2.4 Mitigation with Multi-level Power Converter Typologies

The aforementioned methods, including passive filters, smart gate driver solutions, and soft-switching solutions, all aim to increase the rise time of the voltage pulse to reduce dv/dt. From another perspective, the same goal can be achieved by mitigating the voltage changes(ΔV). In a traditional two-level converter, the output voltage pulse with $\Delta V = V_{DC}$ results in $2V_{DC}$ at the generator terminal when a long cable is connected to the system. However, a multilevel converter topology can distribute the total voltage changes across multiple steps, where the overvoltage value depends on each step of voltage change.

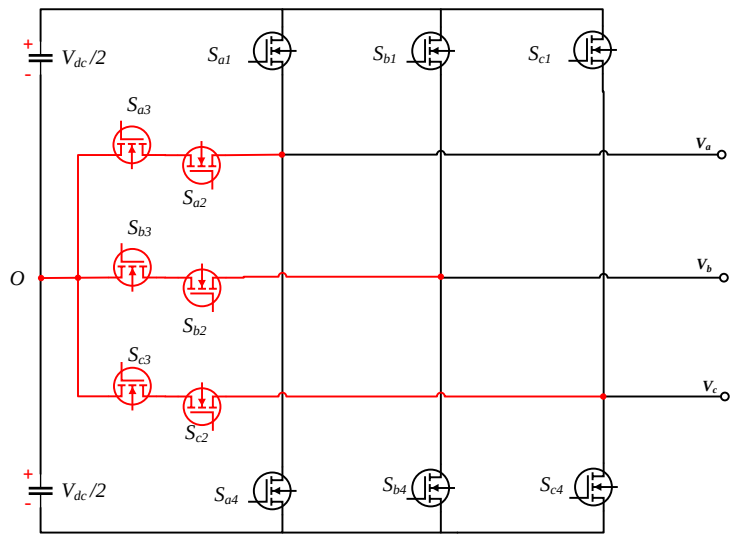


Figure 2.11: The three-level T type inverter topology.

Fig. 2.11 illustrates the three-level T-type inverter topology applied in [24] for investigating voltage overshoot compared with other strategies. A three-level inverter can output voltage pulses with each level at $V_{dc}/2$, which is then doubled at the motor terminal. Therefore, simulation and experimental results show that the voltage at the motor terminal is nearly 1.5 p.u., as opposed to 2.0 p.u. with the traditional two-level inverter topology [24].

Fig. 2.12 the 5-level diode-clamped inverter topology demonstrated in [25], aimed at eliminating common mode voltage and reducing dv/dt in induction motor drives. With this topology, the voltage level is $V_{dc}/4$, which is even smaller than the three-level T-type inverter. Comparisons of experimental results in terms of dv/dt from two-level and five-level inverters have been presented in [25], showing that the maximum dv/dt can exceed 2.0 $kV/\mu s$ for the two-level inverter, while it is approximately 0.5 $kV/\mu s$ for the five-level inverter. This presents around a 75% mitigation of dv/dt with the 5-level inverter topology. The overvoltage can be calculated as a value of 1.25 p.u. with the five-level inverter topology. Multilevel inverter design also brings other advantages

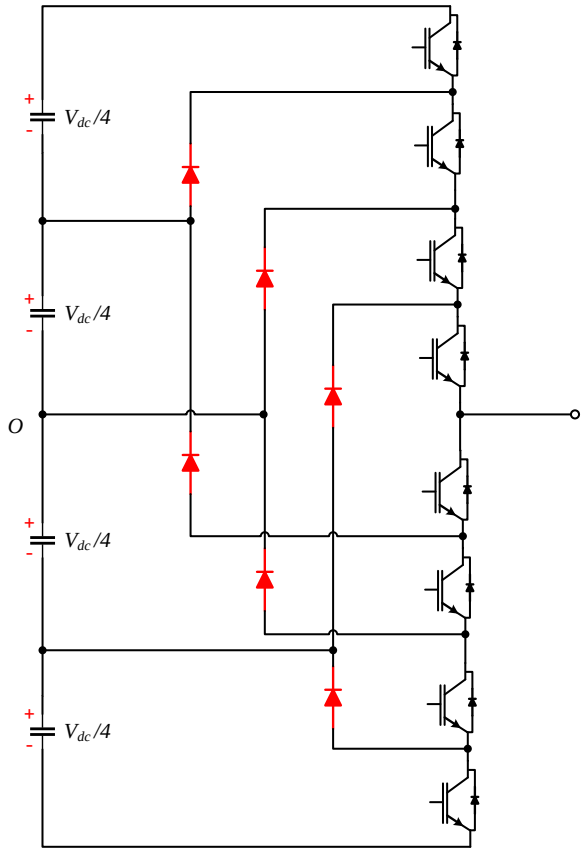


Figure 2.12: The five-level diode clamped inverter topology.

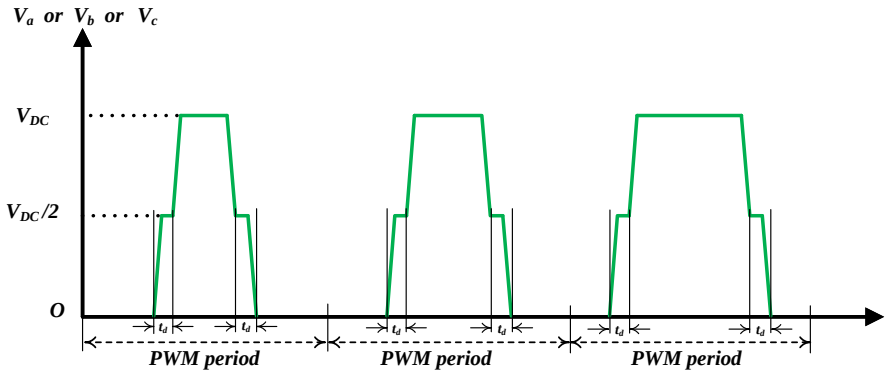


Figure 2.13: PWM voltage pattern having $V_{DC}/2$ level at each pulse transition [26].

such as lower leakage current and Total Harmonic Distortion (THD). However, these types of topologies are more complicated regarding hardware design and switching sequence control.

2.3 Active PWM Control Solutions

The aforementioned two main types of solutions are based on the theories of surge impedance matching and reducing dv/dt. Implementing these solutions inevitably requires the incorporation of additional passive components and even more complicated control methods. On the other hand, active PWM control solutions are rooted in the voltage reflection principle. By breaking the voltage pulse rising/falling edge from two steps to three steps, the overall combined voltage at the motor side approaches 1.0 p.u. The dwell time of the middle step needs to be accurately calculated.

2.3.1 3-Voltage-Step PWM Scheme

As shown in Fig. 2.13, the voltage rising/falling edge has been divided from 2 levels to 3 levels. This voltage pulse can be generated by a 3-level T-type inverter with a unipolar PWM strategy. It's worth noting that even though the converter topology is the same, the output voltage pulses will differ when applying different PWM strategies.

Fig. 2.14 presents the principle of how this 3-voltage-step PWM scheme can result in nearly zero voltage overshoot at the electric motor terminal. In (a) and (b), the first and second voltage pulses are shown, output from the inverter and transmitted to the motor terminal. In (c), the resulting and combined voltage pulse output from the inverter and transmitted to the motor side is illustrated. It can be observed that since there is a time period t_d between two generated pulses from the inverter, the resulting final voltage waveform at the motor side has almost zero overshoot. This method intelligently utilizes the voltage reflection theory and PWM strategy to avoid the severe 2 times of V_{DC}, achieving nearly 1.0 p.u. of V_{DC}.

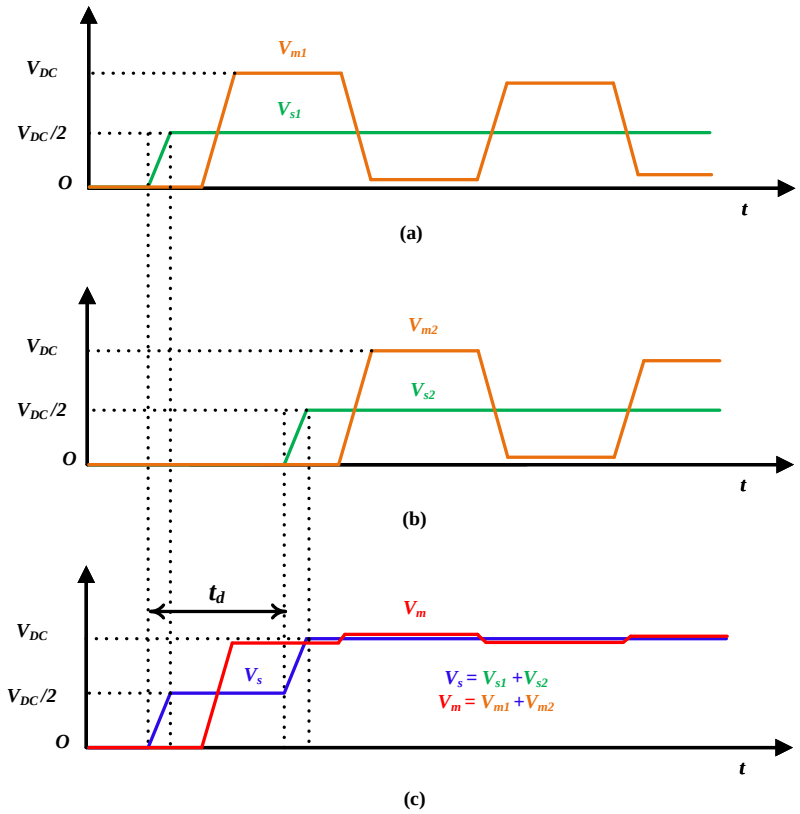


Figure 2.14: The voltage pulse at the inverter and motor terminals [27].

The time period t_d between two voltage steps needs to be accurately defined as $t_d = 2t_p$ to obtain the expected voltage waveform at the motor terminal. Furthermore, this 3-voltage-step PWM scheme can be obtained not only by the 3-level T-type topology with unipolar PWM strategy but also by the H-bridge inverter [28]. A single-phase H-bridge voltage source inverter with a characterized PWM generation strategy is shown in [28]. Two identical triangle carriers separated with t_d are used to compare with the sine wave to generate the required PWM signal. The experimental results showed that with this method, the voltage at the motor terminal is 1.08 p.u. at the rising transition and 1.05 p.u. at the falling transition [28]. The limitation of the H-bridge topology is that only single-phase applications were discussed in the literature.

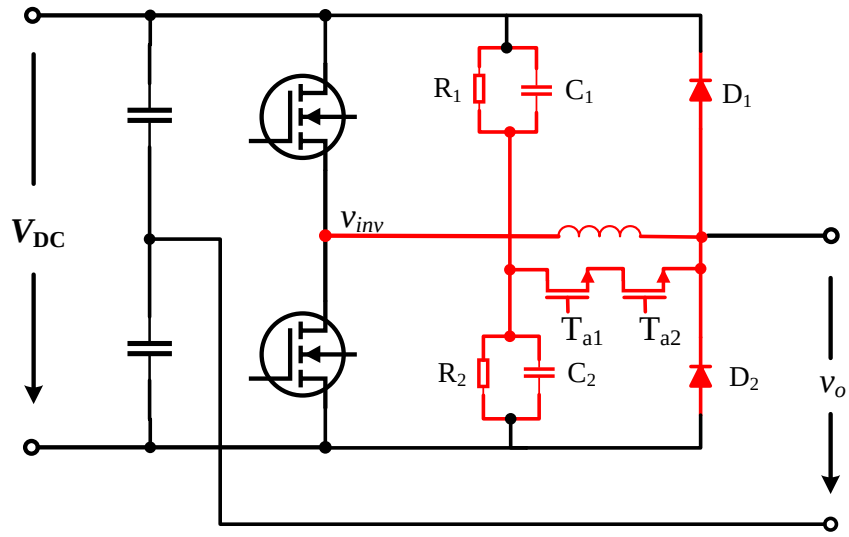


Figure 2.15: Active reflected wave canceller circuit topology [29].

In contrast to the above-mentioned methods that modify the PWM strategy to generate 3-voltage-step voltage pulses, Fig. 2.15 shows another approach that adds an additional circuit to achieve the same goal. This circuit is entitled with Active Reflected Wave Canceller (ARWC), and the detailed operating principle is stated in [29]. The proposed ARWC has been verified to achieve a 75% reduction in overvoltage with simple control, low loss, low cost, and compact features [29].

2.3.2 PWM Scheme with n Voltage Steps

The 3-voltage-steps PWM scheme can be further extended to 5 or even n smaller steps, as shown in Fig. 2.16. The operational principles are similar to the 3-voltage-step PWM scheme. The single-phase schematic of the converter, capable of generating n voltage steps pulse, is depicted in Fig. 2.17 [30]. It is composed of n cells per arm (here shown as half-bridge), and two arms constitute a leg of the three-phase converter [30]. The dwell time, dv/dt, and steps n can be defined as Equation (2.16), and each

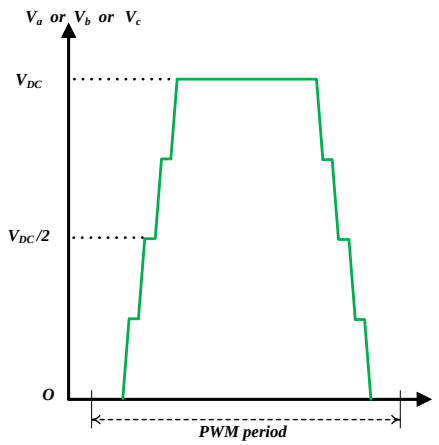


Figure 2.16: Multi-steps PWM scheme [30].

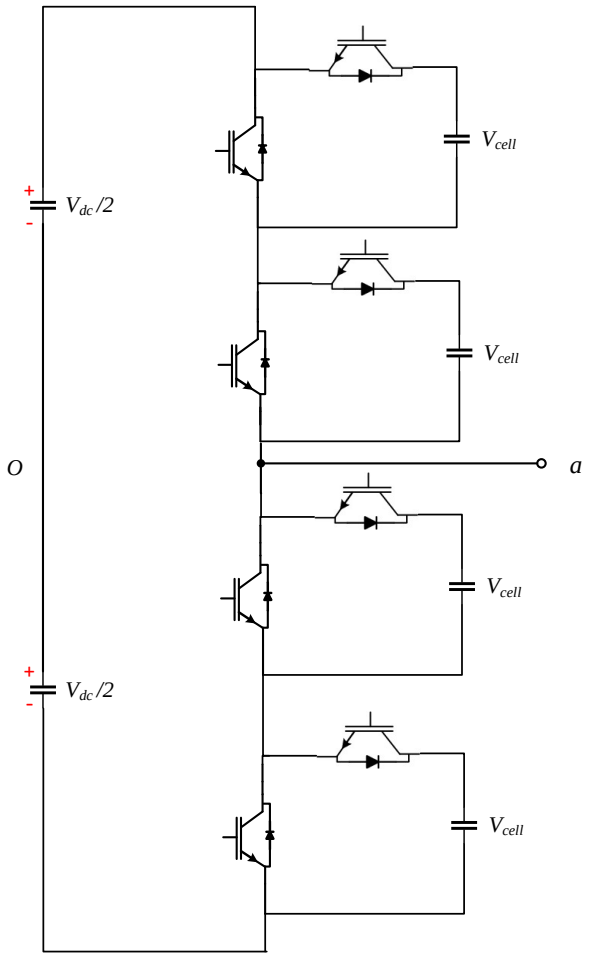


Figure 2.17: Single phase schematics of a multi-voltage steps converter [30].

step voltage can be given as Equation (2.17) [30].

$$t_d = \frac{1}{dv/dt} * \frac{1}{n+1} \tag{2.16}$$

$$V_{step} = \frac{V_{DC}}{n} \tag{2.17}$$

The simulation comparisons of 5L-ANPC and eight-cell converters have been conducted in [30], revealing that the 8-cell converter has lower requirements for converter and filter capacitors given a specific overvoltage limitation. However, the weighted total harmonic distortion (WTHD) and losses of the eight-cell converter are higher than those of the 5L-ANPC converter.

2.4 Integrated Machine-Drive Solutions

As mentioned earlier, the cable connected between the motor and inverter is one of the reasons causing the voltage reflection phenomenon. Canceling the cable connection is the most effective way to avoid the overvoltage issue. Integrated machine drive design is widely implemented, especially in the electric vehicle application scenario. This compact design offers many benefits, such as improved space efficiency, power density, and thermal management, among others.

The 5th generation of PMW e-drive unit design integrates the motor, inverter, and gearbox as a whole assembly. In this design, the motor and inverter are connected directly by a very short length of copper bar. Lucid Air integrated electric motor, inverter, and transmission drive unit, which is also a compact design without long cable connections. It can output power up to 670 hp with a complete assembly weight of 74 kg. Both of these designs position the high-power inverter directly over the electric motor, avoiding the need for long cable connections.

Tesla Model S rear motor drive assembly is composed of an electric motor, power inverter, and gearbox. The left component with the DC high-voltage cable is the power inverter, integrated not over the inverter but in the longitudinal direction. Tesla Model S rear motor drive unit has a different design compared to BMW and Lucid Air, but all of them are compact, space-efficient, and avoid cable connections between the motor and inverter.

Chapter 3 High-Frequency Modeling of Wind-Turbine Generator-Converter Systems

The high-frequency modeling of wind-turbine generator-converter systems is necessary to simulate the transient surge overvoltage phenomenon. In this chapter, existing high-frequency models for electric machines and power cables are thoroughly reviewed. Considering both accuracy and complexity, appropriate high-frequency models for electric machines and power cables are selected and modeled. The active SPWM control strategy is applied to the power converter for generating high-frequency pulses. The SiC power MOSFET C2M0045170D with a gate resistor is modeled for the power converter.

3.1 High-Frequency Modeling of Electric Machines

High-frequency modeling of electric machines is essential for investigating the surge overvoltage phenomenon at machine terminals. Thorough research on this topic has been conducted by researchers, and three main typical types of models have been reviewed in this section. A tapped generator is chosen as the object, and its coil impedance is measured over a wide frequency range (10Hz-8MHz) to facilitate high-frequency modeling of each coil.

3.1.1 Review of the Existing High-Frequency Model

Type I: per phase model

The researchers initially focused on studying the differential mode (DM) voltage at the terminal of the electric machine, commonly referred to as phase-to-phase voltage.

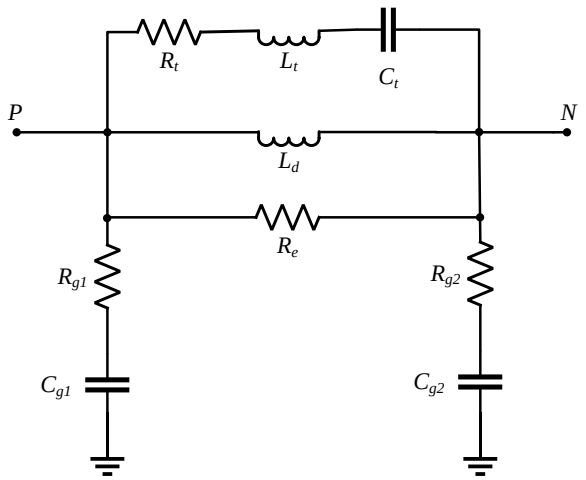


Figure 3.1: High-frequency model of electric machines (per phase).

Consequently, the per-phase electric machine model was well established. The per-phase equivalent circuit depicted in Fig. 3.1 was proposed and utilized in [31].

In this circuit, each parameter holds its physical meaning and significance. R_{g1} and C_{g1} represent the parasitic resistance and capacitance between stator winding and the machine frame; R_{g2} and C_{g2} represent the parasitic resistance and capacitance between the stator neutral and the machine frame; L_d represents the stator winding leakage inductance; R_e represents the high-frequency iron loss of the stator winding; L_t and C_t are represent the skin effect and inter-turn capacitance of the stator windings[31]. The method for extracting these parameters is illustrated in [32]. The simulated phase-to-phase overvoltage waveform from this circuit model aligns well with the measured waveform from the test. While the per-phase model is sufficient for inspecting line-to-line overvoltage, it is unable to further explore the voltage on each coil.

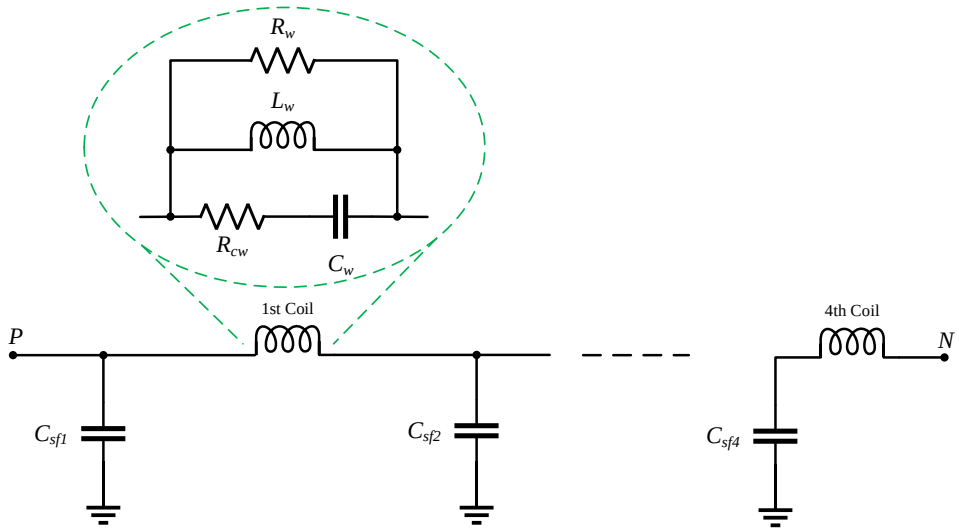
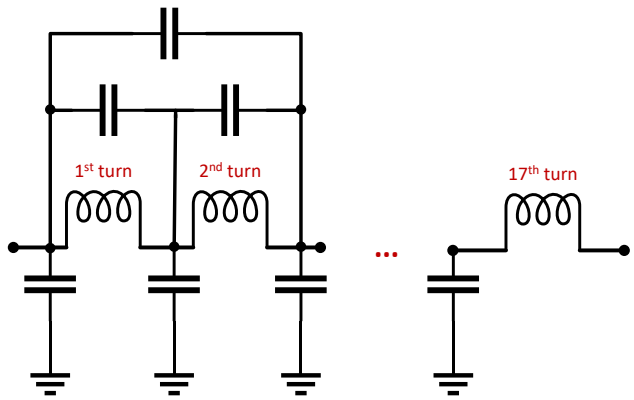


Figure 3.2: High-frequency model of electric machines (per coil per phase).

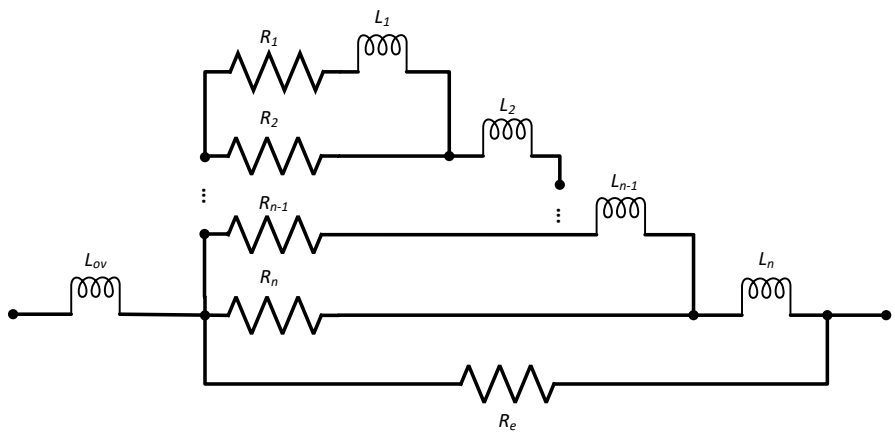
Type II: per coil model

To delve deeper into the overvoltage distribution mechanism on each coil, it is necessary to model each coil individually. This approach enhances the overall accuracy of the electric machine model for studying the high-frequency responses of the stator windings. The high-frequency per-coil model is proposed in [33], as illustrated in Fig. 3.2. In this model, the motor comprises four coils per phase, and each coil has been meticulously modeled.

The presence of stray capacitance C_f between the stator coil and the machine frame is crucial for illustrating the uneven distribution of overvoltage across different coils. Assuming that each coil is identical and has the same impedance, the equations provided in 3.1[33]can be used to estimate the uneven distribution of overvoltage. This circuit not only demonstrates phase-to-phase overvoltage but also presents the



(a) Per coil model



(b) Per turn model

Figure 3.3: High-frequency model of electric machines (per turn per coil).

voltage uneven distribution across different coils.

$$\begin{cases} V_{c1} = Z_w \left(I_{sf2} + I_{sf3} + I_{sf4} + I_{nf}\right) \\ V_{c2} = Z_w \left(I_{sf3} + I_{sf4} + I_{nf}\right) \\ V_{c3} = Z_w \left(I_{sf4} + I_{nf}\right) \\ V_{c3} = Z_w \left(I_{nf}\right) \end{cases} \tag{3.1}$$

Type III: per turn model

The researchers conducted further investigations into modeling each turn within each coil, considering turn-to-turn and turn-to-ground parasitic capacitance. In [34],

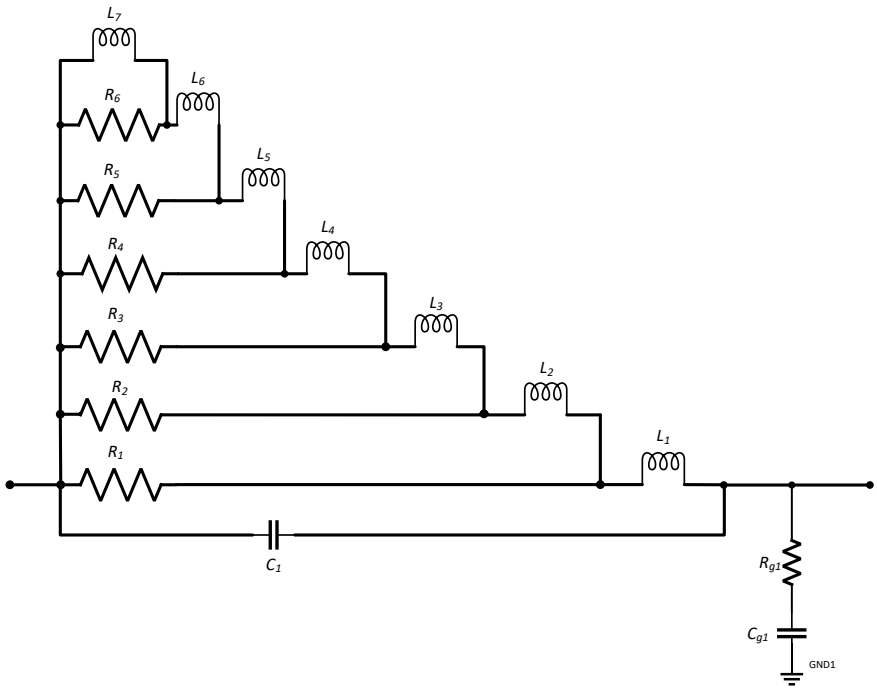


Figure 3.4: Proposed high-frequency per coil equivalent circuit of the generator

a 4-pole 7.5 kW squirrel cage induction machine with random-wound round wire winding was utilized for high-frequency modeling. Fig. 3.3a depicts the per-coil model, which comprises 17 turns, and the parasitic capacitors between turn-to-turn and turn-to-ground are determined using finite element methods. Each turn's model can be further represented by an RL ladder circuit, as shown in Fig. 3.3b, with the laminated iron core effects accounted for by an eddy current loss resistance R_e. The parameters of the RL ladder circuit are extracted via FEM calculation. This model's advantage lies in the ability to observe not only different coil voltages but also to further study each turn's voltage in simulation. Moreover, the overall three-phase machine model becomes more accurate with the inclusion of additional parameters. In [35], a similar circuit topology is applied for a 2.5 MW turbine generator with hairpin windings.

Proposed equivalent circuit per coil over high-frequency

To model each turn for each coil, it is necessary to have access to the terminals of each turn within a coil for impedance measurement. However, the generator used for modeling and impedance measurements in this thesis only has accessible taps for each coil. In [36], the effect of winding parameters on surge voltage propagation is thoroughly analyzed. Based on the simulation and experimental test results in [36], it has been demonstrated that self-capacitance and inductance are the primary parameters influencing the propagation pattern of winding surge voltage. The mutual capacitance between strands, on the other hand, plays a minor role in modeling accuracy and can be considered negligible [36].

Based on the aforementioned reviews of high-frequency machine models, taking into account both the primary parameters and frequency-dependent parameters, the proposed equivalent circuit for each coil is depicted in Fig. 3.4. The RL ladder circuit is incorporated into the model to account for variations in coil inductance with frequency.

3.1.2 High-Frequency Parametric Measurement

The generator utilized in this thesis is a 5-kW, 240-V, four-pole revolving field three-phase synchronous generator with taps for each coil of each phase [37], as shown in Fig. 3.5. Each phase comprises 6 coils connected in parallel(12 coils per phase). Specifically, coils 1 to 6 of one branch extend from terminals L2 to T21, T21 to T23, T23 to T25, T25 to T27, T27 to T29, and T29 to L5, respectively. The impedance of each of these coils is measured separately for high-frequency modeling. However, the taps from T16 to T20 represent 5%, 10%, 21%, 42%, and 68% of one coil's length, respectively, and therefore cannot be utilized for measuring the impedance of each

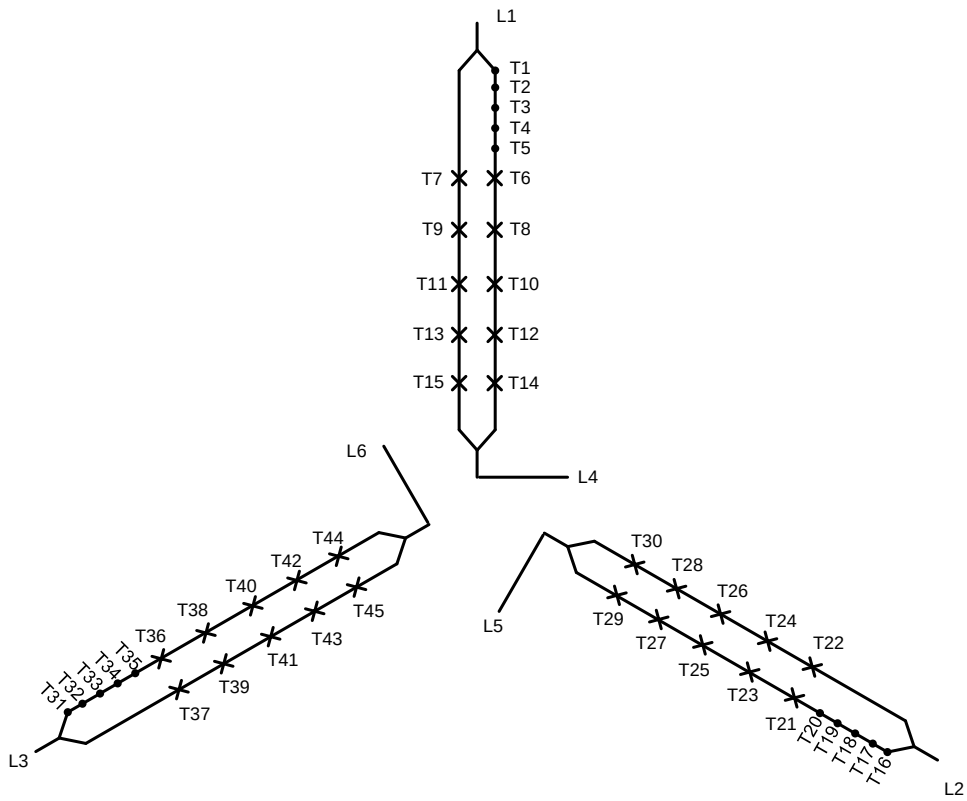


Figure 3.5: Experimental generator with taps for each coil

turn.

To measure the impedance of the coil across a wide range of frequencies, the HIOKI LCR meter IM3536 has been utilized, as depicted in Fig. 3.6. This device offers a frequency measurement range typically spanning from 4 Hz to 8 MHz, although this range may vary based on the impedance value being measured. The aforementioned 5-kW generator is shown in Fig. 3.7.

The impedance measurement results of the aforementioned 6 coils are illustrated in Fig. 3.8, where the first and sixth coils exhibit greater differences compared to the others. This variation may be attributed to the inclusion of extra wires during the impedance measurement process. As depicted in Fig. 3.5, the impedance of Coil-1 is measured from terminals L2 to T21, while the impedance of Coil-6 is measured from

Figure 3.6: The HIOKI LCR meter IM3536

Figure 3.7: The tapped generator used for high-frequency modeling

terminal T29 to L5. To maintain consistency, the impedance measurement data of Coil-4 is selected for high-frequency circuit matching for each coil.

The methodology for extracting the parameters of the equivalent high-frequency coil circuit is based on impedance matching across a wide frequency range. The high-frequency coil circuit can be conceptualized as a transfer function that describes the output voltage in response to an input. Since the coil impedance varies with frequency, the equivalent circuit must be capable of expressing its frequency-dependent

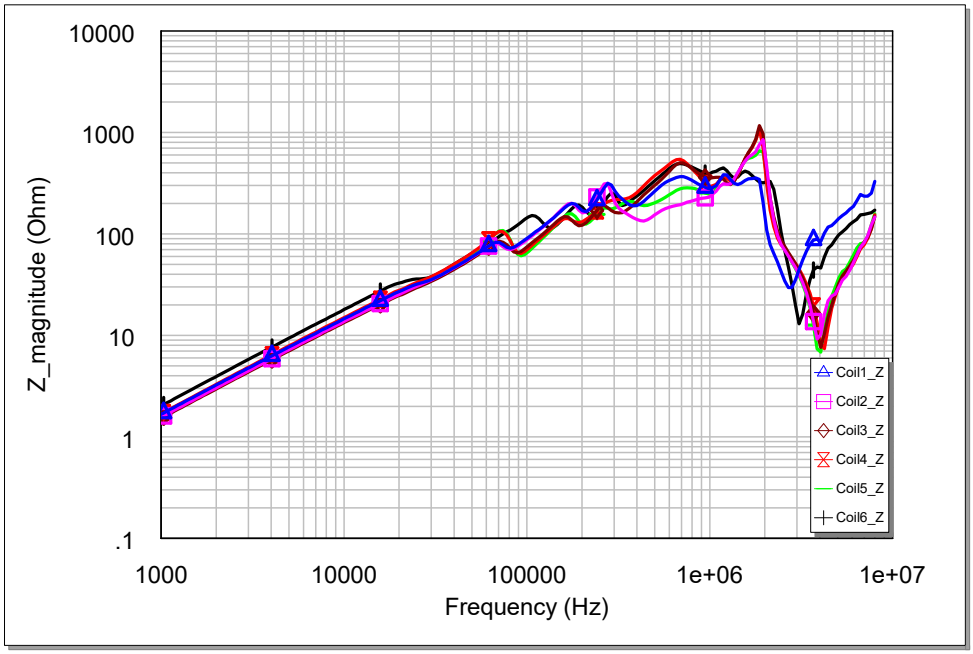


Figure 3.8: 6 coils impedance measurement data of experimental generator

Table 3.1: The matched parameters of the proposed high-frequency per coil model.

R (Ω) and C (F)		Inductance (H)	
R1	387.37	L1	6.03e-10
R2	35.16	L2	1.41e-4
R3	2163.05	L3	2.93e-05
R4	1619.28	L4	5.15e-05
R5	1.89	L5	9.40e-07
R6	0.25	L6	4.19e-05
C1	1e-12	L7	9.9e-4

characteristics. Therefore, to model this feature for each coil, the coil impedance measured over a wide frequency range serves as the target for the matching process.

The impedance matching process is conducted using the AWR Design Environment software. A proposed coil circuit, comprising resistors, capacitors, and inductors, is constructed in this software, incorporating the parameters to be optimized. The optimization procedure utilizes the built-in optimization tool Robust Simplex, aiming to achieve the objective of closely aligning the impedance of the coil circuit

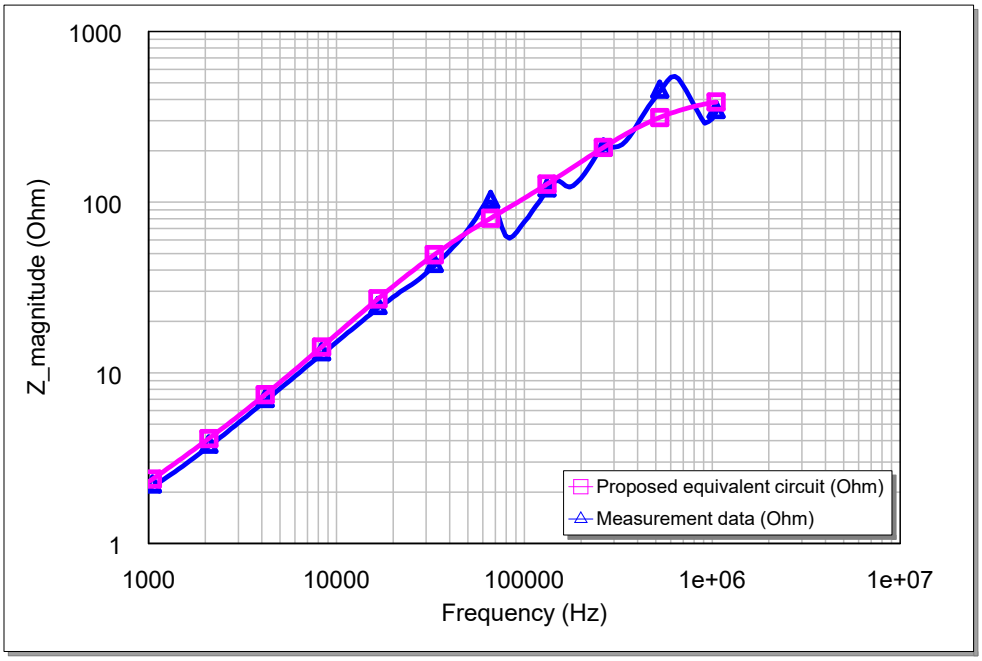


Figure 3.9: Proposed equivalent circuit impedance matched with the measurement data.

Table 3.2: The coils to ground resistance and capacitance.

Resistance (Ω)		Capacitance (pF)	
R_{g1}	143	C_{g1}	455
R_{g2}	443	C_{g2}	230
R_{g3}	445	C_{g3}	213
R_{g4}	336	C_{g4}	260
R_{g5}	423	C_{g5}	233
R_{g6}	403	C_{g6}	199

with the measured data across a wide frequency range.

The impedance matching results are depicted in Fig. 3.9, where the blue waveform represents the measurement data and the pink waveform illustrates the impedance of the proposed coil circuit with optimized parameters. It is evident that the proposed equivalent coil model with matched parameters accurately captures the real impedance of the coil across a wide frequency range. The extracted parameters for the proposed high-frequency per coil model are presented in Table. 3.1. Additionally,

the resistances and capacitances of the coils to ground are measured at a frequency of 1.6 MHz, which is close to the anti-resonant frequency of the generator-cable DM impedance. These values are provided in Table 3.2. The accuracy of the high-frequency coil model can be further validated through the system simulation results presented in Chapter 5.

3.2 High-Frequency Modeling of Power Converters

The power converter employed in the generator-converter system in this thesis is actively controlled, allowing for adjustable parameters such as modulation index, switching frequency, and gate resistance of the switching devices, as shown in Fig. 3.10. By varying the gate resistance of the switching devices, the rise time of the line-to-line voltage can be altered, facilitating investigation into the mechanism of overvoltage changes. The SPWM control strategy is implemented to operate at different switching frequencies and modulation indices.

The switching devices utilized in the power converter are SiC power MOSFETs developed by Wolfspeed. The parameters of the SiC power MOSFET C2M0045170D are detailed in Table. 3.3. SiC MOSFETs are widely used in power electronics due to their superior properties compared to silicon-based devices, such as higher breakdown voltage, lower on-resistance, and the ability to operate at higher temperatures and frequencies.

When a SiC MOSFET switches from the off state to the on state (or vice versa), the voltage across the device changes rapidly. The speed of this voltage change is characterized by dv/dt, the rate of change of voltage over time. High dv/dt values are particularly notable during the turn-off event. This can be broken down into stages as follows: (1) Turn-off initiation: When the gate voltage decreases below

Table 3.3: The parameters of SiC switching device C2M0045170D.

Symbol	Parameter	Value	Unit	Test Conditions
V_{DSmax}	Drain-Source Voltage	1700	V	$V_{GS} = 0V, I_D = 100\mu A$
V_{GSop}	Gate-Source Voltage	-5/+20	V	Recommended operational values
I_D	Continuous Drain Current	75	A	$V_{GS} = 20V, T_C = 25°C$
t_r	Rise Time	19	ns	$R_{G(ext)=2.5\Omega}$
t_f	Fall Time	19	ns	$R_{G(ext)=2.5\Omega}$

the threshold voltage, the MOSFET begins to turn off. The current through the device starts to reduce. (2) Voltage rise: As the current decreases, the drain-source voltage begins to increase. This voltage rise happens because the current through the device is dropping while it still needs to support the load current. The drain-source capacitance plays a crucial role here, it needs to be charged up to the supply voltage, leading to an increase in drain-source voltage. (3) Voltage ramp: The actual dv/dt ramp occurs during this phase where drain-source voltage transitions from a low value (close to zero when fully on) to a high value (close to the supply voltage when fully off). The dv/dt during this phase can be extremely high, often in the range of several V/ns (volts per nanosecond), depending on the gate drive strength and external circuit conditions.

3.3 High-Frequency Modeling of Power Cables

As discussed in Chapter 1, the impedance mismatch between the power cable and the electric machine is one of the primary factors contributing to overvoltage issues. Therefore, accurate modeling of the power cable is essential to represent the high-frequency characteristic impedance, which influences the magnitude and oscillation frequency of surge line-to-line overvoltage. In this section, various high-frequency models for power cables are comprehensively reviewed, and one model is selected for

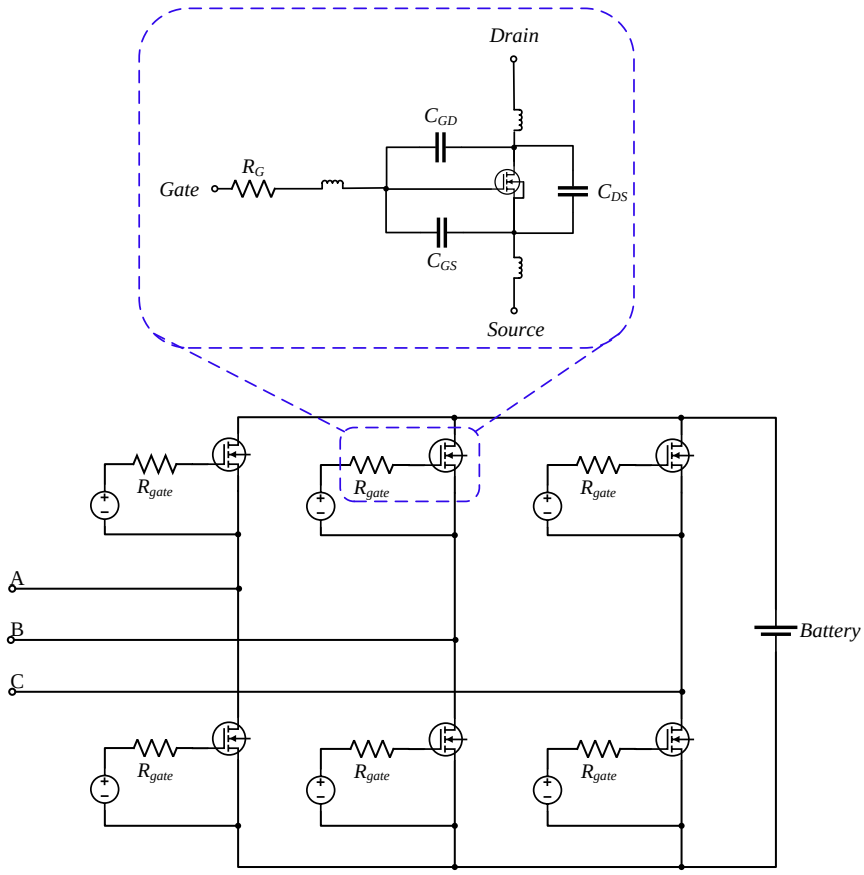


Figure 3.10: The power converter with SiC MOSFETs

implementation in the generator-converter system.

3.3.1 Review of Existing High-Frequency Models

Extensive research has been conducted on high-frequency power cables, spanning from simple transmission line circuits to more complex RL ladder and RC ladder circuits. The accuracy of these models improves as additional components are incorporated into the circuit.

Equivalent circuit of the transmission line

The transmission line model is widely utilized in power system simulation, with its equivalent circuit depicted in Fig. 3.11. Some researchers later adapted this model

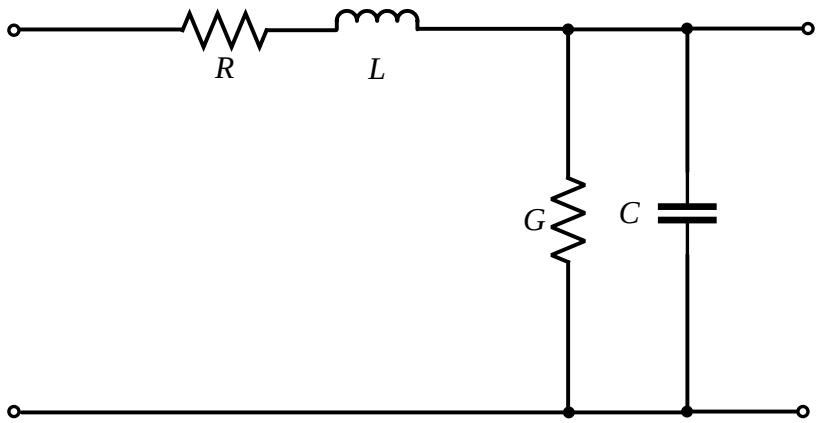


Figure 3.11: The equivalent circuit of the transmission line

as a per-unit model for long cables [38]. In this model, R, L, G, and C represent the resistance of the conductor, inductance of the conductor loop, shunt conductance, and capacitance between conductors, respectively. While this model offers simulation efficiency, its accuracy may not always be satisfactory.

The high-frequency cable model considering dielectric losses

Building upon the transmission line model, a high-frequency cable model that considers dielectric losses was proposed in [39], illustrated in Fig. 3.12. R_{p2} and C_{p2}, combined with R_{p1} and C_{p1}, more accurately represent dielectric losses. However, it should be noted that this model still does not account for skin and proximity effects.

The high-frequency cable model considering dielectric losses, skin and proximity effects

Further improvement is proposed in [40] to incorporate the high-frequency skin and proximity effects. These effects are addressed by introducing parallel-connected elements R_{s2} and L_{s2}, as shown in Fig. 3.13:

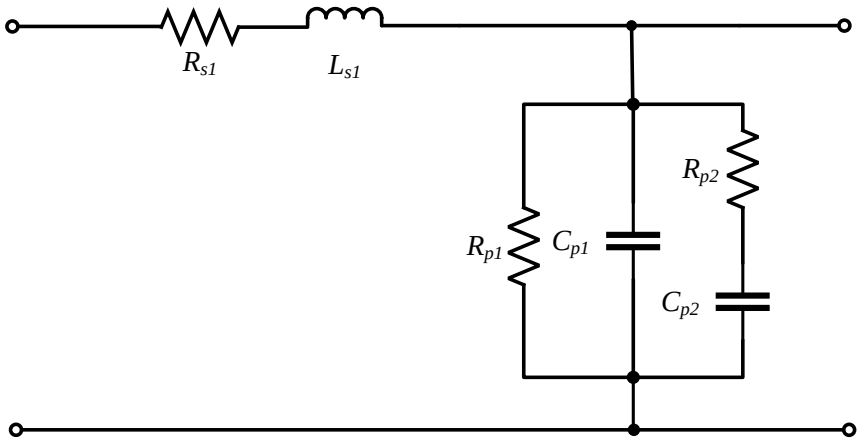


Figure 3.12: The high-frequency cable model considering dielectric losses

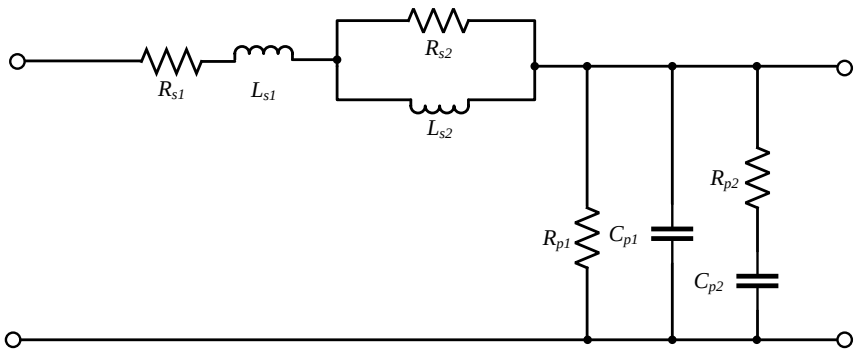


Figure 3.13: The high-frequency cable model considering dielectric losses, skin and proximity effects

The high-frequency cable model considering resonance and anti-resonance frequency

Additionally, to align the circuit's impedance resonance and anti-resonance frequency with the test results, ΔR_s and ΔR_p are introduced, as shown in Fig. 3.14. It is crucial to account for the anti-resonance frequency as it directly affects the oscillation frequency of the line-to-line voltage.

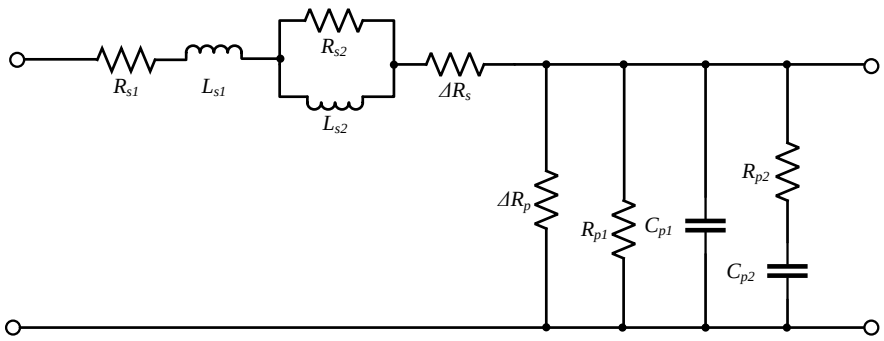


Figure 3.14: The high-frequency cable model considering resonance and anti-resonance frequency

The high-frequency cable model with the RL and RC ladder circuits

One disadvantage of the aforementioned cable models is that including more parameters complicates the extraction process, as it involves solving a larger set of equations. However, the RL ladder and RC ladder circuits proposed in [41] for high-frequency cable modeling have addressed this issue. These circuits account for skin effects, proximity effects, and dielectric losses, while parameter extraction can be facilitated by software with a substantial amount of test data. Consequently, this type of circuit not only ensures the accuracy of the model but also enhances the scientific rigor of the parameter extraction process. This is the rationale for selecting RL and RC ladder circuits for high-frequency cable modeling in the generator-converter system.

3.3.2 High-Frequency Parametric Measurement

Based on the review of existing high-frequency cable models, the one employing RL and RC ladder circuits is chosen due to its balance of accuracy and parameter extraction efficiency, as illustrated in Fig. 3.16. Specifically, a 12-AWG 4-conductor shielded motor supply cable has been selected for high-frequency parametric measure-

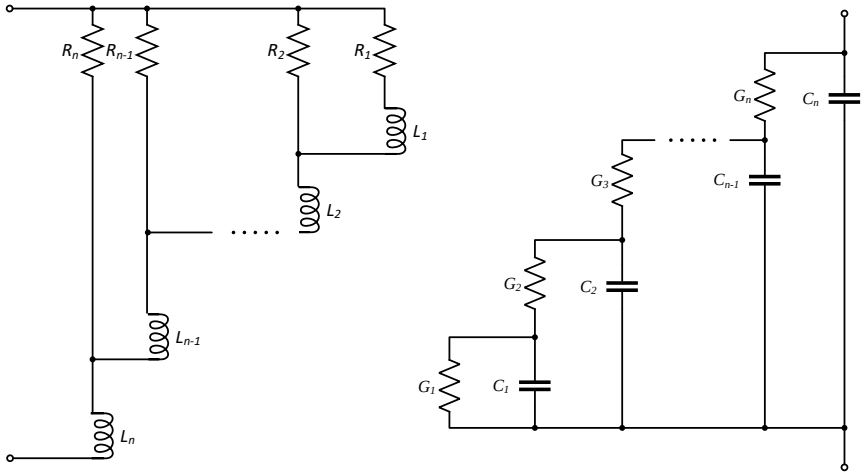


Figure 3.15: The high-frequency cable model with RL and RC ladder circuits

Table 3.4: The parameters of selected cable(29m).

Parameter	Value
AWG	12
# Conductors	4
Conductor material	Tinned Copper
Nom. Characteristic Impedance	71 Ohm
Nom. Inductance	$0.197\mu H/ft$
Nom. Capacitance Conductor to Conductor	26 pF/ft
Max. Operating Voltage	1000 V RMS
Max. Recommended Current	30 Amps per conductor @ 30°C

ment in this thesis. The basic parameters of the cable can be found in Table. 3.4, and a one-meter cable is depicted in Fig. 3.17. Similar to the coil impedance measurement, the HIOKI LCR meter IM3536 has been utilized for impedance measurement of the cable across a wide range of frequencies, as shown in Fig. 3.6.

The methodology for extracting the parameters of the RL and RC ladder circuit is based on impedance matching. Initially, the impedance of a one-meter cable across a wide frequency range is measured using the LCR meter. Subsequently, the RL ladder circuit, as depicted in Fig. 3.16, is constructed in the AWR Design Environment soft-

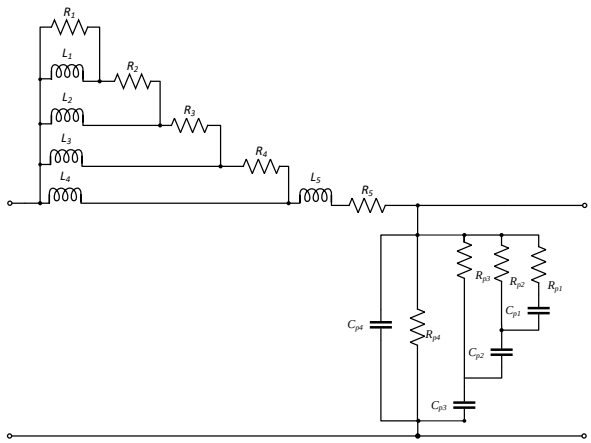


Figure 3.16: The high-frequency cable model chosen for generator-converter system

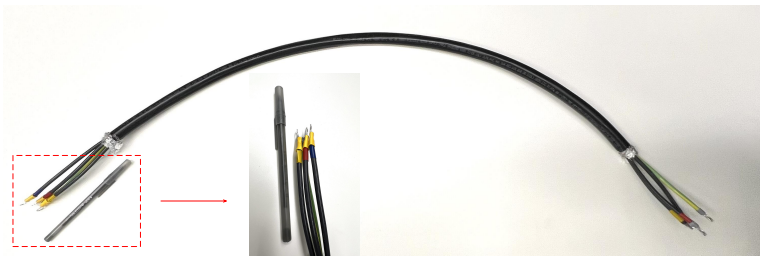


Figure 3.17: Power cables with 12-AWG and a length of 1-meter

ware, and the measured impedance data is imported into the software to generate the parameters for the RL ladder circuit. To ensure the extraction of precise parameters, the optimization method Robust Simplex is employed with 30,000 iterations. The optimization goals are set to achieve parameters Z_{diff} and $Phase_{diff}$ as close to 1 as possible. These parameters, defined in Equation 3.2, indicate better matching when they are closer to 1.

$$\begin{cases} Z_{diff} = abs\left(Z_{measurement}/Z_{RLladder}\right) \\ Phase_{diff} = abs\left(Phase_{measurement}/Phase_{RLladder}\right) \end{cases} \tag{3.2}$$

The magnitude and phase matching of the one-meter cable impedance is depicted in Fig. 3.18 and Fig. 3.19, respectively. The optimization results for magnitude and phase are constrained between 0.985 and 1.01, indicating a matching error of less

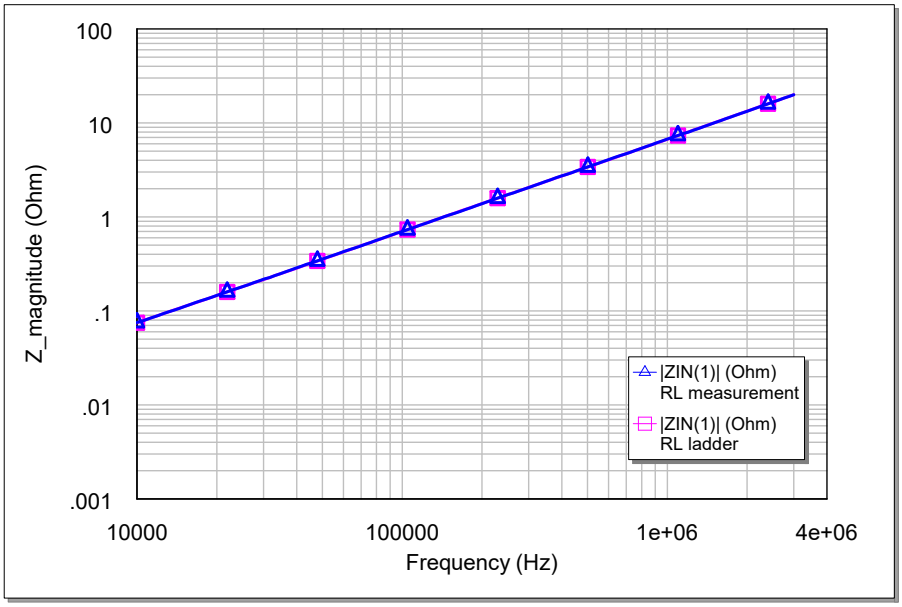


Figure 3.18: The matching of the impedance magnitude

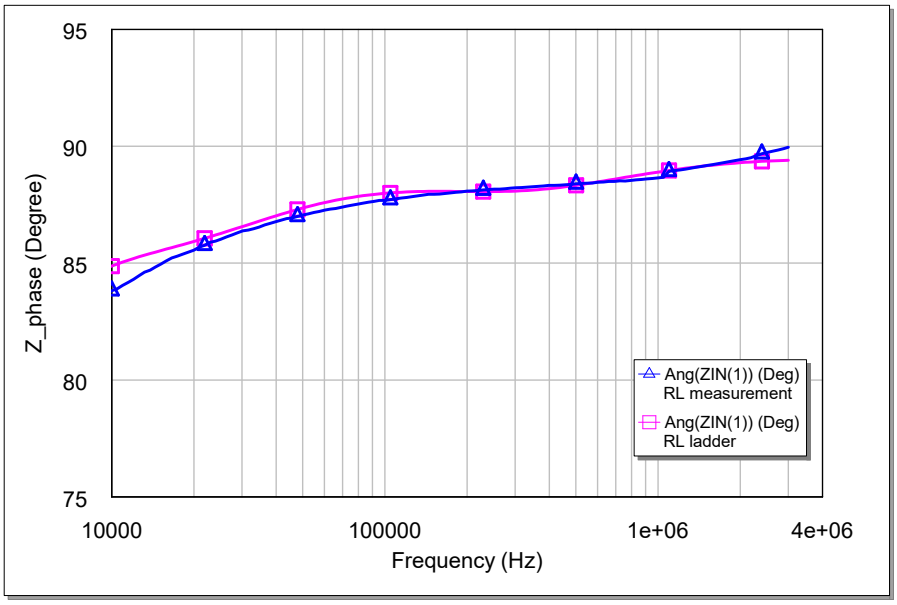


Figure 3.19: The matching of the impedance magnitude

than 1.5%, as illustrated in Fig. 3.20. The RL ladder circuit parameters extracted from this optimization process are presented in Table. 3.5.

The extraction of RC ladder circuit parameters follows a similar procedure to that for the RL ladder circuit. However, the RC ladder circuit represents the effects be-

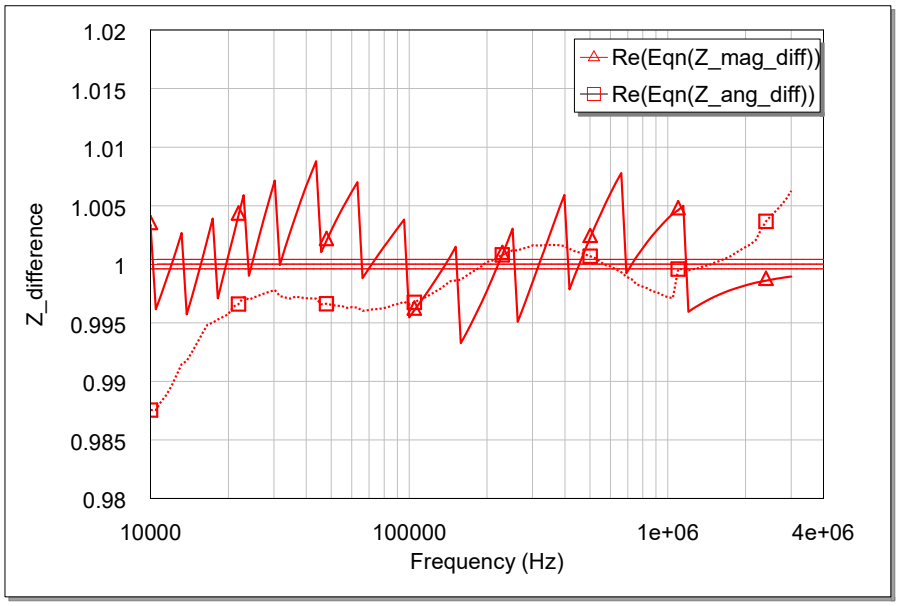


Figure 3.20: The ratio of impedance from the lab measurement and RL ladder circuit

Table 3.5: The parameters of RL ladder circuit.

Resistance (Ω)		Inductance (H)	
R1	5000	L1	2.30e-5
R2	48.50	L2	1.46e-5
R3	1.37	L3	1.00e-4
R4	0.56	L4	1.21e-6
R5	4.19e-3	L5	2.72e-9

tween two conductors. Therefore, open circuit impedance measurement between two conductors is conducted for the matching and optimization process. The matching results of impedance magnitude and phase are depicted in Fig. 3.21 and Fig. 3.22, respectively. The impedance difference between the measurement data and RC ladder circuit can be observed in Fig. 3.23. The extracted RC ladder circuit parameters are presented in Table. 3.6.

The matching process described above is based on impedance measurement data from a one-meter cable. The extracted cable parameters are then used for simulations with cables of different lengths by simply scaling them up. However, the impedance

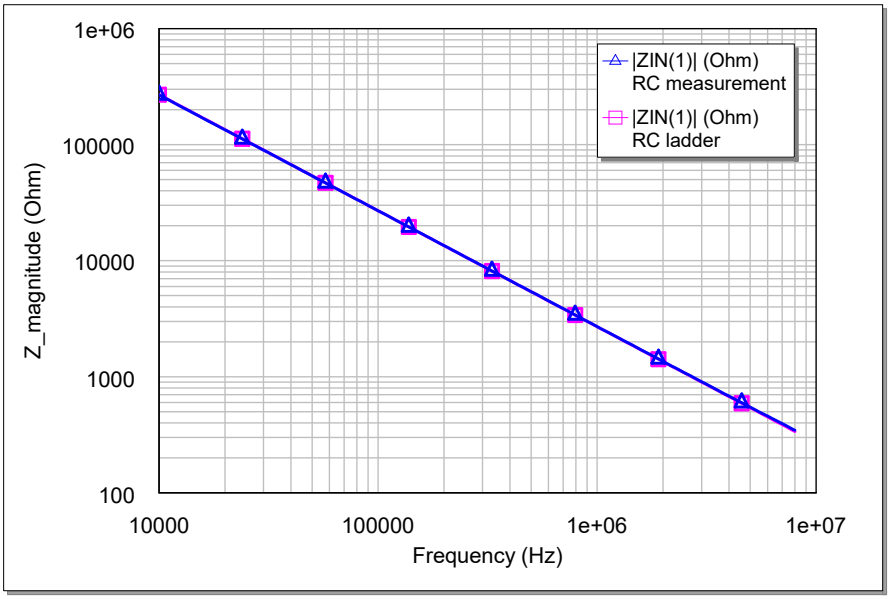


Figure 3.21: The matching of the impedance magnitude for RC ladder circuit

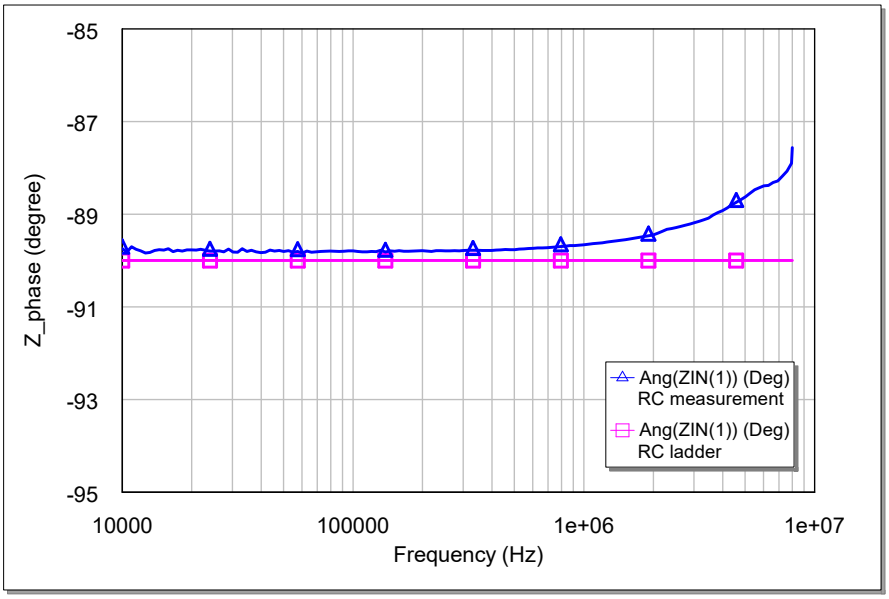


Figure 3.22: The matching of the impedance phase for RC ladder circuit

of the cable does not precisely follow a linear relationship with cable length. Consequently, errors may accumulate, particularly with longer cables.

To enhance the accuracy of the one-meter cable model for representing longer cables, a 29-meter cable is utilized to correct a portion of the parameters of the one-

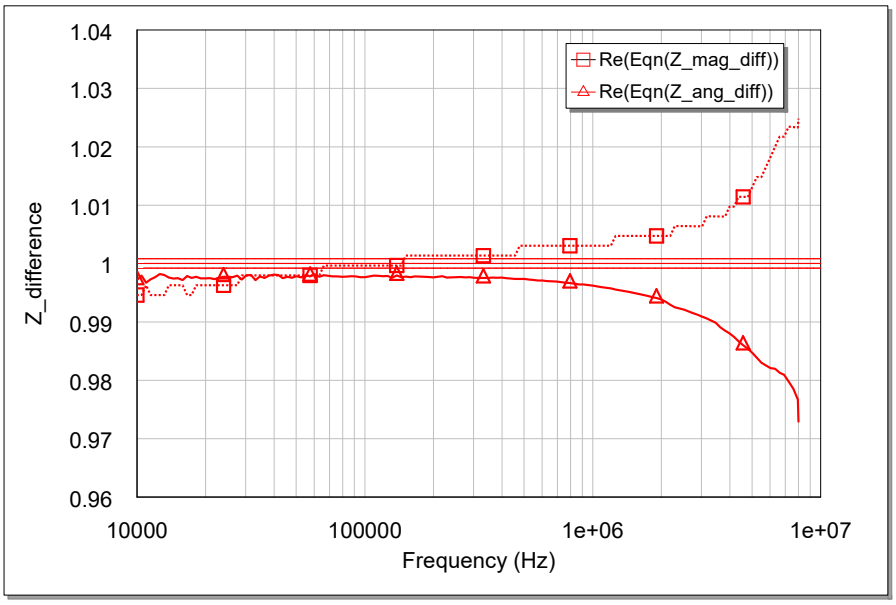


Figure 3.23: The ratio of impedance from measurement and RC ladder circuit

Table 3.6: The parameters of RC ladder circuit.

Resistance (Ω)		Capacitance (F)	
R_{p1}	8.31e+18	C_{p1}	0.98e-3
R_{p2}	2.69e+19	C_{p2}	0.41e-3
R_{p3}	3.74e+19	C_{p3}	0.06e-9
R_{p4}	2.31e+19	C_{p4}	0.06e-9

meter cable. The open circuit and short circuit impedance of the 29-meter cable in both differential mode and common mode are measured. This data is then used to optimize a portion of the one-meter cable parameters by matching the cable model's impedance with the measurement data, focusing on the anti-resonant frequency and the impedance at this frequency.

Fig. 3.24 and 3.25 illustrate the matching results of the 29-meter cable model with optimized parameters and the measurement data in terms of the short circuit and open circuit in differential mode. Similarly, Fig. 3.26 and 3.27 depict the matching results in terms of short circuit and open circuit in common mode. The critical matching point is the lowest impedance, typically around 1.579 MHz, as at this fre-

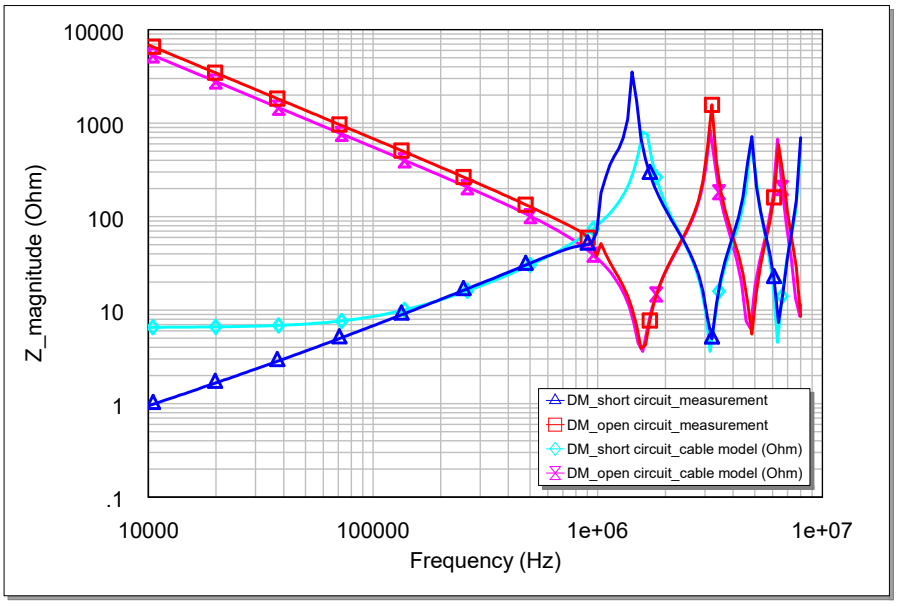


Figure 3.24: The magnitude matching of the short-circuit and open-circuit impedance in differential mode.

Table 3.7: The optimized cable parameters

Parameters	Value
R_5	0.15
L_4	0.2e-6
C_{p4}	0.037e-11

quency, the reflection coefficient between the cable and motor is maximum, resulting in surge overvoltage. This anti-resonant frequency should also align with the line-to-line surge overvoltage oscillation frequency. The optimized parameters are presented in Table. 3.7. The cable CM and DM impedance measurements are shown in Fig. 3.28 and Fig. 3.29, respectively. Opening the connection between conductor C and G allows for the measurement of open circuit and short circuit impedance for the common mode. Similarly, by opening the connection between conductor B and C, measurements for open circuit and short circuit impedance for differential mode can be obtained.

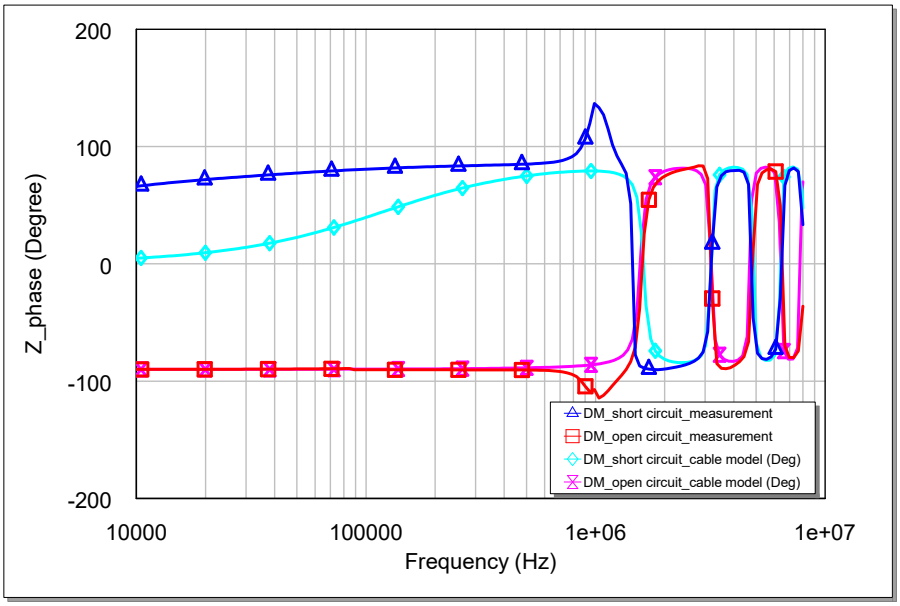


Figure 3.25: The phase angle matching of the short circuit and open circuit impedance in differential mode

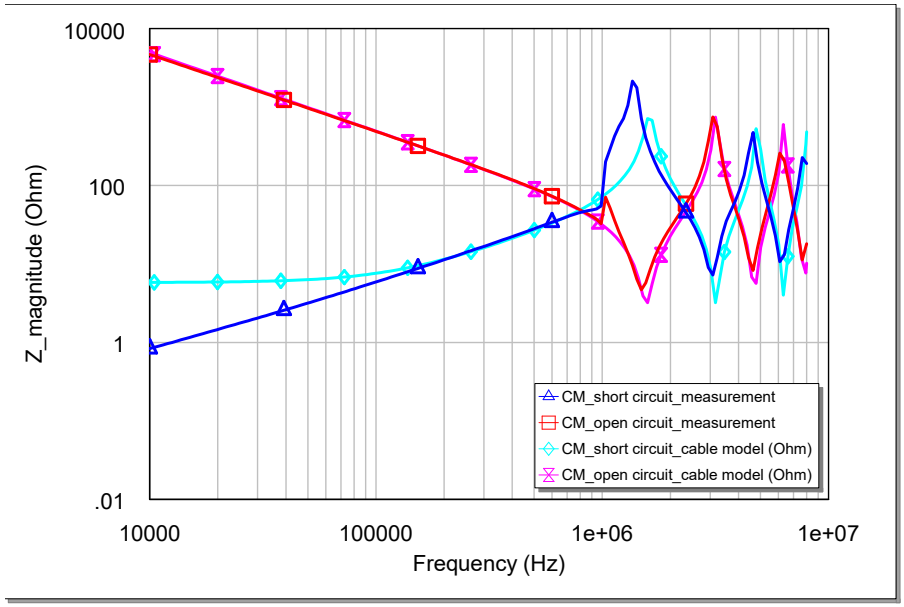


Figure 3.26: The magnitude matching of the short circuit and open circuit impedance in common mode

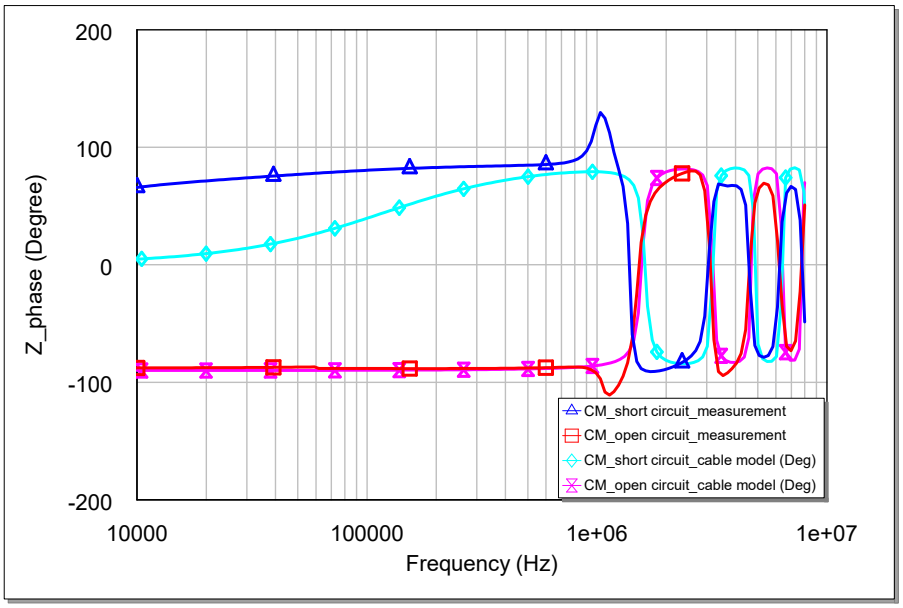


Figure 3.27: The phase angle matching of the short circuit and open circuit impedance in common mode

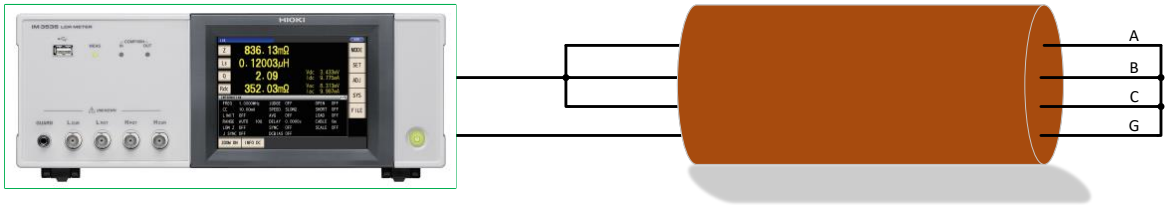


Figure 3.28: The cable common-mode impedance measurement

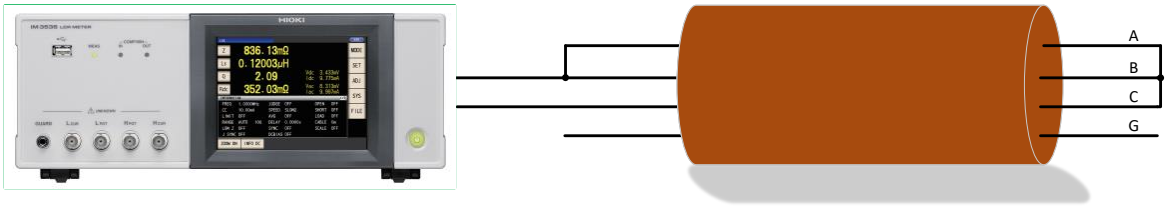


Figure 3.29: The cable DM impedance measurement

Chapter 4 Proposed Smart Coil Solution

The uneven distributions of reflected high-frequency surge voltage on different coils are observed both in tests and simulations [42], as shown in Fig. 5.2 in next Chapter. The proposed smart coil solution is specifically designed to mitigate the surge voltage stress for the first few coils of the generator. Unlike other solutions, the smart coil circuit features fewer components, resulting in a smaller size that can conveniently be installed in the junction box of the generator. This section will delve into the operating principle, control strategy, and parametric sizing of the smart coil circuit.

4.1 Operating Principle of the Smart Coil Concept

The proposed smart coil topology, depicted in Fig. 4.1 when added to the first coil, primarily comprises two capacitors, one connected in parallel with coil directly and the other in series with GaN switches. Although GaN switches can naturally function as bi-directional switches, their reverse conduction characteristics differ from those in the normal direction. One possible design approach involves connecting two switches in series with opposite directions, with one switch operating in the normal direction and the other in the reverse direction. However, to mitigate potential effects from reverse conduction, each GaN device is used only for one-direction conduction in this design; thus, only one switch is activated at a time. One advantage of the parallel connection of these two GaN switches is the elimination of extra conduction losses from the inactive switch when one switch is activated. Diodes are incorporated into the circuit to ensure one-direction conduction of the GaN switches.

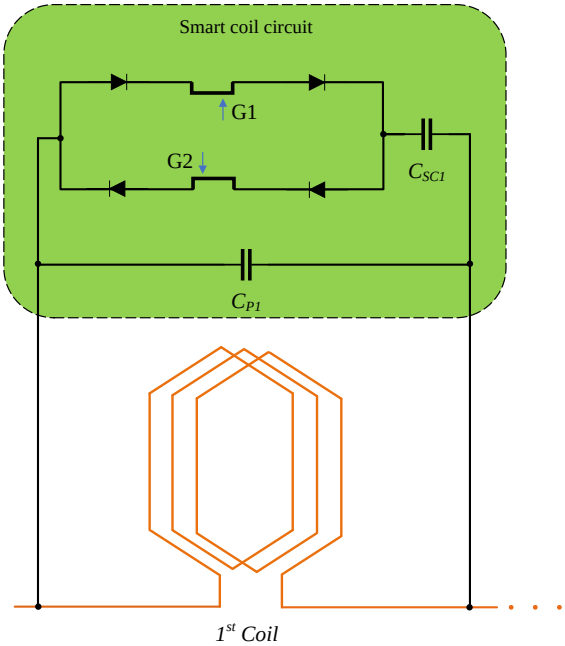


Figure 4.1: The proposed smart coil circuit applied to the first coil

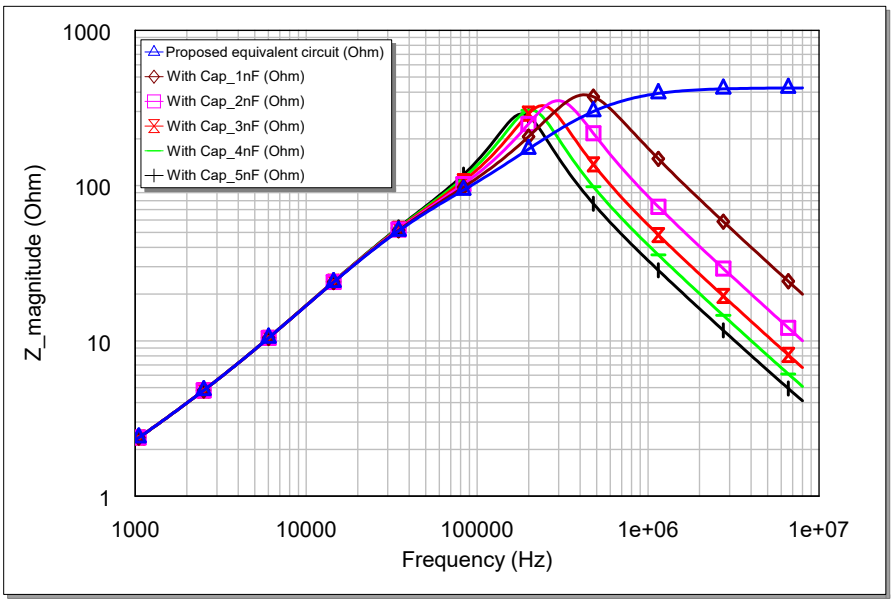


Figure 4.2: The impedance of the first coil with different capacitors

The capacitor C_{P1}, connected in parallel with the coil, aids in reducing the impedance of the first coil at high frequencies. As depicted in Fig. 4.2, the impedance of the first coil decreases further with larger capacitors. Consequently, overvoltage on the first coil can be mitigated. However, the impedance of the second coil remains

unchanged, resulting in the reduced overvoltage from the first coil being transferred to the second coil, potentially causing higher overvoltage there. Consequently, simply adding a fixed capacitor to the first coil does not evenly distribute coil voltage among different coils.

The capacitor C_{SC1}, connected in series with the two GaN switches, operates whenever one of the switches is turned on. In this configuration, the capacitor is effectively connected in parallel with C_{P1}, further reducing the impedance of the coil. Unlike connecting a fixed capacitor in parallel, the impedance of the first coil varies as the GaN switch is toggled on and off. Consequently, the overvoltage on the first coil can be regulated by setting up a threshold voltage, and simultaneously, the overvoltage on the second coil can be indirectly controlled. This approach allows for more dynamic control of coil impedance and voltage distribution.

Additionally, the smart coil circuit can be added to the second coil when the overvoltage exceeds threshold levels and cannot be evenly distributed among the coils as required, as illustrated in Fig. 4.3. By incorporating one more smart coil, the voltage of the third coil can also be indirectly controlled, allowing for more effective management of voltage distribution across multiple coils.

With a system configuration of 120 m cable length and a 20 ns rise time, four scenarios were simulated and compared in 4.4.

-The orange bar represents the coil voltages without any additional circuits or components connected.

-The yellow bar shows the coil voltage with one fixed capacitor connected in parallel with the first coil, with a capacitance value of 2 nF.

-The blue bar presents the coil voltages when the proposed smart coil is added to the first coil.

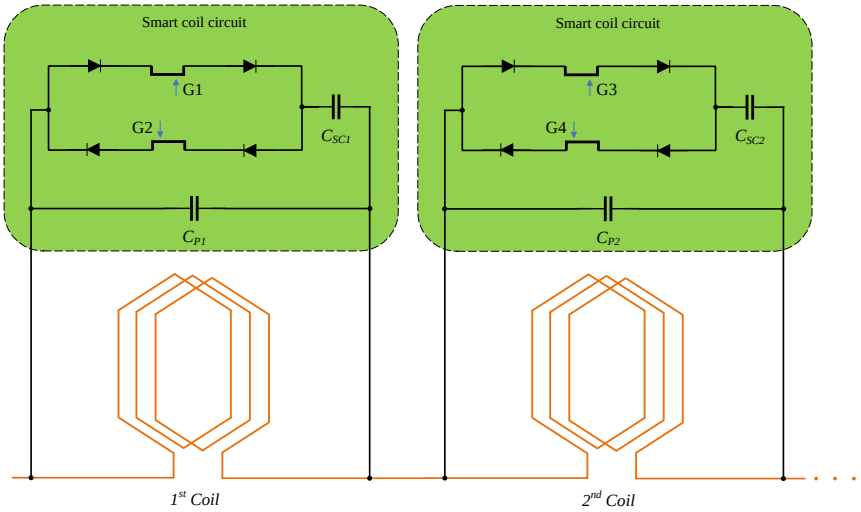


Figure 4.3: The proposed smart coil circuit applied to the first two stator coils

-Lastly, the green bar shows the coil voltages when the proposed smart coil is added to the first two coils.

It is observed that initially, the first coil voltage reaches the highest point without any capacitor or smart coil added to it. Subsequently, the second coil reaches the second highest point when only one fixed capacitor is added to the first coil.

Upon adding the smart coil to the first coil, the first coil voltage can be controlled within the threshold value, while the voltage of the second coil increases and exceeds the threshold voltage. However, this scenario is still preferable to the case with only the fixed capacitor added to the first coil.

Finally, with the green bar, it is evident that the overvoltage has been evenly distributed among the different coils, and none of the coil voltages exceed the threshold voltage when the smart coil is applied to the first two coils. The parameters of the smart coil can be found in Table 4.1.

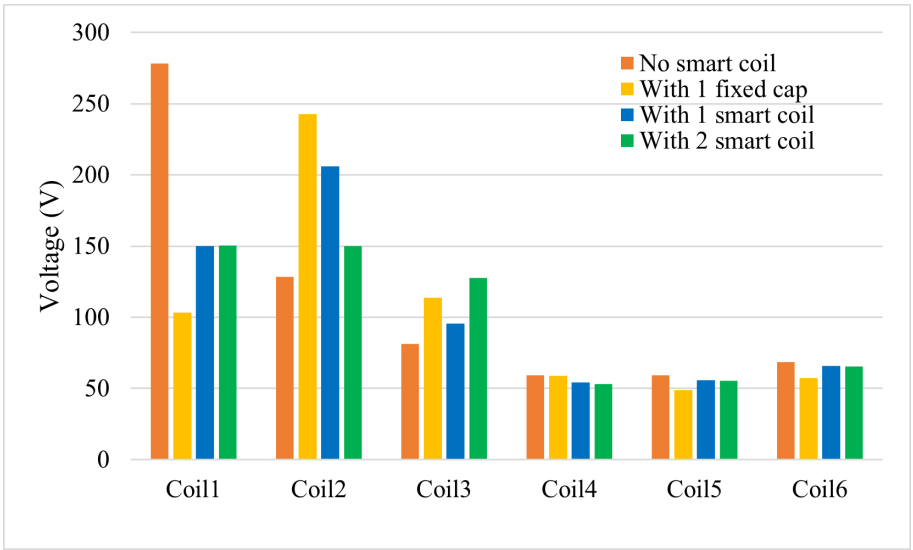


Figure 4.4: The coil voltages comparisons with different circuit typologies

Table 4.1: The parameters of the smart coil

Parameters	Value
C_{SC1}	1.8 nF
C_{P1}	0.2 nF
C_{SC2}	2 nF
C_{P2}	0.01 nF

4.2 Control of the Smart Coil Circuit

The control strategy of the smart coil is illustrated in Fig. 4.5, comprising the input of the coil voltage, a voltage-controlled Schmitt trigger, and the output of the gate signal for the GaN switches.

Firstly, the coil voltage is detected and sent to the voltage-controlled Schmitt trigger, which can be set with a threshold voltage. For instance, the threshold voltage here can be calculated as $Vt-Vh, Vt+Vh$, ranging from 130 V to 150 V. The Schmitt trigger continuously outputs signal 1 as long as the input voltage is between 130 V and 150 V; otherwise, it outputs signal 0.

Subsequently, the output signal is transmitted to the gate controller of the GaN

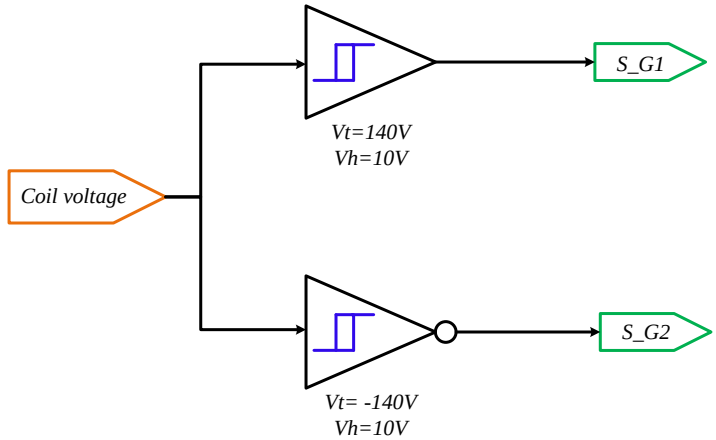


Figure 4.5: The control logic for the smart coil circuit

switches. When S_{G1} is 1, V_{GS} will be provided with a 7 V voltage, causing the GaN switch to turn on. Consequently, with this control strategy, GaN switch 1 will turn on when the coil voltage exceeds the upper threshold voltage of 150 V and remain on until the coil voltage drops below 130 V.

Similarly, the other GaN switch in the opposite direction will turn on when the coil voltage exceeds the threshold voltage of -150 V and remain on until the coil voltage rises above -130 V. Thus, it is ensured that the coil voltage is constrained within the range of -150 V to 150 V.

From Fig. 4.6, it is evident that both the first and second coil voltages are precisely controlled by the GaN switches, with the third coil voltage controlled indirectly. Consequently, all of the first three coil voltages are maintained below the threshold as required.

Furthermore, it can be observed that the second coil voltage is initially controlled from time t1 to t2. This occurs because a larger fixed capacitor is connected to the first coil, causing the second coil voltage to increase to the threshold voltage more quickly than the first coil. Simultaneously, the third coil voltage increases as the

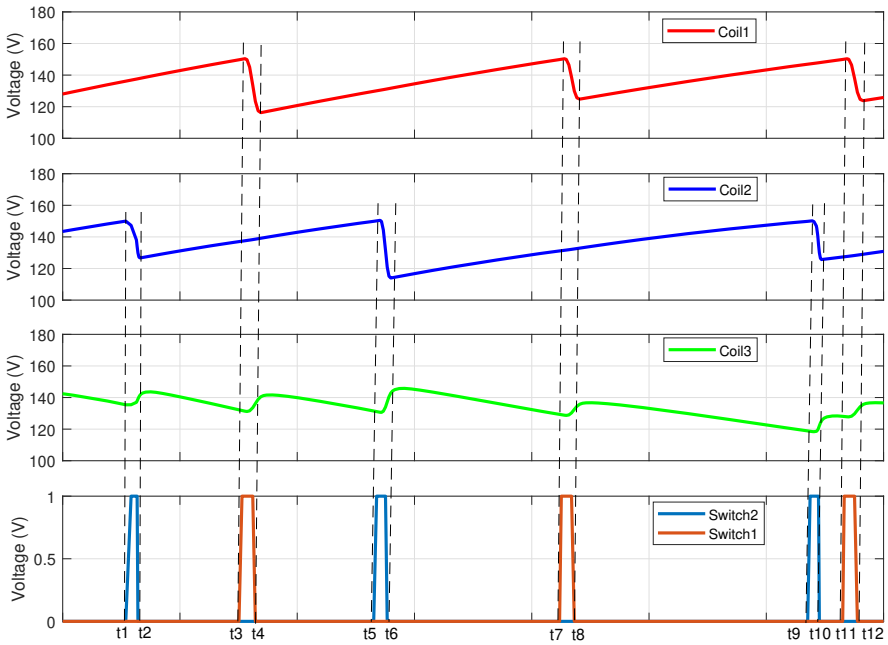


Figure 4.6: The controlled coil voltages

second coil voltage drops.

At the time point t3, the first coil voltage reaches the threshold voltage for the first time, triggering the switch to turn on and resulting in a voltage drop during the time interval (t3, t4). As a result, the third coil voltage increases, indirectly controlled in this manner.

4.3 Parametric Sizing of the Smart Coil Circuit

Designing the four capacitors for the two smart coil circuits, along with determining the threshold voltage, is a crucial aspect of ensuring effective voltage control in the system. While the operating principle introduced in the first section indicates the limitations of controlling coil voltages with fixed capacitors or only one smart coil, highlights the advantage of incorporating the second smart coil lies in its ability to

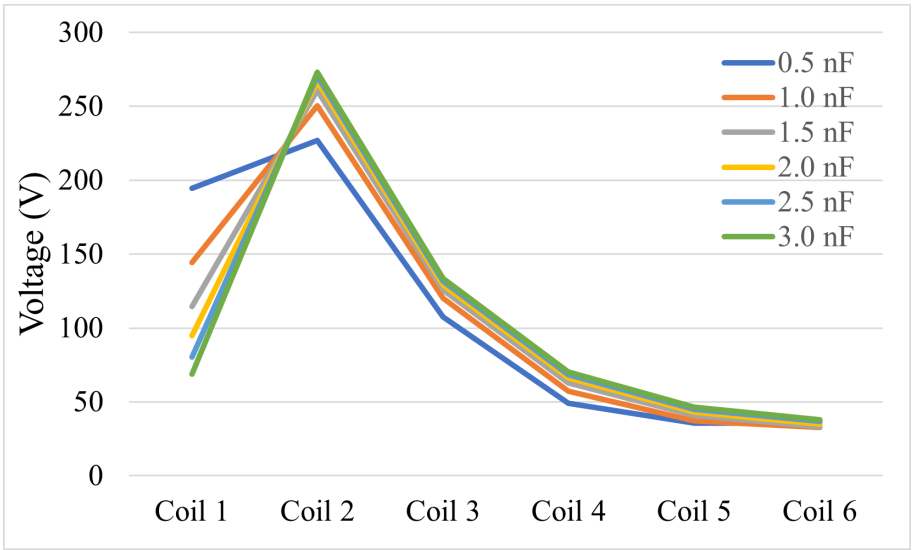


Figure 4.7: The coil voltages with different fixed capacitors

indirectly control the voltage of the third coil. However, designing the values of these four capacitors, along with determining the appropriate threshold voltage, is not a straightforward task.

In this section, we outline the steps for sizing the four capacitors to achieve more even voltage distribution across different coils while ensuring adaptability to various system configurations, including different cable lengths and rise times. The fundamental approach involves sizing the two capacitors for the first smart coil and subsequently using the selected values to size the remaining two capacitors for the second smart coil.

Initially, two system configurations were established for the design assessment. One configuration featured a 29 m cable length with a 40 ns rise time, while the other comprised a 60 m cable length with a 20 ns rise time. The latter case, with its longer cable length and shorter rise time, served to examine an extreme scenario. The maximum voltages observed on the first coil for these two configurations were 300 V and 323 V, respectively. Consequently, the threshold voltage was set to 150

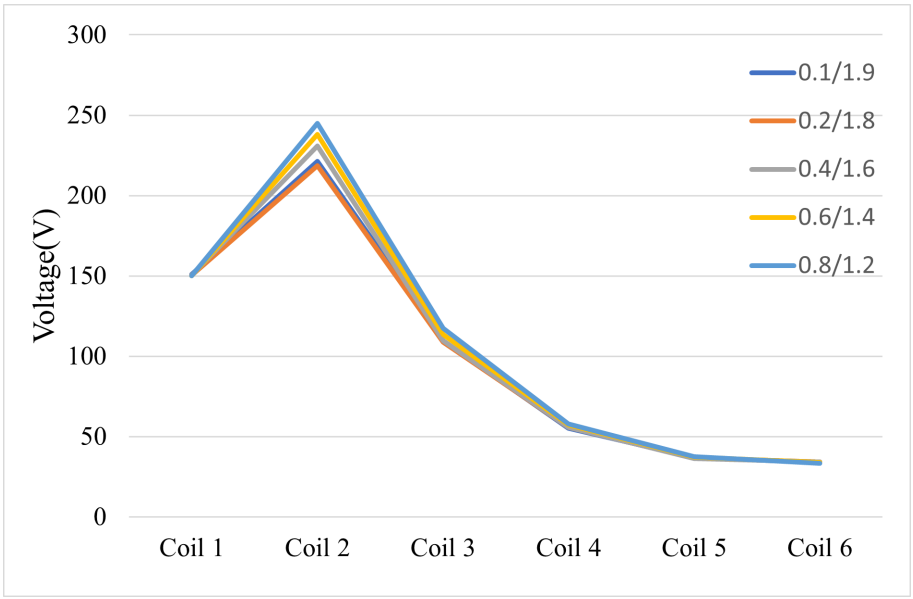


Figure 4.8: The coil voltages with different parameters of the first smart coil

V, half of its original value.

Analyzing the coil voltages with different capacitors (as depicted in Fig. 4.7) revealed that decreasing the voltage on the first coil corresponded to an increase in the voltage on the second coil. A 1 nF capacitor was found to effectively constrain the first coil voltage below 150 V. Therefore, a capacitor with a value larger than 1 nF was deemed suitable. However, selecting the largest possible capacitor was not ideal, as it led to a significant increase in the second coil voltage, which was undesirable.

Based on the collected data, a capacitor with a value of 2 nF was chosen as it effectively balanced the reduction in the first coil voltage with the increase in the second coil voltage, thus aligning with the design goal.

Next, the chosen capacitor needed to be divided into a fixed capacitor and a capacitor connected to the switches. Various combinations of these two capacitors were simulated for the two system configurations, and the resulting coil voltage distributions are depicted in Fig. 4.8. The legend indicates the values of C_{P1} (the fixed capacitor) and C_{SC1} (the capacitor connected with the switches), respectively.

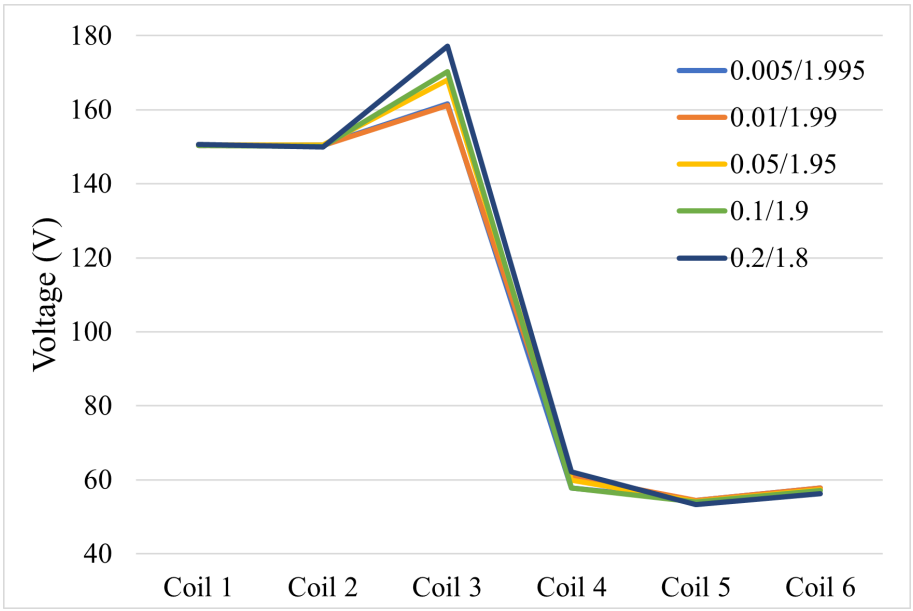


Figure 4.9: The coil voltages with different parameters of the second smart coil

A general trend observed was that as the capacitor connected directly in parallel decreased in value, the voltage on the second coil also decreased. However, upon comparison of the results from configurations (0.1/1.9) and (0.2/1.8), it was noted that the latter yielded even better outcomes. Consequently, the parameters of (0.2/1.8) for the first smart coil were selected.

Subsequently, with the selected parameters for the first smart coil, an analysis was conducted on the effects of the second smart coil circuit's parameters on the coil voltage distributions. To validate the second configuration through simulation, the parameters of the second smart coil were sized using the specifications of a 60 m cable length and 20 ns rise time.

The results shown in Fig. 4.9 indicate that reducing the value of C_P2 leads to a smaller increase in voltage on the third coil. However, upon comparing configurations (0.01/1.99) and (0.005/1.995), it was observed that even when C_P2 was halved from 0.01 nF, the voltage distribution remained almost the same as in the case of (0.01/1.99). This suggests that there is a limit to the reduction of C_P2, and a value

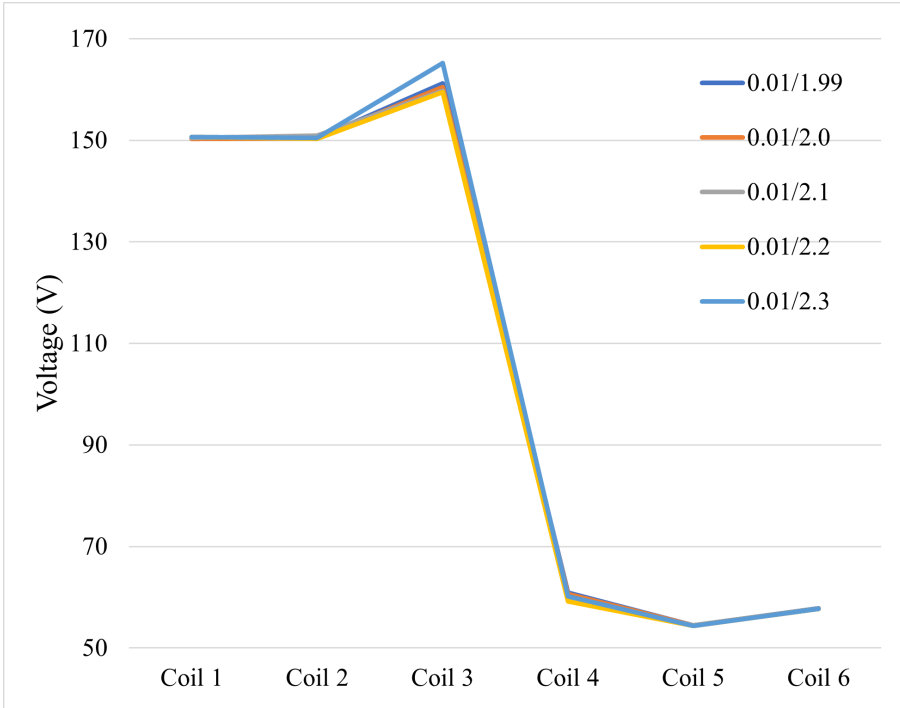


Figure 4.10: The coil voltages with different parameters of the second smart coil

of 0.01 nF was chosen for C_P2.

Finally, with C_P2 maintained at 0.01 nF, an investigation was conducted into the effects of increasing C_SC2. The results depicted in Fig. 4.10 indicate that the third coil voltage experiences a slight decrease as C_SC2 is increased, but this decrease is not indefinite. Conversely, the third coil voltage begins to increase when C_SC2 reaches 2.3 nF. Therefore, based on this analysis, the value of (0.01/2.0) for the second smart coil capacitors was chosen.

It is noteworthy that although the third coil voltage exceeds 150 V and reaches approximately 160 V with the chosen parameters, further simulation across different system configurations revealed that all coil voltages could be constrained below 150 V. Additionally, given that the first coil voltage reaches 323 V with a 60 m cable length and 20 ns rise time, the threshold voltage could be adjusted to 160 V accordingly, ensuring all coil voltages remained below this threshold with the selected parameters.

Further simulation results with the sized parameters will be presented in the next chapter.

Chapter 5 Simulation Results

This chapter integrates the matched high-frequency generator model, cable model, and converter into a system. It begins by presenting the simulation results of surge overvoltage, focusing on line-to-line overvoltage and the uneven voltage distribution across different coils. Subsequently, the simulation results with implemented smart coils are presented. Through these simulations, the effectiveness of overvoltage mitigation with smart coils is demonstrated.

5.1 Baseline Simulation of the Generator-Converter System

In this section, the system simulation results are presented by combining the high-frequency models matched with a 29 m cable and a 240 V generator from Chapter 3, along with the SPWM-controlled power converter.

The line-to-line voltage comparisons between the converter and generator terminals are illustrated in Fig. 5.1. With a cable length of 29 m and a rise time of 40 ns, the line-to-line voltage on the generator terminal is 1.75 times that of the voltage on the converter terminal. In [43], the analysis of surge overvoltage utilized an impedance-based approach, which demonstrated that the oscillation frequency of surge overvoltage corresponds to the anti-resonance frequency of cable differential mode impedance. From the simulation results shown in Fig. 5.1, the line-to-line surge overvoltage oscillation frequency, measured at 1.52 MHz, aligns well with the cable DM impedance anti-resonance frequency, which is 1.56 MHz, as shown in Fig. 3.24. This alignment suggests good accuracy of the generator-cable-converter system and indicates that the system is well-tuned.

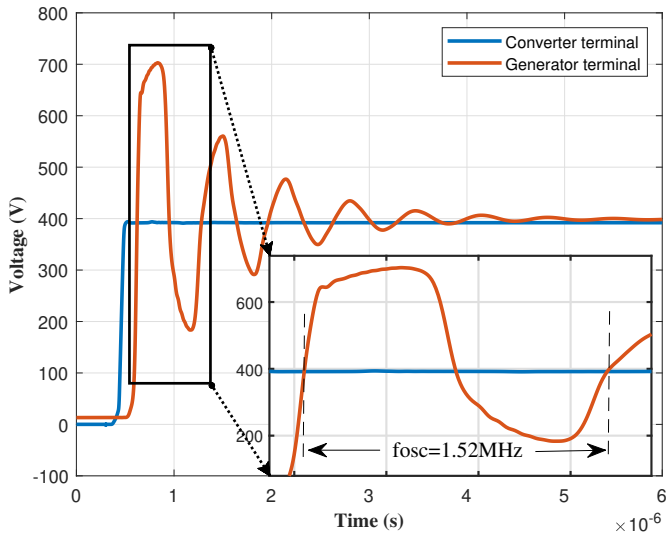


Figure 5.1: The line-to-line voltage comparisons between the converter and generator terminals

Furthermore, Fig. 5.2 showcases the uneven distribution of voltage across different coils, which is a crucial characteristic of the surge overvoltage issue. It is evident that the voltage on the first coil is approximately 2 times that of the second coil and more than 3 times that of the third coil. Ideally, each of the 6 coils should be capable of evenly sustaining a maximum of 2/3 of the line-to-line voltage (on the generator terminal), which equates to 77.78 V. However, the first coil is required to sustain 3.86 times the expected amount. Consequently, the design specifications for all of the copper wire should meet the requirements of the first coil, leading to an increased overall cost of the copper wire.

As discussed in Chapter 1, the investigations into voltage reflection theory indicate that overvoltage escalates with an increase in cable length and a decrease in rise time. In Chapter 3, a distributed 1-meter high-frequency cable model was constructed, enabling the simulation of various cable length adjustments by aggregating different quantities of 1-meter cable models. Moreover, rise time adjustments are feasible by modifying the gate resistance of the SiC MOSFET.

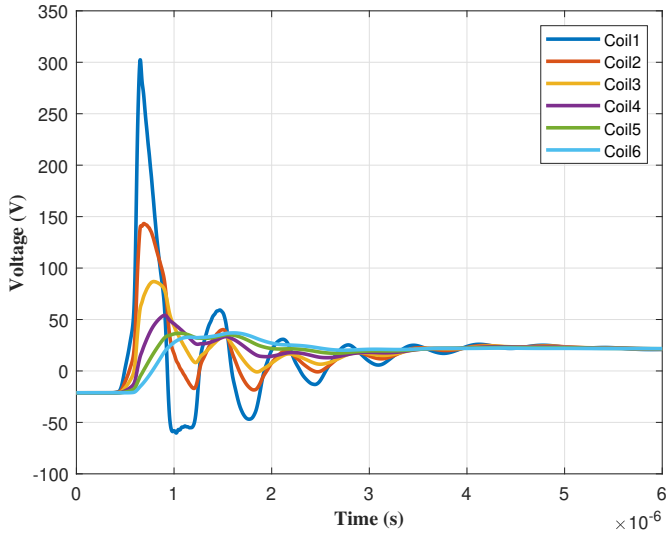


Figure 5.2: The uneven voltage distribution on different coils

The trend in the line-to-line voltages at the generator terminal, influenced by cable length and rise time, is depicted in Fig. 5.3. The normalized voltage presented here is derived by dividing the line-to-line voltage at the converter terminal. The observed overvoltage variation aligns well with theoretical expectations. It's noteworthy that the line-to-line voltage at the generator terminal doesn't escalate indefinitely with increasing cable length; instead, it reaches a saturation point beyond a certain cable length, as evident from the simulation outcomes. This behavior is consistent with the voltage reflection theory discussed in Chapter 3 since the cable impedance also increases with longer cable lengths. Additionally, Fig. 5.4 illustrates the changing trend in the first coil's voltage concerning cable length and rise time. The normalized voltage shown here is computed by dividing two-thirds of the line-to-line voltage at the converter terminal, representing the maximum total voltage for one phase.

The validity and accuracy of the high-frequency distributed cable model and generator model have been confirmed by the simulation results presented above. Consequently, this developed system can be utilized to assess the effectiveness of the smart

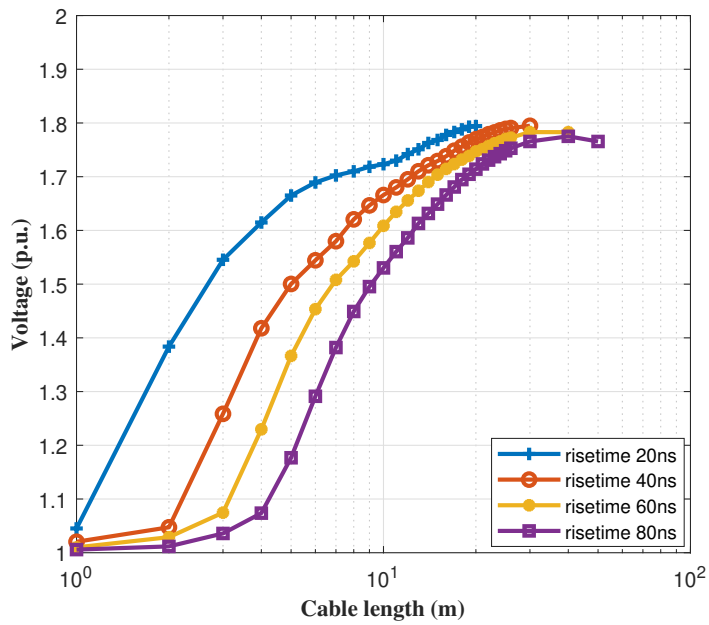


Figure 5.3: The line-to-line voltage across the generator terminal with different cable length and rise time

coil concept in the following section.

5.2 Overvoltage Mitigation with the Proposed Smart Coil Concept

This section demonstrates the effectiveness of the smart coil by applying it to the first coil alone and then to both the first and second coils. The difference in overvoltage mitigation between these two integration methods is illustrated through simulation results.

Initially, the smart coil circuit described in Chapter 4 is employed on the first coil with a 29 m cable length and 40 ns rise time. The simulation outcomes are depicted in Fig. 5.5. It is obvious that the voltage on the first coil has been reduced from 300 V to 150 V, achieving a 50% mitigation rate. However, the voltage on the second coil has increased and exceeded the threshold voltage of the first coil, which does not meet the design criteria. Additionally, the voltage on the third coil has also increased

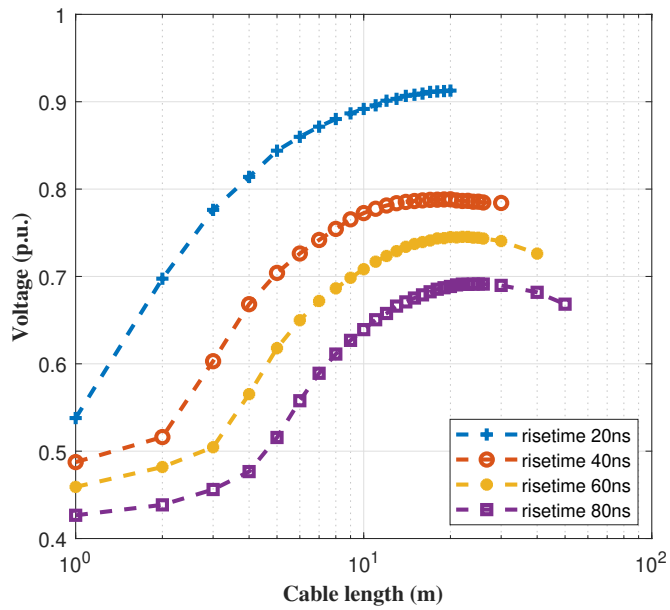


Figure 5.4: The first coil voltage with different cable length and rise time

but remains below the threshold voltage.

Subsequently, to ensure that all coil voltages remain below the threshold value, the smart coil circuit is also implemented on the second coil. The simulation results are displayed in Fig. 5.6. In this scenario, all coil voltages are maintained below the threshold value. Although the voltage on the third coil increases passively, it remains below the upper limit value.

The effectiveness of overvoltage mitigation by applying one smart coil versus two smart coils is compared in Fig. 5.7. Employing two smart coils, both on the first and second coils, results in better mitigation capability. Overvoltage is distributed more evenly among the first three coils and remains below the threshold voltage, thus meeting the design requirements.

To verify the applicability of these integration methods, simulations were conducted for another system configuration with a 60 m cable length and 20 ns rise time.

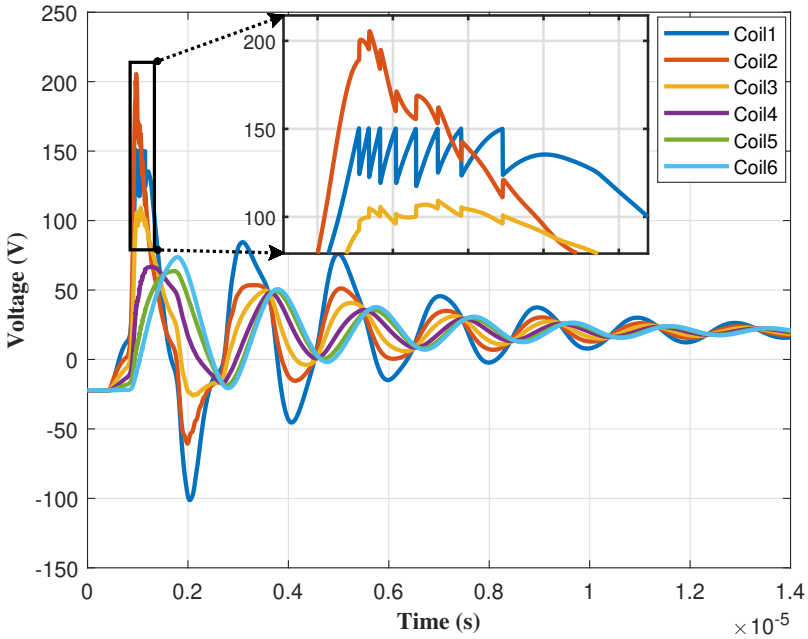


Figure 5.5: The coil voltages with smart coil on the first coil

Similarly, initially applying the smart coil circuit solely on the first coil yielded the simulation results shown in Fig. 5.8. While the first coil voltage was mitigated, the second coil voltage increased to nearly 250 V. Comparing this scenario to the first one (cable length = 29 m, rise time = 40 ns), the increase in the second coil voltage was more pronounced due to the longer cable length and shorter rise time. Simulating this scenario aids designers in verifying the application of extreme cases.

After integrating the smart coil into the second coil as well, it's evident from Fig. 5.9 that both the first and second coil voltages have been mitigated below the threshold value, while the third coil voltage increased to 160 V, surpassing the threshold value. However, since the third coil voltage of 160 V is close to the threshold value of 150 V, the mitigation results are still acceptable. Fig. 5.10 illustrates that the implementation with two smart coils outperforms using only one smart coil.

In this scenario, the first coil voltage can reach 323 V without the application

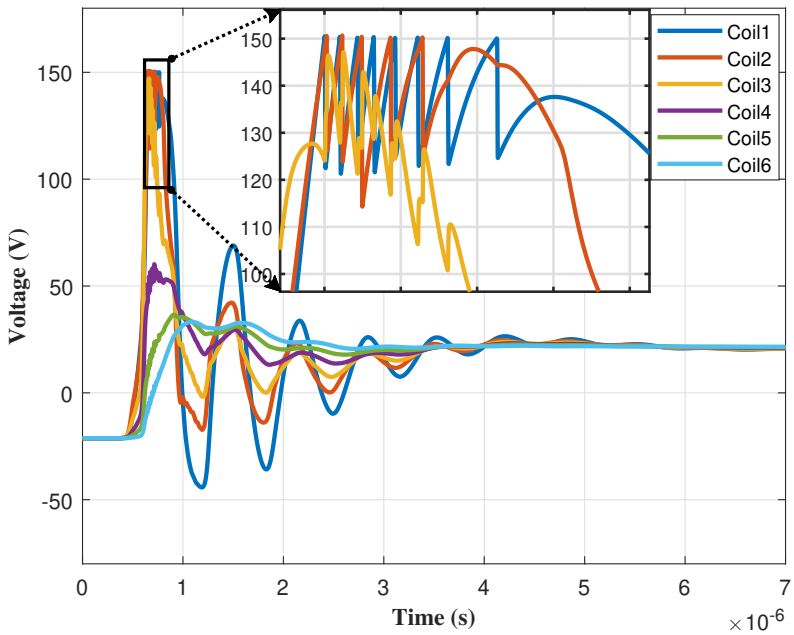


Figure 5.6: The coil voltages with smart coil on the first and second coils

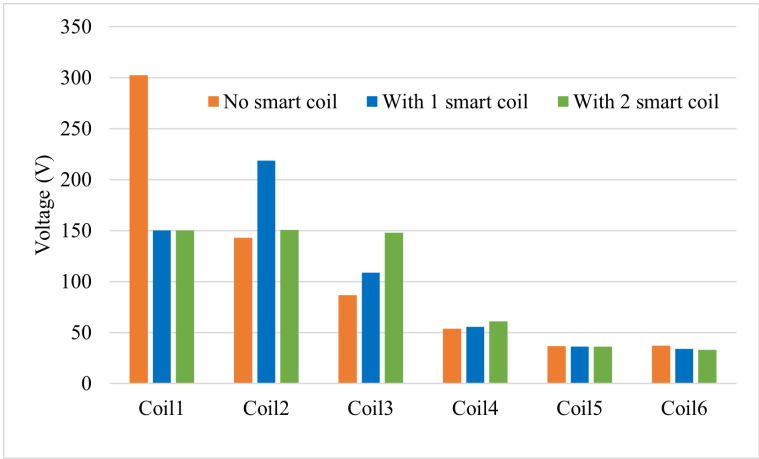


Figure 5.7: Comparisons of the coil voltages with and without the smart coils (cable length = 29 m, rise time = 40 ns).

of the smart coil circuit. Consequently, the threshold voltage can be set to 160 V, approximately half of its maximum value. By applying the same parameters of the smart coil circuit to the first two coils, all coil voltages can be constrained within the limit, as depicted in Fig. 5.11. Additionally, Fig. 5.12 compares the coil voltages with one and two smart coil circuits, illustrating that overvoltage is more evenly

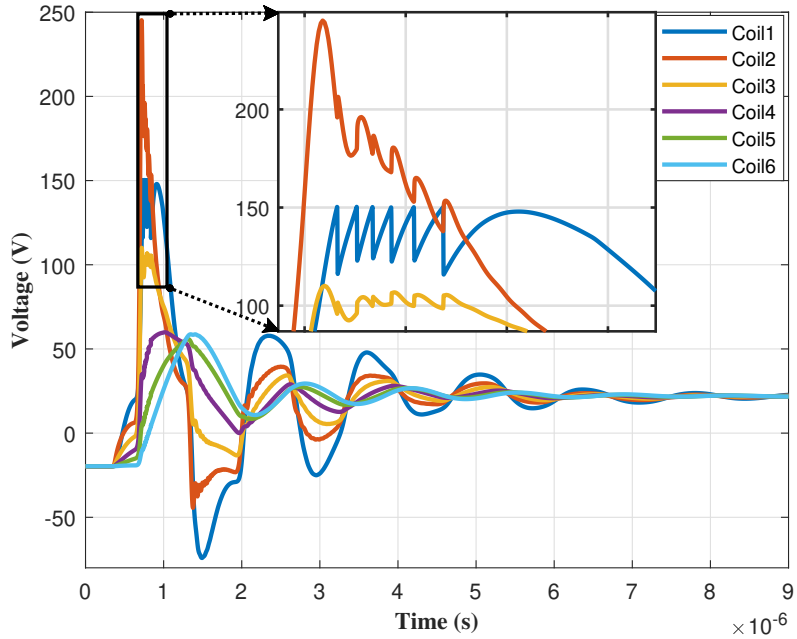


Figure 5.8: The coil voltages with smart coil connected across the first coil.

distributed among different coils when two smart coils are applied.

In the third scenario, the cable length is configured to 120 m, considering the real application of a generator-converter system in a wind turbine, which typically has around 100 m of cable connecting the generator and converter. The rise time is maintained at 20 ns.

Similarly, when only one smart coil is applied, the second coil voltage exceeds the threshold value, as shown in Fig. 5.13. However, with two smart coils applied, all of the coils' voltages are under the upper limit, as shown in Fig. 5.14. The comparisons between the application of one smart coil and two smart coils are shown in Fig. 5.15.

5.3 Conclusion

The baseline simulation of the generator-converter system, incorporating the matched high-frequency distributed cable model and per-coil generator model, demonstrates

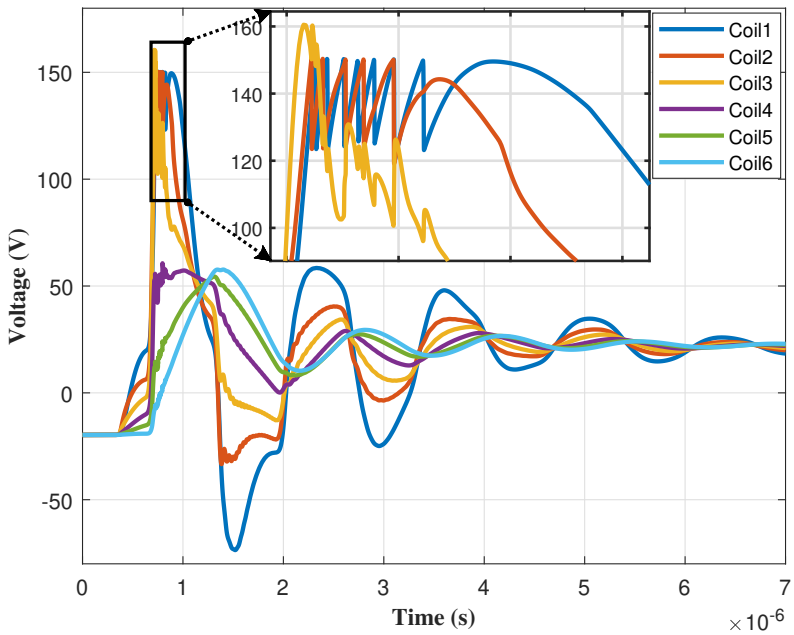


Figure 5.9: The coil voltages with smart coil connected across the first and second coils.

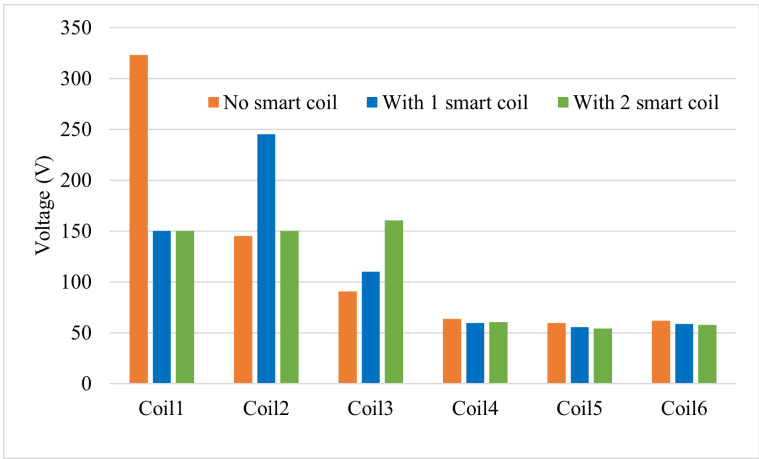


Figure 5.10: Comparison of the coil voltages with and without the smart coils (cable length = 60 m, rise time = 20 ns).

that the surge overvoltage reflection phenomenon aligns well with theoretical expectations. The line-to-line overvoltage increases with longer cable lengths and shorter rise times, while the overvoltage distribution across coils remains uneven, resulting in the first coil bearing a significantly higher voltage compared to others. These baseline simulation results confirm the rationality and accuracy of the matched high-frequency

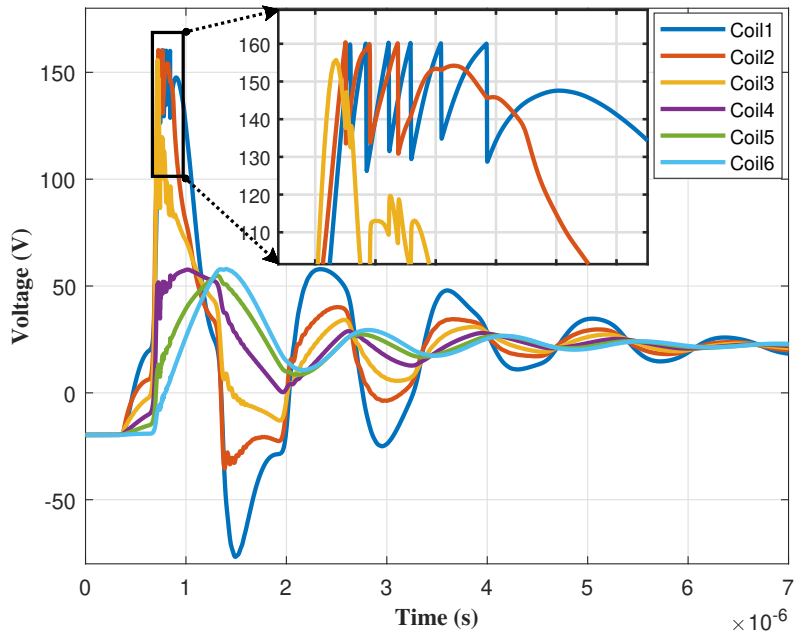


Figure 5.11: The coil voltages with smart coil connected across the first and second coils. (threshold voltage = 160 V)

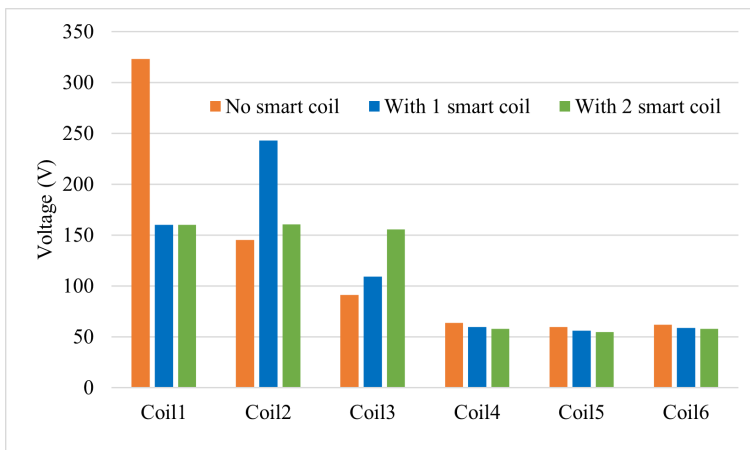


Figure 5.12: The coil voltages comparisons with and without the smart coils (cable length = 60 m, rise time = 20 ns, threshold voltage = 160 V).

cable model and generator model.

The simulation results from the three scenarios with varying cable lengths and rise times validate the efficacy of the smart coil concept. When only one smart coil is integrated with the first coil, it consistently leads to an increase in the second coil voltage, surpassing the threshold value. However, with two smart coils integrated

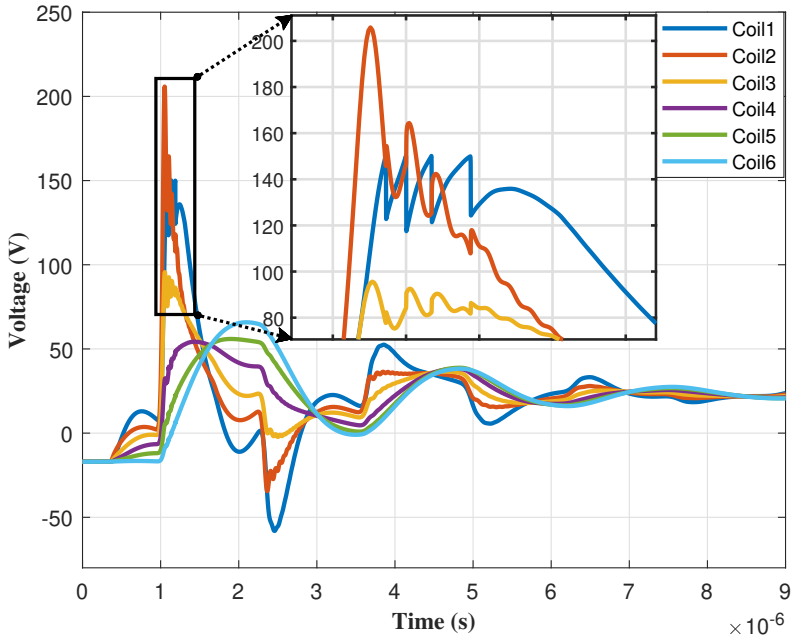


Figure 5.13: The coil voltages with smart coil connected across the first coil.

into both the first and second coils, two out of three scenarios demonstrate effective control of all coil voltages under the upper limit. Even in the scenario with a 60-m cable and 20-ns rise time, where the third coil voltage exceeds the threshold by 6.7%, it is deemed acceptable. Thus, the simulation results confirm that the reflected overvoltage on coils can be effectively mitigated and more evenly distributed by employing two smart coils across both the first and second coils of the generator.

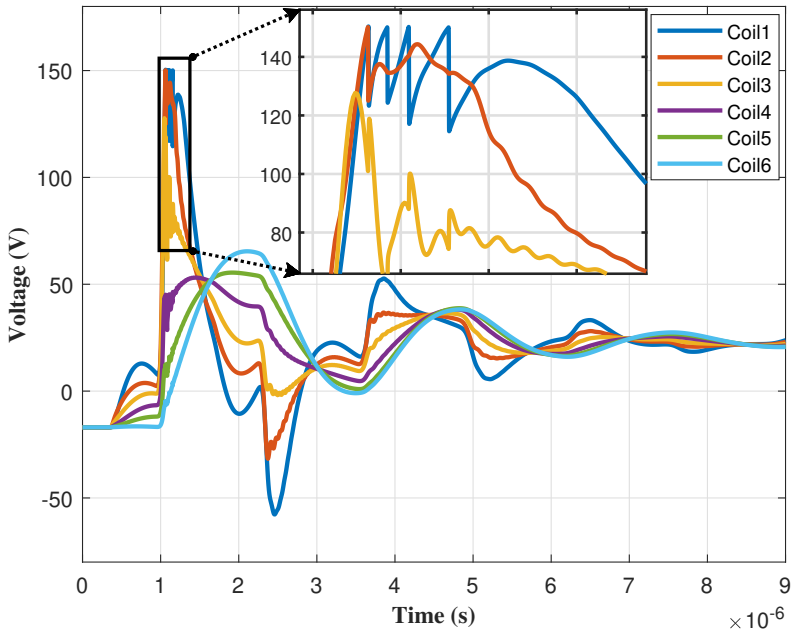


Figure 5.14: The coil voltages with smart coil connected across on the first and second coils.

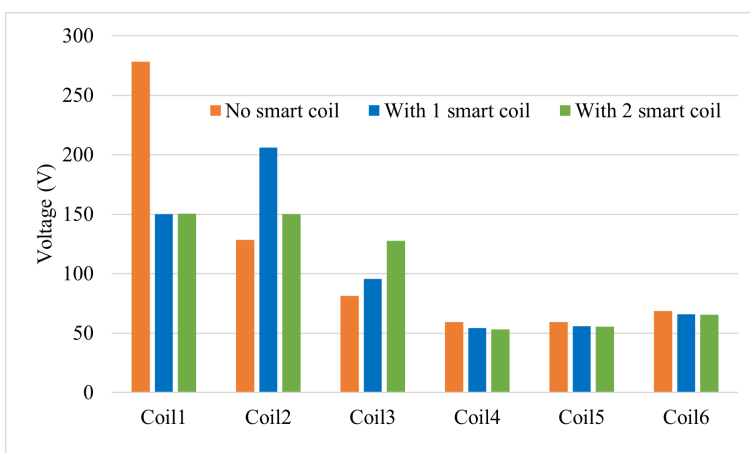


Figure 5.15: Comparison of the coil voltages with and without the smart coils (cable length = 120 m, rise time = 20 ns).

Chapter 6 Conclusion and Future Work

6.1 Conclusion

The global demand towards carbon neutrality has spurred the transition from fossil fuel-based energy to clean and renewable sources. Wind turbine systems have emerged as pivotal players in this endeavor, with increasing installations worldwide, both on-shore and off-shore. In many applications, wind turbine systems feature a configuration where the generator is located atop the nacelle, while the converter is located at the foundation of the tower, facilitating maintenance. However, such an arrangement necessitates long power cables connecting the generator and power converter, which can lead to reflected surge overvoltage at the generator terminals. If not mitigated, such high-frequency voltage spikes will damage the insulation systems of generator windings, leading to significant downtime cost or even power outage. This thesis introduces an innovative mitigation solution named as the smart coil, to mitigate the overvoltage challenges by implementing it on the first one or two coils of the generator close to the converter side, thereby promoting a more even distribution of surge voltages across the coils.

The investigation into transient surge overvoltage reflection theory revealed that it is primarily influenced by the surge impedance mismatch, cable length and switching device rise time. As cable length increases and rise time decreases, line-to-line surge overvoltage tends to rise up within a certain range. However, the surge overvoltage reaches saturation as cable length becomes sufficiently long due to the increase in total cable impedance, as presented in Chapter 5.

Existing overvoltage mitigation solutions were studied and categorized based on the factors contributing to overvoltage issues. Some solutions target the rise time of switching devices, potentially complicating control algorithms. Others focus on impedance matching between the cable and electric machine, often resulting in the addition of bulky and lossy filters that can reduce system efficiency.

To investigate the reflected surge overvoltage issues in generator-converter systems and to validate the proposed smart coil concept through simulation, the high-frequency cable and generator models were developed based on the selected real-world components. Impedance measurements were conducted across a wide frequency range for a one-meter length of the selected cable, and parameters of the distributed cable model were adjusted to match the measured impedance from a 29-meter cable. Similarly, impedance measurements were performed for each coil of the selected generator, with one coil chosen as the unified high-frequency coil model. Chapter 5 confirmed the accuracy of the system model.

The proposed smart coil concept was detailed in terms of operating principles, control logic, and parametric sizing. It was demonstrated that surge overvoltage cannot be evenly distributed across coils with only fixed capacitors or a single smart coil. Only with two smart coil circuits applied to the first two coils can surge overvoltage be more evenly distributed, as the third coil voltage can be indirectly controlled in this manner. The operating principle and control logic were found to be relatively straightforward compared to the parametric sizing process, which highlighted the importance of appropriately sizing capacitors connected in parallel with coils.

Constructing and simulating a generator-converter system with high-frequency cable and generator models, alongside an active controlled converter, revealed line-to-line surge overvoltage and its variation with cable length and rise time. The simulation

also illustrated the uneven distribution of coil voltages, with the first coils bearing the brunt of the overvoltage, particularly the first coil. These simulation results confirmed the accuracy of the previously constructed system model and its suitability for verifying the effectiveness of the smart coil concept. With parametrically sized smart coil circuits applied to the first two coils, surge overvoltage was more evenly distributed across coils, and all coil voltages were constrained below the threshold value. Thus, the proposed innovative smart coil concept was validated as effective in mitigating coil voltages.

6.2 Future Work

Certainly, while simulation results provide valuable insights and initial validation, experimental verification would further enhance the credibility and robustness of the smart coil concept. Although time limitations may have hindered immediate experimental verification, it remains a crucial step for confirming the effectiveness of the proposed solution in real-world scenarios.

6.2.1 Experimental Verification

In Chapter 3, it was established that a 12-AWG 4-conductor 29-meter cable and a 5-kW tapped generator were utilized for high-frequency modeling based on impedance measurement data. Accordingly, a 200-kW two-level SiC back-to-back power converter will be developed in the laboratory and connected to the tapped generator to investigate reflected surge overvoltage across generator coils.

Firstly, the line-to-line voltage over both the power converter and generator will be measured and compared with simulation results. Key metrics such as amplitude and oscillating frequency of the line-to-line voltage over the generator terminal will

serve as indices to assess the accuracy of the cable and generator models derived from the simulation.

Secondly, surge overvoltages across the first few coils will be measured and compared with simulation results to validate the uneven distribution of surge voltage across different coils as predicted by the simulation.

Lastly, the proposed smart coil circuit will be implemented on the first two coils, and coil voltages will be measured and compared with cases where the smart coil circuit is not applied. The effectiveness of voltage mitigation on the first two coils will be observed while ensuring that the third coil voltage remains below the threshold voltage. Additionally, experimental results will be compared with simulation data to further verify the accuracy of the simulation system model.

6.2.2 Develop an Adaptive Control Scheme for the Smart Coil

In this thesis, capacitor sizing was determined primarily through simulation results, focusing on whether the coil voltage could be constrained under the threshold value. However, an alternative approach for improving voltage mitigation effects on the coils involves designing an adaptive control scheme for the smart coil based on surge impedance.

In the future, an adaptive surge impedance matching scheme could be developed. This scheme would involve updating the impedance matching process in real time according to an adaptation law. The goal would be to ensure that the parallel branch of the smart coil circuit ideally provides a zero reflection wave at the generator terminal, thereby further enhancing voltage mitigation effects on the coils.

6.2.3 Develop a Design Automation Software Tool

The parametric sizing process outlined in Chapter 4 can be enhanced and condensed into an automated design process with inputs based on specific design requirements. This automation could lead to the development of a software tool aimed at sizing the power components within the smart coil circuit. Such a tool would be invaluable for potential large-scale manufacturing or commercialization efforts in the market.

6.2.4 Develop a Self-Powered Gate Driver DC Supply Circuit

In this smart coil concept, the power supply for the gate drivers of the GaN switches is supposed to be an independent power source. To further downsize the smart coil circuit, the voltage in one of the stator coils (i.e., the 2nd coil) can be rectified into DC and serve as the DC power supply for the gate drivers of the GaN switches.

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