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Development of DC Circuit Breakers for Medium-Voltage Electrified Transportation

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DEVELOPMENT OF DC CIRCUIT BREAKERS FOR MEDIUM-VOLTAGE ELECTRIFIED TRANSPORTATION

THESIS

A thesis submitted in partial fulfillment of the requirements for the degree of Master of Science in Electrical Engineering in the College of Engineering at the University of Kentucky

By

Trevor M. Arvin

Lexington, Kentucky

Director: Dr. JiangBiao He

Department of Electrical and Computer Engineering

2022

ABSTRACT OF THESIS

DEVELOPMENT OF DC CIRCUIT BREAKERS FOR MEDIUM-VOLTAGE ELECTRIFIED TRANSPORTATION

Medium-voltage DC (MVDC) distribution is an enabling technology for the electrification of transportation such as aircraft and shipboard. One main obstacle for DC distribution is the lack of adequate circuit fault protection. The challenges are due to the rapidly rising fault currents and absence of zero crossings in DC systems compared to AC counterparts. Existing DC breaker solutions lack comprehensive consideration of energy efficiency, power density, fault interruption speed, reliability, and implementation cost.

In this thesis, two circuit topologies of improved DC circuit breakers are developed: the resonant current source based hybrid DC breaker (RCS-HDCB) and the high temperature superconductor fault current limiter based solid state DC breaker (HTS-FCL-SSDCB). The RCS-HDCB utilizes a controllable resonant current source based upon wide bandgap (WBG) switches that enable low loss and fast fault interruption due to the fast switching speed. The voltage applied by the controllable resonant current source is much lower than the rated voltage of the DC breaker, allowing the utilization of significantly lower voltage rated WBG switches. The conduction path's sole component is a fast-actuating ultra-low resistance vacuum interrupter for high efficiency during normal operation. As the second DC breaker concept, the HTS-FCL-SSDCB is subdivided into a fault current limiter (FCL) and solid state DC breaker (SSDCB). The FCL is based upon a high temperature superconductor cable which has natural fault current limiting capabilities while having negligible insertion losses for normal load currents. The SSDCB utilizes WBG switches to decrease conduction losses compared to Silicon-based breakers. The FCL reduces fault current such that the number of semiconductive switches in the SSDCB is minimized. Both breakers feature a metal-oxide varistor device in parallel to clamp overvoltages and dissipate energy after fault interruption.

Modeling, simulation, and analysis in electrical and thermal domains are conducted to verify the functionality of the DC circuit breakers. The simulation results confirm the feasibility of these two DC breakers in their proposed applications of 2.4 kV electric aircraft and 20 kV shipboard MVDC distribution systems.

KEYWORDS: Circuit breaker, MVDC, resonant current source, high temperature superconductor, fault current limiter

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May 6, 2022

DEVELOPMENT OF DC CIRCUIT BREAKERS FOR MEDIUM-VOLTAGE ELECTRIFIED TRANSPORTATION

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Chapter 1 Introduction

It has become clear that global climate change is becoming an increasingly pressing issue with each passing year. Humanity as a whole must work together across the scientific and political spectrum to combat our effect on the environment. That is why advancements in transportation, power generation and distribution must be made to do its part in curbing greenhouse gas emissions.

We have come to rely on fossil-fuel-based transport, but it accounts for a large amount of global emissions. These include vehicles such as the average automobile, aircraft, and ships. Transportation accounts for 29% of emissions in the United States [1] and 24% of emissions globally [2]. The emissions of these vehicles needs to be reduced to help curb the effects of global warming. This is the motivation in electrifying these vehicles to make hybridized and all-electric versions. These new vehicular systems need efficient and robust power distribution. Hybrid and electric automobiles are already being adopted in the market, but the development of electrified aircraft and shipboard is more challenging due to the much higher power ratings and complicated environmental operating environment. Referring to Fig. 1.1, aircraft and shipboard account for 12% of all transportation emissions in the United States. Emissions due to aircraft are especially harmful due to their deposition directly into the atmosphere [3]. The electrification of these modes of transport can help to drastically reduce their emissions. This presents new engineering challenges with the possibility of incorporating advanced electric technologies. Medium voltage DC (MVDC) distribution is one such promising technology for the enabling of electrified aircraft and shipboard, due to the advantages of low cable weight, high energy

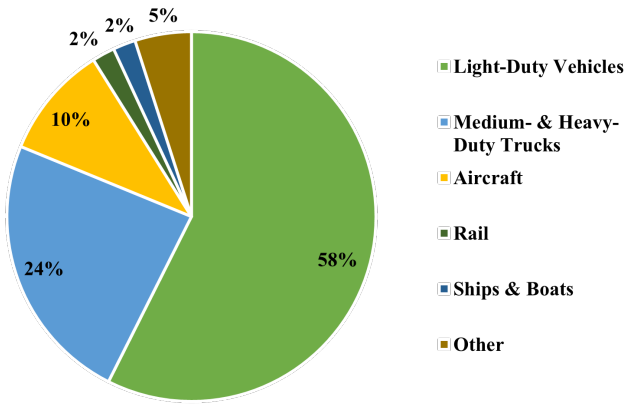


Figure 1.1: U.S. transportation sector greenhouse gas emissions by source [1].

efficiency, and low cost [4–6]. However, the main limitation for widespread implementation of MVDC distribution is the lack of adequate circuit protection. Unlike AC systems, MVDC systems have higher short-circuit current resulting from the lower impedance, and there is no inherent zero crossing in the DC current to extinguish an arc. Thus, the conventional AC circuit breakers cannot be applied for DC systems. This thesis will be focused on developing MVDC circuit breakers (CB) that are fast, reliable, compact, and efficient for future electrified aircraft and shipboard applications.

1.1 Research Motivation

MVDC systems have been proposed as a promising technology for future aircraft and shipboard systems. These systems can vary in degree of electrification such as more-electric, hybrid, and all electric topologies. All of these topologies will be crucial in implementing more efficient, powerful, and environmentally friendly vehicles. Each requires robust fault protection since they are reliant on their electric distribution systems.

MVDC has several advantages over conventional AC distribution. These include reductions in cable weight, system cost, eliminated need for synchronization, and increased efficiency (e.g., elimination of corona losses, fewer energy conversions, no reactive power transmission, etc.). For instance, AC distribution needs at least three cables to transmit all three phases. In DC, only two cables are needed for the positive and negative DC bus, and more power may be transmitted for the same cable cross-section [7]. This provides a crucial increase in system power density and efficiency that is pivotal in weight-critical transportation applications. The main technical barrier in the way of MVDC distribution is the lack of adequate circuit protection. The causes of difficulty in DC circuit protection is detailed in section 1.3.

1.2 Electrified Propulsion Distribution Systems

DC distribution is best utilized in electrified propulsion due to the high efficiency and high power density. To enable this and allow for widespread implementation, fast and efficient circuit breakers must be developed. Any mode of transportation stands to benefit from electrification, but the work herein will focus on the higher-power applications of aircraft and shipboard.

The general propulsion topology of an electric aircraft is provided in Fig. 1.2. For simplicity, The exact topology depicted is an all-electric aircraft with a 2.4 kV DC bus, but other configurations are possible. The voltage of the battery is boosted with

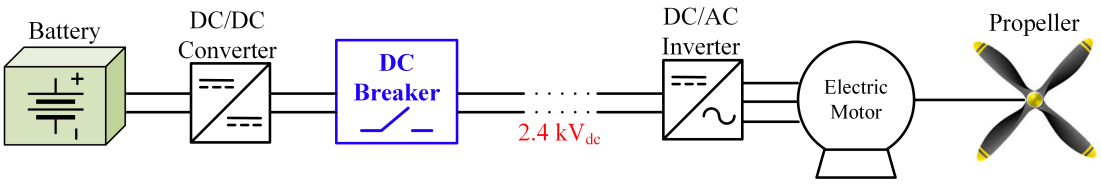


Figure 1.2: General topology of an all-electric aircraft propulsion system

a DC/DC converter to a higher voltage for efficient distribution across the aircraft. This can be used to power many electrified systems. These systems can replace more complex and inefficient conventional mechanical systems, such as pneumatics or hydraulics [8]. In the figure, the DC breaker is shown installed on the 2.4 kV DC bus. If a fault were to happen between the DC circuit breaker and any of the electric loads (e.g., DC/AC inverter, wing de-icers, wing actuators, etc.), then the breaker would isolate the fault from the DC source before any damage could be done. This all-electric type is suited for short range commuter craft up to single-aisle aircraft. This is due to the lithium ion battery having a much lower power density than jet fuel and not being sufficient for long range flight. Larger aircraft with longer range can be developed if a jet fuel internal combustion engine were added to assist the stored battery energy (i.e., Hybrid electric). These could be in several different configurations such as more-electric, series, parallel, or series-parallel. These systems have shown good performance in reducing fuel burn and increasing efficiency. For instance, the Boeing 787 uses a more-electric topology to achieve a 20% reduction in fuel usage [5].

A hybrid-electric shipboard propulsion topology is provided in Fig. 1.3. Shipboard power ratings are generally higher than that of aircraft, so the battery storage can

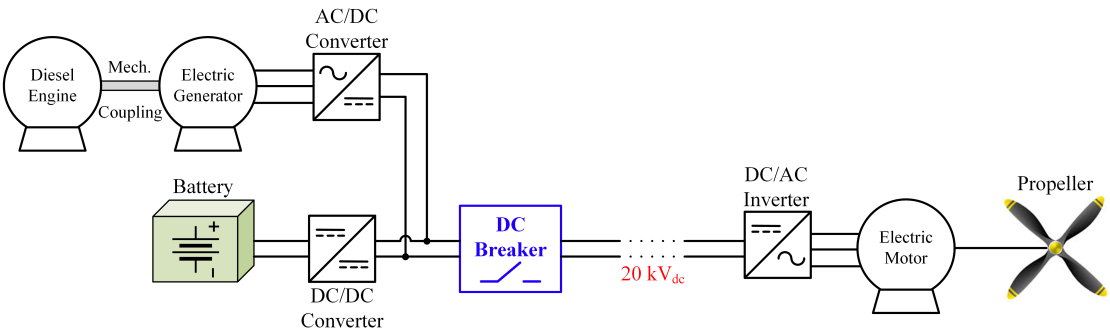


Figure 1.3: General topology of a hybrid-electric shipboard propulsion system

be supplemented with diesel generators. While similar, the main difference between electrified aircraft and shipboard is the much higher DC bus voltage and higher power rating. In this instance, the DC bus can also be used to easily power electrified loads such as electric motors, rail guns, sonar, and more. Examples of such hybrid electric ships include the ABB hybrid ferry in the Norweigan fjords [9] and the commissioned ABB hybrid ferry in Maine [10, 11]. Both are plug-in hybrid ships, meaning that the battery storage can be pre-charged between voyages and the ship can choose between using electric energy or diesel engines. With this technology, the Maine ferry is expected to reduce up to 800 tons of carbon emissions yearly.

1.3 DC Circuit Breakers

In electric distribution, circuit breakers are the key components that protect the entire system from damage. If a short circuit fault occurs, then a large current that is orders of magnitude larger than rated load current will flow through the system. This could easily damage the power source and any sensitive components. For this reason, it is crucial to have adequate protection that is fast, efficient, and high power density.

In AC distribution, there are solutions that work well and provide full protection and fault isolation. Conventional mechanical circuit breakers are sufficient for AC systems. This is due to nature of AC voltages and currents. Since the system oscillates at a set frequency (e.g., 50 Hz, 60 Hz, or higher), then the inductance in the line is a significant choke that controls the speed at which fault current magnitudes increase. For mechanical circuit breakers during interruption operation, an arc will be established across its separating contacts due to the system inductance. Through this arc, the system current will continue to flow and the circuit cannot be isolated. If

the current were to become zero, then the arc would quench, the separated contacts would build up their dielectric strength, and the circuit would achieve isolation. An AC system naturally has zero crossings twice every cycle (e.g., every 8.3 ms for 60 Hz), so there is no need to artificially induce a current zero. For these reasons, an AC circuit breaker can have an interruption speed on the order of several tens of milliseconds and provide sufficient circuit protection.

Contrasted to AC, DC current is much more difficult to interrupt. The distribution frequency is, ideally, zero. This means that the system's inductive impedance is minimized, so fault currents tend to increase in magnitude rapidly. Current is also constant in DC, so there is no natural zero crossing to extinguish arcs. This introduces the challenge of artificially inducing a current zero, and it is especially important for quenching arcs between mechanical contacts during interruption. For these reasons, it is critical to interrupt a DC fault within a few milliseconds [12].

The basic branch structure of a DC circuit breaker is provided in Fig. 1.4. Typically, DC breakers consist of three parallel branches. The conduction branch is the main branch, and all current flows through this during normal load conditions; all other branches are essentially open circuits in normal operation. Since no other branches are conducting at this time, the power losses of the conduction branch de-

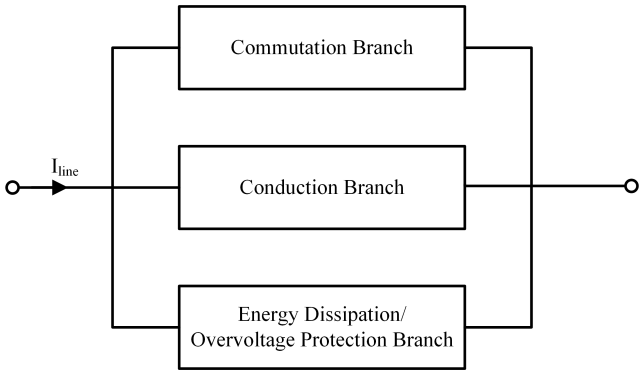


Figure 1.4: Typical branches of a generic DC circuit breaker

termine the breaker's efficiency. The remaining branches are used only to assist in interruption. During a fault, the conduction branch starts to isolate (e.g., opening metallic contacts, shutting off devices, etc), and the commutation branch creates the current zero crossing in the conduction branch. This transfers the fault away from the conduction branch and into the commutation branch for a short while. This is usually accomplished by injecting current into the conduction branch or by providing a low resistance path for the fault current. This allows the conduction branch to achieve isolation. Since the system inductance is charged from the fault current, an overvoltage will be induced across the breaker upon the attempted current interruption. This is referred to as "inductive kick." The energy dissipation branch clamps this overvoltage such that it does not damage the breaker. In doing so, it also dissipates residual energy leftover in the system. Once completed, the fault has been cleared. Note that Fig. 1.4 displays typical branches. Some topologies have no need for these three distinct branches since one branch can perform a combination of functions. For example, a purely solid state breaker does not need a commutation branch since the solid state switches in the conduction branch are able to provide their own zero crossing. This will be explained in more detail in section 1.3.2.

In application, there is typically an additional mechanical breaker in series with the main DC circuit breaker. This extra breaker does not interrupt, but is simply a mechanical switch to provide total isolation and opens after the main breaker clears the fault.

On the other hand, it might be possible to design a power electronic converter such that it achieves fault tolerance. However, this is challenging and poses a risk when its microcontroller is tripped. This can happen if the circuit interfaces high electromagnetic interference (EMI). Considering the case of a basic two-level inverter

driving an electric motor, if the controller gets tripped then the inverter will be out of control. Since the inverter now has no control signals, it cannot stop the motor. It will then continue to spin and act as an uncontrolled generator. The high back electromotive force (back-EMF) derived from the high-speed motor will be rectified through the inverter's antiparallel diodes and charge the DC bus to a high voltage. This highlights the need for a separate circuit breaker to protect the system in events such as this uncontrolled generator faults. The DC circuit breaker operates independently of the other components in the system. The breaker decides whether or not a fault has occurred typically based on the line current [13]. Then the breaker acts and separates the fault from the source protecting the system. In the following subsections, the pros and cons of the existing DC breaker technologies will be reviewed.

1.3.1 Passive Resonant Mechanical DC Circuit Breaker

The topology of a passive resonant mechanical DC Breaker (PRMDCB) is shown in Fig. 1.5. This topology is most similar to the conventional circuit breakers used in AC distribution. The main conduction branch is comprised of a mechanical switch. Usually, this is a vacuum interrupter (VI) for MVDC systems, but it is possible to use other interrupting mediums such as sulfur hexaflouride. This branch is responsible for conducting all load current and creating an open circuit during a fault. Next, the commutation branch contains a passive LC resonating circuit. Once the mechanical switch starts to separate its contacts during a fault, an arc is established between them with a voltage drop. This voltage drop causes the LC resonant circuit to charge and oscillate at its resonant frequency. Once the peak oscillation is equivalent to the magnitude of the fault current, a current zero is achieved in the switch and the

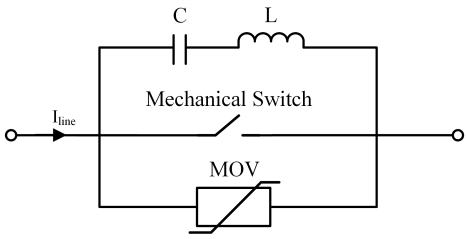


Figure 1.5: Mechanical DC circuit breaker topology

arc quenches. Next the energy dissipation branch, a metal oxide varistor (MOV), clamps the overvoltage and dissipates all residual energy. It should be noted that the MOV only conducts negligible leakage current until its knee voltage is surpassed by the induced overvoltage. At which point it becomes a very small resistance. This conducts the large fault current and clamps overvoltages. It is possible to use other devices in the energy dissipation branch, such as an RC snubber, but MOVs offer the best voltage protection comparatively.

Due to the mechanical switch being the sole component in the conduction branch, this breaker excels at efficiency. This is due to the ultra-low resistance of the mechanical contacts (e.g., approximately 1 $\mu\Omega$). However, the time needed to actuate the mechanical contacts results in poor interruption speeds on the order of 10-100 ms [14]. This is further exacerbated by the time needed to build up the resonating current in the passive LC circuit. The PRMDCB performs well in efficiency, simplicity, and cost, but the sluggish interruption speed makes this topology unsuitable to safely provide protection in DC applications.

1.3.2 Solid State DC Circuit Breaker

For faster interruption speeds, a solid state DC breaker (SSDCB) can be utilized. The topology of the SSDCB is given in Fig. 1.6. In the main conduction branch is a set of solid state semiconductor switches connected in series and parallel depending

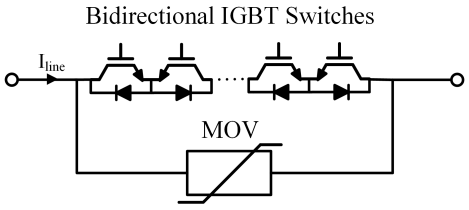


Figure 1.6: Solid state DC circuit breaker topology

on the rated voltage and current requirements. These devices are traditionally silicon (Si) based such as insulated-gate bipolar transistors (IGBT) or thyristors. But recent advancements in wide bandgap semiconductor technologies allow the use of silicon carbide (SiC) or gallium nitride (GaN) metal-oxide-semiconductor field-effect transistors (MOSFET). Under normal load operation, these devices are held on and all load current flows through them. Notice that there is no need for a commutation branch in this circuit breaker. This is because the semiconductor devices do not generate an arc when they are switched off. In other words, the devices create their own zero crossing. Once the switches are off and have achieved current zero in the conduction branch, the MOV in the energy dissipation branch clamps the resulting overvoltage and dissipates residual energy.

The main benefit of the SSDCB is the ultra-fast interruption speed. Since the current is interrupted by simply turning off the semiconductors, the breaker can achieve a fault interruption speed within 100 μs [15–17]. However, the semiconductor switches' on-state resistive losses result in relatively lower efficiency. They also need a cooling system to cope with the significant losses. These two problems are somewhat mitigated by opting for solid-state DC circuit breakers.

1.3.3 Conventional Hybrid DC Circuit Breaker

The conventional hybrid DC breaker (HDCB) is a combination of the solid state and mechanical breakers. Its topology is provided in Fig. 1.7 [18]. The conduction branch is a combination of both semiconductor switches, usually IGBTs, and a mechanical switch. In doing so, the amount of IGBTs in the conduction path are reduced. Rated load current flows through this branch during normal operation. During a fault, the mechanical switch is commanded to open, and an arc is established that continues to conduct fault current. To achieve a current zero, the conduction path IGBTs are switched off while the commutation path is switched on. This provides a lower resistance path for the current to flow through, and the fault is redirected from the conduction path. This induces a current zero, and the arc between the mechanical contact quenches. Once the contacts have built up their dielectric strength, the commutation path can then switch off. At this point, the fault is interrupted and an overvoltage is induced across the breaker. This is clamped by the MOV in the energy dissipation branch and all energy leftover in the system is dissipated.

The HDCB is a compromise between the efficiency of the PRMDCB and the speed of the SSDCB. Since the IGBTs are paired with a mechanical switch in the conduction branch, the number of IGBTs needed in the path is reduced. The rated voltage is

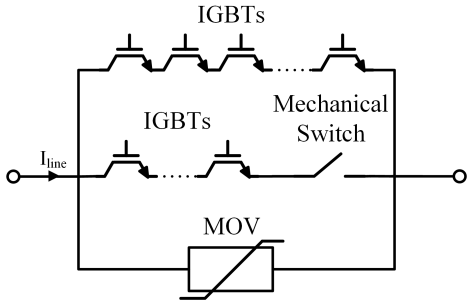


Figure 1.7: Conventional hybrid DC circuit breaker topology

split between the mechanical switch and the IGBTs. The normal operation on-state resistance is then minimized resulting in higher efficiency than the SSDCB. Also, fast-switching IGBTs achieve zero current crossing much faster than the purely mechanical PRMDCB. However, the interruption speed is still limited by how quickly the actuator of the mechanical switch can open its contacts. Therefore, the interruption speed is on the order of several ms. The IGBTs are still present in the conduction path and have non-negligible losses that affect efficiency. The compromise is an improvement, but the interruption speed is too slow for DC systems and the efficiency is still undesirable due to the conduction path IGBTs.

1.4 Objectives

This work's objective is to develop ultra-fast, efficient, compact, reliable, and low-cost circuit breakers that meet the needs of emerging MVDC distribution for electric aircraft and shipboard applications. Two breaker topologies will be studied: a resonant current source based hybrid breaker and a high temperature fault current limiter based solid state breaker. Both breakers will be designed by leveraging the advantages of the emerging wide bandgap switches, such as GaN and SiC MOSFETs, and will be electrically and thermally modeled and simulated to verify the function and feasibility of the two breakers.

1.5 Outline of Thesis

The outline of this thesis is provided as follows:

Chapter 1 includes the necessary background on the motivation of MVDC distribution and its role in electrifying transportation. The concept of DC circuit breakers is introduced, and various common breaker topologies are reviewed.

Chapter 2 introduces the resonant current source converter based DC circuit breaker. Its topology, RLC circuit, operating principle, and control scheme is detailed.

Chapter 3 includes the simulation models of the different subsystems of the resonant current source DC circuit breaker such as the resonant converter based on SiC MOSFETs, arc modeling for the VI, and metal oxide varistor models. Simulation results are provided to confirm the function of the circuit breaker during fault interruption.

Chapter 4 details the concept of the high temperature superconductor fault current limiter based solid state DC breaker. An overview of high temperature superconductor technology and fault current limiter is provided along with the breaker topology and its operating principle.

Chapter 5 describes the simulation models used to simulate the high temperature superconductor fault current limiter based solid state breaker. Models include the SiC-based solid state breaker, high temperature superconductor cables, transmission line, and overvoltage mitigation. Simulation results are provided to demonstrate the effectiveness of the combination of fault current limiter with solid state breakers. A discussion is also given over the power law model for the high temperature superconductor cables.

The work is concluded in Chapter 6 to summarize the performance of the two breaker concepts based on the investigation presented in this thesis. Future work to further improve and verify the performance of these two DC circuit breakers is also discussed.

1.6 Publications

Listed below are the journal and conference papers that were published based on the work to be introduced in this thesis, including:

- T. Arvin, J. He and N. Weise, "Modeling and Simulation of an Ultra-Fast Resonant DC Circuit Breaker Based on Current Source Module," Vol. 6 No. 1, Transactions on Techniques in STEM Education, Oct-Dec 2020.

- T. Arvin, J. He, N. Weise and T. Zhao, "Modeling and Simulation of a 20kV Ultra-Fast DC Circuit Breaker for Electric Shipboard Applications," 2020 IEEE Transportation Electrification Conference & Expo (ITEC), 2020, pp. 795-801.

- T. Arvin, J. He, and K. Waters "Solid-State DC Circuit Breaker Based on HTS Fault Current Limiter and SiC MOSFET Modules," accepted by 2022 IEEE Transportation Electrification Conference & Expo (ITEC), 2022.

Chapter 2 Resonant Current Source-Based Hybrid DC Breaker

2.1 Circuit Description

The conventional hybrid DC breaker (HDCB) is a compromise between the benefits and drawbacks of the solid state and mechanical breakers. The efficiency is improved over the solid state breakers, and the interruption speed is improved over the mechanical breakers. However, the losses are not negligible and the interruption speed is not sufficiently fast for DC protection. To improve upon the conventional HDCB, the semiconductors must be fully removed from the conduction path and the actuator opening the mechanical contacts must be improved. The efficiency can be increased by using a high frequency solid state resonant current source (RCS) in the commutation branch. This removes all semiconductors from the conduction path leaving only the contact resistance of the mechanical switch (in the range of $\mu\Omega$). This eliminates their on-state losses during normal operation thus making losses negligible and efficiency high. Along with the high frequency RCS, the interruption speed is then improved by opening the mechanical contacts with a high speed actuator. In doing so, the breaker can interrupt faults much quicker than the conventional HDCB.

The high-level circuit topology of the resonant current source hybrid DC breaker (RCS-HDCB) is shown in Fig. 2.1. The sole component in the conduction branch is a vacuum interrupter (VI). This is operated by a fast-actuator that combines permanent magnets and Thomson coils to open the breaker within 500 μs. The commutation branch is made of one or many RCS modules. The RCS-HDCB uses a modular approach such that the individual sub-systems can be stacked. This allows

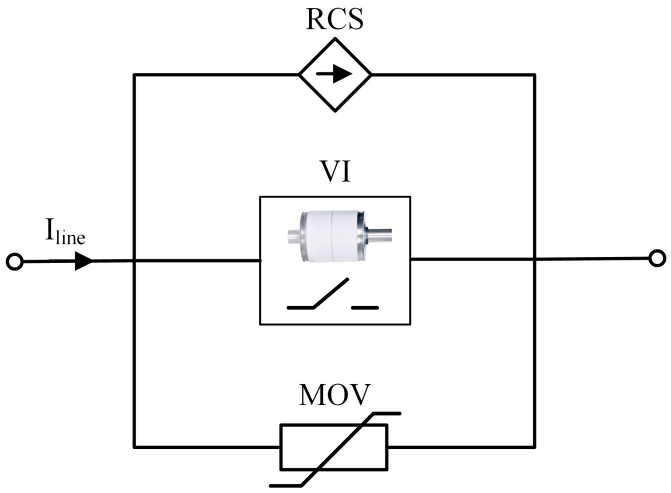


Figure 2.1: High-level topology of the RCS-HDCB

for scalability to any DC power application. The RCS module itself uses low-loss fast-switching wide bandgap (WBG) devices to enable high frequencies of resonant current. Not only does this enable fast ramping of the resonant current, it enables physically smaller inductors and capacitors inside the RCS. The final branch is the energy dissipation branch. Much like other breakers, the RCS-HDCB uses a metal oxide varistor device to clamp overvoltages and dissipate residual energies.

The applications of this breaker are shown in Table 2.1. In one case study, the aircraft application [19, 20] will use GaN transistors due to the lower DC voltage level (i.e., 2.4 kV). In another case study, the shipboard breaker [21] will use SiC MOSFETs due to higher voltage level (i.e., 20 kV). These devices are used in lieu of conventional Si MOSFETs since they feature higher power density, lower switch losses, higher operating temperature capability, and faster switching speeds. This enables the RCS to have increased power density and achieve high frequencies of resonance with lower losses. For voltage protection, the aircraft application is able to use an off-the-shelf MOV since its voltage is relatively lower. However, a surge arrester (SA) (essentially many MOV disks) must be used for the shipboard application to

Table 2.1: Intended Applications of the RCS-HDCB

Category	**Aircraft**	**Shipboard**
Rated Voltage	2.4 kV	20 kV
Power	2.5 MW	20 MW
Target Efficiency	99%	99%
Interruption Speed	$\leq$500 μs	$\leq$500 μs
Lifetime	40k cycles, 35 yrs	40k cycles, 35 yrs
Cooling	Passive	Passive

account for the increased voltage and system inductance.

2.1.1 Topology

The detailed topology of the RCS-HDCB is provided in Fig. 2.2. The main conduction branch is composed of a low-resistance VI. The energy absorption branch is composed of a MOV or a SA. The commutation branch either has a single RCS or multiple modules stacked. Stacking the modules in parallel increases the maximum fault current magnitude that the branch can safely commutate. For example, the two RCS modules in Fig. 2.2 effectively double the fault current capabilities without adding more stress on the individual modules. The modules themselves are H-bridge converters driving an LC resonator fed with a capacitor voltage source, C_s. The H-bridge oscillates its source voltage at the resonant frequency of the resonant inductors, L, and capacitors, C. This allows the building of resonant current and will be explained in more detail in Section 2.1.2. Low-voltage devices can be leveraged since the RCS source voltage is much lower than the DC bus voltage. This decreases the cost of each RCS module and allows them to be physically and electrically smaller. The main requirement is that the WBG devices must have high current carrying capabilities, especially pulse current, for fault commutation.

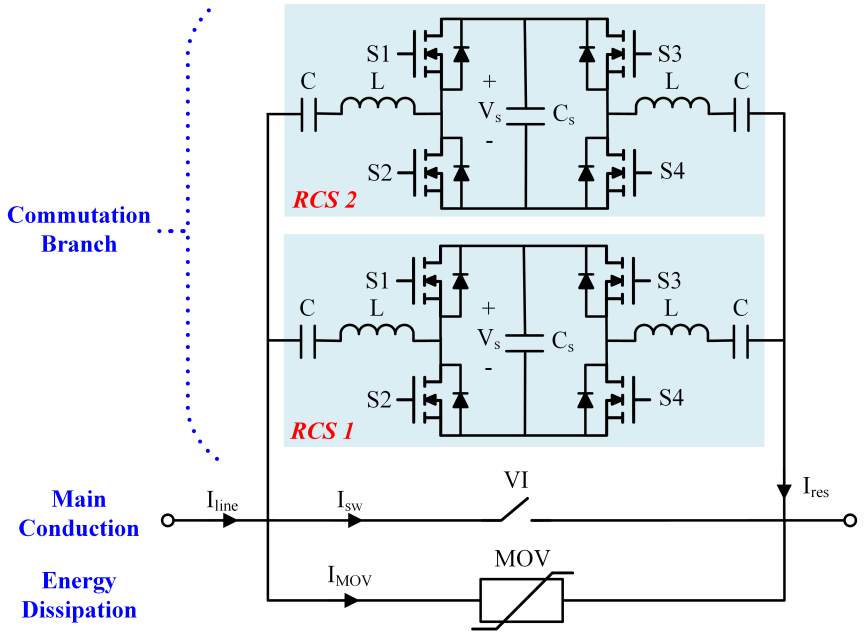


Figure 2.2: Circuit topology of the RCS-HDCB

2.1.2 Operating principle

During normal operation, the nominal load current flows through the conduction path of the VI. Since the VI has extremely low contact resistance, the losses here can be neglected, enabling high energy efficiency. At this point, the RCS modules do not conduct and the MOV in the dissipation branch is a high impedance. Only negligible leakage current flows through the MOV, so both branches can be regarded as essentially open circuits. Once a fault occurs (i.e., the DC bus is shorted), an abnormally high current will flow through the conduction branch. This faulty current is orders of magnitudes higher than the nominal load current. Its rise time is limited by the line inductance and its magnitude by the line resistance. The fault is detected and the VI is commanded to open its contacts. This takes time to fully separate, and an arc is established between the contacts. It provides a low-resistance path for the current to continue to flow and will continue until the arc is quenched by a zero current.

The main function of the commutation branch is to induce the current zero in the conduction branch. The current flowing through the conduction path is provided by equation 2.1.

$$i_{sw} = i_{line} - i_{res} \tag{2.1}$$

where:

- i_{sw}: conduction branch current

- i_{line}: line current

- i_{res}: commutation current

It is apparent from this equation that the current through the VI will be zero when the magnitude of the commutation current, i_{res}, is equivalent to the magnitude of the fault current, i_{line}. In doing so, an artificial zero crossing is achieved within the VI to quench the arc.

To induce the zero crossing, the RCS is controlled to build a fast-ramping oscillating current to oppose the fault current. An example of a typical RCS waveform is provided in Fig. 2.3. The WBG switches in the H-bridge are controlled to output a resonant current by oscillating the voltage from the pre-charged source capacitor,

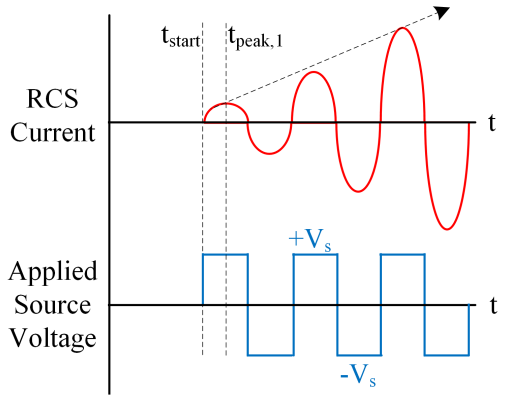


Figure 2.3: Typical waveforms generated by RCS

C_s, at the resonant frequency of the resonant inductors and capacitors. The resonant frequency is calculated by the Equation 2.2. It should be noted that the resistance of the RCS is determined by the parasitic or on-state resistances of the RCS components themselves. Resistance limits the peak resonant current of the RCS module and is thus desired to be minimal.

$$\omega_d = \sqrt{\frac{1}{LC} - \frac{R^2}{4L^2}} \tag{2.2}$$

$$\alpha = \frac{R}{2L} \tag{2.3}$$

where:

- ω_d: damped radian frequency (rad/s)
- L: equivalent inductance of RCS (H)
- C: equivalent capacitance of RCS (F)
- R: equivalent resistance of RCS (Ω)
- α: damping constant

Once excited with alternating voltages, the resonant inductors and capacitors will create a ramping oscillating current that ramps approximately linearly with time. Each half period of resonance is referred to as a reversal since the resonating current alternates sign. Depending on the choice of source capacitance, resonant inductance and capacitance, and the on-state resistance of the WBG devices, the magnitude of the oscillating current will eventually saturate and decay at a high number of reversals. The choice of the source capacitor is the most significant in terms of saturation since it can only store certain amount of charge, so a sufficiently high capacitance must be chosen. It is preferable that the RCS achieves current zero within the linear growth

portion of its current. Typically this is within a few tens of reversals. After many reversals, the current saturates, and there are diminished returns in the peak-to-peak current gain. The time at which the first peak RCS current occurs, and all subsequent, are given by Equations 2.4 - 2.5.

$$t_{peak,1} = \frac{1}{\omega_d} \arctan(\frac{\omega_d}{\alpha}) \tag{2.4}$$

$$t_{peak}(n) = (n-1)\frac{\pi}{\omega_d} + t_{peak,1} \tag{2.5}$$

where:

- $t_{peak,1}$: 1st reversal peak (s)
- $t_{peak}(n)$: n_{th} reversal peak (s)
- n: corresponding peak number

The magnitude of each of these resonant current peaks is given in Equation 2.6.

$$i_{peak}(n) = B(1)e^{-\alpha t_{peak,1}} \sin(\omega_d t_{peak,1}) \tag{2.6}$$

$$B(n) = \frac{V_d(-1^{n-1}) - V_c(n-1)}{L\omega_d} \tag{2.7}$$

where:

- $i_{peak}(n)$: magnitude of n_{th} reversal peak current (A)
- $B(n)$: underdamped ringing coefficient
- V_d: H-bridge's DC bus voltage (V)
- V_c: initial capacitor voltage (V)

The current saturation is largely determined by the source capacitor, since the voltage across the capacitor will deplete over many reversals. The equations above

assume an ideal voltage source instead of a source capacitor, so the peak-to-peak current gain is not attenuated by the source capacitor's limited stored charge. With an ideal voltage source, the current saturation is controlled only by the impedance of the LC resonating circuit. Finally, the capacitor voltage stored at the end of each reversal is found by the Equation 2.8.

$$V_c(n) = \frac{B(n)}{C}\frac{\omega_d}{\alpha^2 + \omega_d^2}(e^{-\alpha\frac{\pi}{\omega_d}} + 1) + V_c(n-1) \tag{2.8}$$

where:

- $V_c(n)$: voltage stored in capacitor after the n_{th} reversal (V)

Larger magnitudes of commutation current can be achieved by either increasing the source voltage of the H-bridge or by utilizing more current reversals. Increasing the number of reversals in turn decreases the required initial source voltage of the H-bridge and vice versa. However, there is a limit to the amount of reversals possible. This is constrained by the rated voltage of the WBG devices, the rated current, and the saturation rate of the RCS. There is a tradeoff between the number of reversals and the peak junction temperature of the MOSFETs. Generally, the more reversals performed means a higher junction temperature. Using too few reversals would result in an initial source voltage that exceeds the voltage ratings of the MOSFETs. A low number of reversals would also drastically increase the peak-to-peak resonant current gain. This would put uneven wear on the WBG devices and have a high temperature differential per reversal. In doing so, it would negatively affect the reliability and lifetime of the RCS module.

Once the RCS module(s)' resonant current exceeds the magnitude of the VI current, the zero crossing is successfully achieved. This provides an opportunity for the

arc to quench inside the VI. In doing so, the contacts become an open circuit and gradually rebuild their dielectric strength. The fault has now been interrupted, and the energy dissipation mode begins. The RCS module ceases resonance, and the fault current flows briefly through the resonant components and the anti-parallel diodes of the H-bridge. This serves the dual purpose of commutation and recharging the source capacitor. After interruption is completed, an overvoltage rapidly builds across the breaker due to the attempted interruption in the system inductance's current.

If the breaker did not have overvoltage protection, it would likely become damaged by the excessive voltage, or the arc could re-establish itself which would resume the fault. Since mechanical contacts are utilized and the WBG devices are decoupled from the full fault voltage, this topology is not as sensitive to overvoltages as others such as the SSDCB or conventional HDCB. The duty of the MOV or SA is to clamp this overvoltage such that it is within a safe limit for the the breaker to endure. The MOV is an extremely nonlinear device. At relatively low voltage, the resistance is extremely large, but the resistance becomes extremely low for high voltages. This transition occurs at the knee voltage of the particular MOV device. In this low impedance state, the MOV clamps the overvoltage and dissipates the residual energy stored in the system impedance and resonant components of the H-bridge. The time it takes to expend the energy depends on the amount stored and the total impedance still present in the circuit. Once all leftover energy is dissipated, the voltage across the breaker relaxes to the nominal DC bus voltage of the distribution system, and the MOV resumes as a near-open circuit high impedance. At this point, the fault can be considered fully isolated.

Note that this design can handle bidirectional current in the systems. A positive or negative directed current can easily be detected by employing a current sensor

in the main conduction path. The VI and MOV are naturally bidirectional, and the RCS can be utilized to compensate for whichever direction the fault current flows. By inverting the related pulse width modulated (PWM) signals, the pulsating commutation current can be reversed. This produces a negative or positive peak reversal for a correspondingly positive or negative fault current. In a simpler scenario, the RCS can instead utilize one extra reversal without the need to modify control signals. The current zero would then occur on the next reversal. Either approach can be used to provide interruption of bidirectional current. After the fault is interrupted, then the current would flow briefly through the antiparallel diodes of either S1 and S4 or S2 and S3, depending on its direction.

2.1.3 Controls

The RCS components require an alternating voltage pulse in order to resonate charge between the inductor and capacitor. This builds a constantly ramping oscillating current through the RCS. Likewise, the oscillating of the RCS must be timed in tandem with the VI. If the RCS were to attempt current interruption before the VI contacts were fully open, it would be more likely for the arc to re-establish. This presents the danger of resuming the fault and failing interruption. Mechanical contacts have the greatest dielectric withstand capability when they are the farthest apart, so the peak reversal current must be timed at the moment when the VI is fully actuated.

Given a desired number of RCS reversals, the time at which the RCS must start resonating relative to when the VI starts to open can be calculated with Equation 2.9-2.10. This equation coordinates the peak reversal with the instance the mechanical contacts are fully open.

$$t_{res} = (m-1)\frac{\pi}{\omega_d} + \frac{1}{\omega_d}\arctan(\frac{\omega_d}{\alpha}) \tag{2.9}$$

$$t_{start} = t_{VI} - t_{res} \tag{2.10}$$

where:

- t_{res}: time to complete the desired number of reversals (s)

- t_{start}: time delay to start RCS resonating after VI starts opening (s)

- t_{VI}: time it takes to fully open VI (s)

- m: number of current reversals desired

The necessary source voltage to pre-charge C_s can be estimated using the Equations 2.11 - 2.15. Similar to the approach in [22], these equations use the envelope of the resonant current to calculate each peaks' magnitude. It works well for reasonable reversal numbers (e.g., within a few tens of reversals). In other words, the approximation is accurate enough for the linear region of resonant current growth but less so for the saturation region. This is derived via the provided equations, the RLC transfer function, and convenient assumptions about the shape of the source capacitor discharging voltage during interruption. The approximation tends to overestimate, so the voltage can be tuned exactly via a trial-and-error method in simulation, or a correction factor can be added given experimental testing.

$$Z_{LC} = \sqrt{\frac{L}{C}} \tag{2.11}$$

$$I_o = \frac{1}{Z_{LC}} \tag{2.12}$$

$$I_{LC} = \frac{f_d}{30C_s Z_{LC}\omega_d^3}\left(30I_o t_{res}^2\omega_d^3 + 60I_o f_d \sin(2\omega_d t_{res})\right) +$$

$$\frac{f_d}{30C_s Z_{LC}\omega_d^3}\left(15I_o\omega_d \cos(2\omega_d t_{res}) + 108C_s t_{res}\omega_d^3\right) -$$

$$\frac{f_d}{30C_s Z_{LC}\omega_d^3}\left(40I_o f_d t_{res}^3\omega_d^3 - 60I_o f_d t_{res}\omega_d \cos(2\omega_d t_{res})\right) \tag{2.13}$$

$$gain_{RCS} = bI_{LC} \tag{2.14}$$

$$V_s = \frac{I_{fault}}{gain_{RCS}} \tag{2.15}$$

where:

Z_{LC}: characteristic impedance (Ω)

- I_o: RCS current with V_s=1 V

- I_{LC}: approximate RCS current gain per volt of V_s after t_{res} seconds (A/V)

- f_d: resonant frequency of RLC circuit (Hz)

- $gain_{RCS}$: gain of entire commutation branch (A/V)

- b: number of RCS modules in parallel

- V_s: estimated voltage to pre-charge C_s (V)

- I_{fault}: expected fault current magnitude (A)

The RCS is controlled with a square wave signal of 0.5 duty cycle to generate the ramping resonant current. Switches S2 and S3 can be turned on to create a positive sinusoidal pulse and vice versa for S1 and S4. The corresponding gate pulses and resulting current can be seen in Fig. 2.4. Because the current injected into the VI is the inverse of the resonant current, the maximum peak of resonant current must occur in the positive portion of the sinusoidal waveform to cancel the fault current.

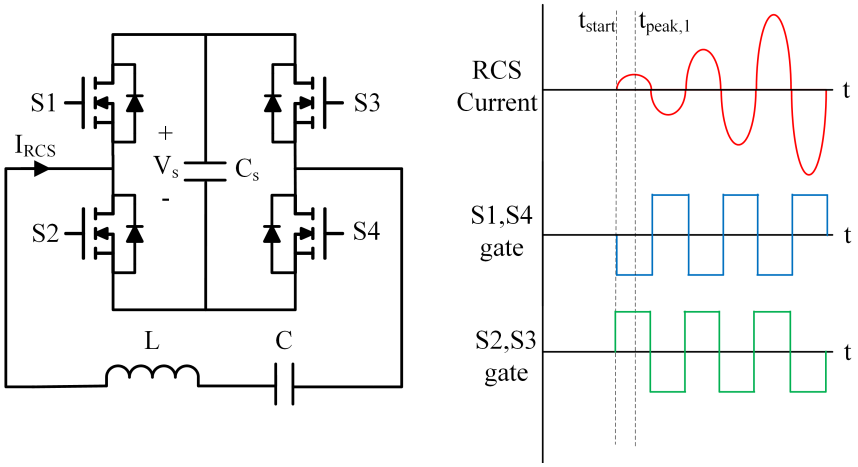


Figure 2.4: Typical control signals to generate resonant current in the RCS

Table 2.2 shows the criteria and resulting phase delay of the waveforms for timing the peak pulse.

Using a simple square wave control scheme, as detailed, has benefits in simplicity and loss management. Since the gates of the MOSFETs are turned on and off at the instance each reversal is completed, then the MOSFETs are inherently zero-current switching. In other words, the switching losses are minimized since little to no current is flowing through the MOSFET during its switching event. All losses are therefore associated with conduction losses. This increases the capabilities of the RCS since the MOSFET's junction temperature will not rise quickly.

Note that PWM strategies could theoretically be implemented with the H-bridge converter [23]. This could regulate the RCS current to a specific magnitude. Current regulation may also be theoretically achieved by leveraging the LC transfer function gain at different frequencies. If the magnitude of the resonant current could be held

Table 2.2: RCS Pulse Delay According to Reversals

Reversals	**Starting Pair**	**S1, S4 Phase Delay (s)**	**S2, S3 Phase Delay (s)**
Even	S1, S4	0	π/ω_d
Odd	S2, S3	π/ω_d	0

at the magnitude of the fault current, then the zero-current-crossing would be longer lasting and allow the mechanical contacts more time to build dielectric withstand. This would further decrease the likelihood of the arc re-establishing or restriking. However, PWM or variable frequencies would intersperse switching events across each reversal. This would drastically increase switching losses due to the large currents. The main obstacle in using PWM would be the management of these switching losses. Therefore, the resonant frequency 0.5 duty cycle control scheme described earlier in this section is used for its zero-current switching characteristics.

2.2 RLC Sizing

The equivalent series RLC circuit network for the RCS is given in Fig. 2.5. For an RLC circuit, there are three basic responses: underdamped, overdamped, and critically damped. All are classified according to how much damping or resistance present in the circuit. Underdamped circuits exhibit harmonic ringing, and overdamped or critically damped circuits slowly approach a steady state value with no ringing. The goal of this inverter is to create a continuously growing ringing current, so we must create an underdamped circuit for the RCS. In other words, we want to minimize the amount of resistance present in the series RLC network. In fact, it is counter-productive to have damping since it decreases the peak-to-peak current gain. Therefore, the resistance in our circuit is considered as the parasitic on-state resistance of the MOSFET switches, R_{on}. Since WBG devices are used, this is typically

Figure 2.5: Equivalent RLC circuit of the RCS

very small especially since multiple switches are used in parallel to increase their current capabilities. The source capacitance, C_s, is much greater than the capacitance of the resonant capacitor. Therefore, it does not have significant effect on the resonance of the circuit.

Fig. 2.6 shows the transfer function of the RLC network about the resonant frequency of 100 kHz for different impedances of L or C. The transfer function does not change at resonance, since the impedance of the RLC circuit is purely resistive, but increasing the impedance of the LC portion controls the current-over-voltage gain at all other frequencies. Presumably, as mentioned in Section 2.1.3, the gain at other frequencies could theoretically be utilized to regulate the RCS current. The main drawback to this approach is the substantial switching losses.

The peak magnitude at each reversal is shown in Fig. 2.7 for many reversals. These are compared with different combinations of LC impedance. Increasing the impedance controls the ramping rate of the RCS current. With greater impedance, the current

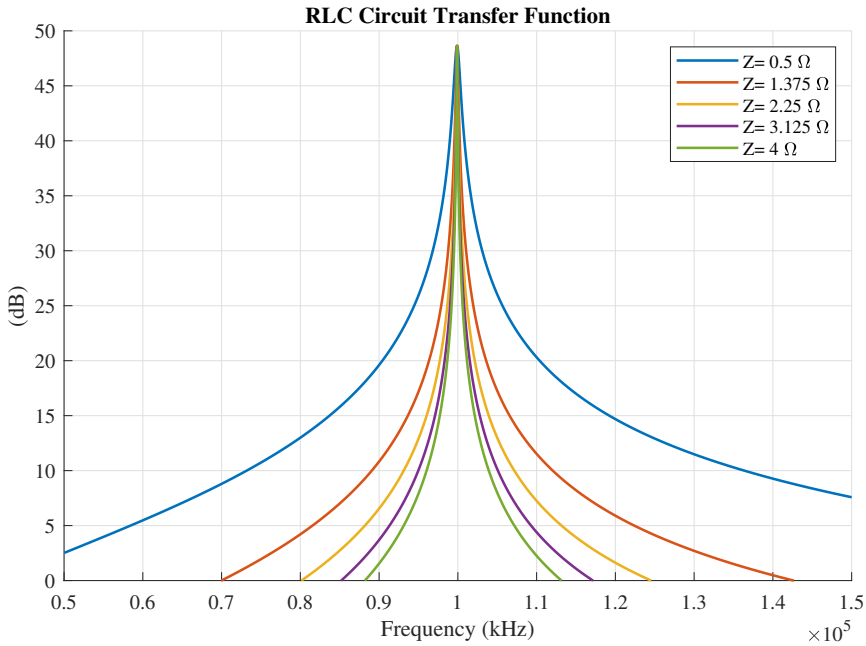


Figure 2.6: Transfer function of RLC network with different LC impedances

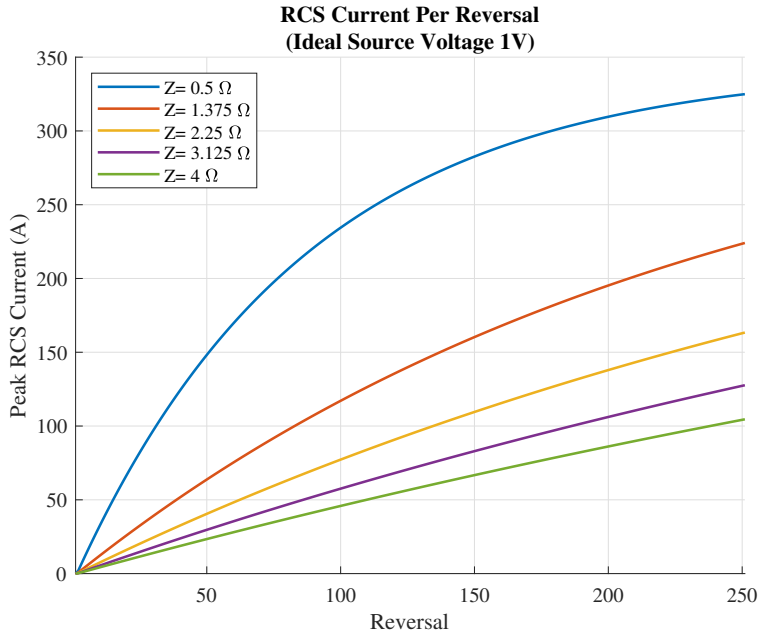


Figure 2.7: RCS reversal peak magnitude with different LC impedances

ramps less quickly but sustains longer linear growth. With lower impedances, a high ramping rate is possible, but the current saturates much more quickly. The high current differential may negatively affect electromagnetic interference and device lifetime. For future studies, the impedance of the RCS should be optimized against parameters such as device lifetime, peak device junction temperature, power density, and speed of interruption. For the purposes of this work, the impedance of 1.59 Ω is chosen as sufficient for its relatively quick ramping and sufficient linear growth before saturation. At 100 kHz, this impedance results in an equivalent inductance of 2.53 μH and a capacitance of 1.00 μF. Using the impedance, other inductances and capacitances can be easily calculated for any desired resonant frequency.

2.3 Conclusion

An improved hybrid DC circuit breaker is introduced in this chapter, which is based upon a solid state RCS to achieve ultra-fast induction of current-zero crossings. The

RCS leverages the fast-switching WBG MOSFETs to achieve high frequencies of resonance. The control strategy of the RCS module is introduced to induce the current zero and quench the arc. The mechanical switch, a VI, is utilized as the sole component in the conduction branch to achieve high efficiency. To improve interruption speed, the VI is equipped with an actuator that combines permanent magnets and Thomson coils. For overvoltage mitigation during the fault interruption, a MOV is used for aircraft applications of 2.4 kV, and a SA is used for 20 kV shipboard. Combining this technology, the proposed breaker concept can interrupt faults within 500 μs. Modeling and simulation analysis will be presented in the following chapter to further investigate the performance of the improved hybrid DC circuit breaker.

Chapter 3 Modeling and Simulation of Resonant Current Source Based Hybrid DC Breaker

3.1 WBG MOSFET Modeling and Considerations

The thermal performance of the WBG MOSFETs are closely related to the maximum fault current capabilities of the RCS. Using information provided on the MOSFETs' datasheet, a thermal model can be developed such that the junction temperature of the devices can be monitored during fault interruption. This model, built in PLECS simulation software, takes into consideration the conduction losses, switching losses, and transient thermal impedance.

Since the source voltage of the WBG devices is decoupled from the DC bus, low voltage semiconductor devices can be utilized. This significantly reduces the number of devices and implementation cost. The main consideration for sizing the MOSFETs is having a sufficiently high current carrying capability. As a rule of thumb, the continuous DC current rating can be used to quickly compare different MOSFETs. For the 2.4 kV aircraft application, the EPC2022 GaN MOSFET (100 V, 90A continuous, 150°C) [24] is used. Three parallel combinations of two in-series devices are used per leg of the H-bridge to give a maximum source voltage of 200 V. For the 20 kV shipboard application, the Cree CAS325M12HM2 SiC MOSFET half-bridge module (1.2 kV, 256 A continuous, 175°C) is simulated [25]. In a physical application, this choice has the added benefit of decreased parasitic inductance between MOSFET connections due to its modularity, and the half-bridge structure lends convenience to building the H-bridge. Two half-bridge modules in parallel are used on each side of

the H-bridge to increase the peak resonant current capabilities.

The lifetime and efficiency of the circuit breaker is dominated by its normal operation mode, so the MOSFETs lay dormant for most of the breaker's life. This mode is what determines the efficiency of the breaker since the losses during the fault interruption are small in proportion to breaker lifetime. Therefore, the losses during fault interruption are neglected. Instead, the objective is to ensure that a fault can be safely and reliably interrupted. There must be minimal damage or thermal stress to the components of the breaker. For this reason, the maximum junction temperature of the WBG devices is kept below $100°C$. The ambient temperature for the aircraft simulation is room temperature $25°C$, and the worst case scenario is simulated for shipboard at $50°C$.

Due to the nature of the resonant current, the MOSFETs switch at every current zero of the RCS. The losses of the devices are therefore dominated by conduction since the switching losses are minimized. There is a tradeoff between the number of reversals possible and the peak current. In general, larger numbers of reversals necessitates longer conduction times and higher junction temperatures. However, this also decreases the necessary source voltage as it allows more time for the RCS to build its current. This is beneficial when considering lifetime and its dependency on temperature swing. The higher the peak-to-peak current difference results in more drastic junction temperature swings and uneven junction temperature distribution among the semiconductor devices. This is detrimental to RCS lifetime and reliability. Therefore, a balance must be struck between reversal number and semiconductor device stress.

3.2 Vacuum Interrupter Modeling

The focus of this study is on the power electronic breaker circuits and how the other components behave as circuit elements. For this reason, it is important to model the effects of the VI from the circuit's point of view. It can be modeled behaviorally using a black box arc model. Other models can be used, but they vary widely in complexity and scope. The functional processes of VI operation and arcing are described in this section.

In DC conditions above a few tens of milliamperes and a few volts, an arc will be established between two current-carrying contacts when they separate [26]. Despite the separation, the arc will allow the current to continue flowing across from contact to contact. It is crucial that the arcing time be kept to a minimum. The longer an arc is allowed to form the more severe the damage on the contact's metal surfaces will be [27]. This negatively affects the lifetime of the vacuum interrupter.

When the mechanical contacts first separate, a molten bridge of contact material will connect the two surfaces. As the contacts continue to displace, the molten bridge will rupture and disperse metal vapor about the insulation medium (e.g., air, SF6, vacuum, oil). This metal vapor provides the conditions for the arc to initiate, especially in vacuum mediums. Afterwards, the arc may stabilize in the form of a diffuse or columnar arc. If the insulation medium is gas, then the arc will be composed of a low resistance plasma. Once the arc stabilizes, it will appear as a low resistance and low voltage drop to the circuit.

To quench this arc, a zero current crossing must be provided either naturally or artificially. Once this is achieved, the arc no longer has enough power to sustain itself and collapses. The behavior of the arc can be approximated using a variety of

different black box arc models, which will be explained in the next section.

3.2.1 Black Box Arc Model

The behavior of an arc is physically complex and stochastic in nature. However, there are models that simplify their processes such that they can be replicated and modeled as an electrical component. Black box arc models (BBAM) are one such model that make it possible to analyze how arcing affects the circuit (e.g., arc resistance, voltage transients, failures to quench, etc.). This type of modeling is commonly used in AC circuit analysis, but in other works it has been been applied in DC with desireable results [28–32]. Other arc models have also been proposed recently that are derived specifically for DC conditions [33].

There are many variants of the BBAM that can be used with varying fidelity, parameters, and complexity. In general, the BBAM models the arc as voltage dependent conductance. This can be conveniently manipulated using Ohm's law to make a voltage dependent current source. The two most popular models are the Mayr and Cassie. These are widely used, and many other models are based upon them. Mayr and Cassie models are based upon the energy conservation principle and use a series of convenient assumptions to derive their models [34]. The equation for the Cassie model is provided in Equation 3.1, and the Mayr is given in Equation 3.2.

$$\frac{1}{g}\frac{dg}{dt} = \frac{1}{\tau}\left(\frac{u_{arc}^2}{u_0^2} - 1\right) \tag{3.1}$$

$$\frac{1}{g}\frac{dg}{dt} = \frac{1}{\tau}\left(\frac{g u_{arc}^2}{P_{out}} - 1\right) \tag{3.2}$$

where:

- g: arc conductance (S)

- τ: arc time constant (s)

- u_{arc}: instantaneous arc voltage (V)

- u_0: arc reference voltage (V)

- P_{out}: cooling power of arc (W)

The two models can be considered complementary to each other. In other words, the models are suited for different arcing conditions due to their various assumptions. Other derivative models of the Mayr and Cassie exploit this relationship by combining the two to increase accuracy. The Mayr is most suited to high voltage arcs in the low current regime (<500 A and near current-zero). However, the Cassie model well suits high voltage arcs in the high current regime (>500 A and away from current-zero). By combining both, the resulting model can better represent arcs in both regimes. The Mayr and Cassie models are heavy simplifications of arcing behavior, so they tend not replicate experimental data well numerically. Instead, they are good qualitative models that describe arcs behaviorally and their effect on the circuit [35].

The motivation of other models that are derivative of Mayr and Cassie is to increase the quantitative accuracy. One such model that is commonly employed is the Schwarz model. In simplest terms, it can be thought of as a combination of both Mayr and Cassie. Both models can be found by manipulating certain parameters of the Schwarz model. The equation of the Swcharz model is given in Equation 3.3 [36].

$$\frac{1}{g}\frac{dg}{dt} = \frac{1}{\tau_0 g^{\alpha_s}}\left(\frac{g u_{arc}^2}{P_0 g^{\beta}} - 1\right) \tag{3.3}$$

where:

- P_0: constant factor of cooling power (W)

- τ_0: constant factor of arc time constant (s)

- α_s: exponential term of time constant

- β: exponential term of cooling power

The Schwarz model is flexible enough to perform well in both high and low current regimes. This increases its usefulness in studying arc establishment, stability, and quenching [37].

The assumptions involved in deriving this model are as follows:

- Arc temperature varies exponentially with time
- Arc cross-sectional area is constant
- Power loss in the arc column is constant
- Arc time constant and cooling power are exponential functions of conductance

The assumption that the arc time constant and cooling power are exponential is what enables this model to easily match experimental data. There is no physical justification for this relationship, but it is mathematically convenient and performs well in practice. For the upcoming simulation, the Schwarz BBAM is utilized for its relative simplicity and its ability to accurately model arcing behavior.

By varying the parameters of the model, the arcing behavior can be changed. τ_0 and α_s control the initiation time and delay of the establishing arc. P_0 and β are similar to u_0 in the Cassie model since they control the peak value of the overvoltage. By increasing this variables, the arc is easier to quench. τ_0 is also analogous to the insulation level of the mechanical contacts themselves while P_0 is to the maximum breaking capacity of the contacts [31, 32]. By varying these parameters, the model can be fitted to experimental arc data, or an arbitrary model can be established.

Table 3.1: Simulation Parameters of Schwarz Arc Model

Category	**2.4 kV Aircraft**	**20 kV Shipboard**
τ_0	30 ns	20 ns
α_s	0.20	0.20
P_0	50 kW	260 kW
β	0.30	0.50

In the upcoming simulation, a parameter sweep is utilized to tune the model for an arbitrary VI. The criteria is such that a stable arc is established upon contact separation and is quenched following a current zero crossing. The parameters of the Schwarz BBAM for each application are provided in Table 3.1

3.3 Overvoltage Mitigation Modeling

MOVs and SAs are nonlinear devices used to divert surges and clamp overvoltages. They are commonly placed in parallel with circuit breakers for clamping purposes. The RCS-HDCB is aimed at 2.4 kV aircraft and 20 kV shipboard distribution systems. A MOV can be used for the relatively lower voltage of aircraft, but an SA is a better fit for shipboard to account for the greater voltage and energy demands. A surge arrester is simply a stack of MOVs such that they can handle greater ratings. This section details the models used for the simulation of both the 2.4 kV and 20 kV MVDC systems.

Various models are available that can replicate the clamping and dissipative characteristics of the MOV. The device itself is made of stacked metal-oxide disks that are used to suppress transient overvoltages like lightning strikes or switching surges. By diverting or clamping these transients, vital or especially sensitive equipment is protected. In circuit breakers, the voltage clamping characteristics also have a dual purpose of preventing arc restrikes due to excessive voltage. The general current-

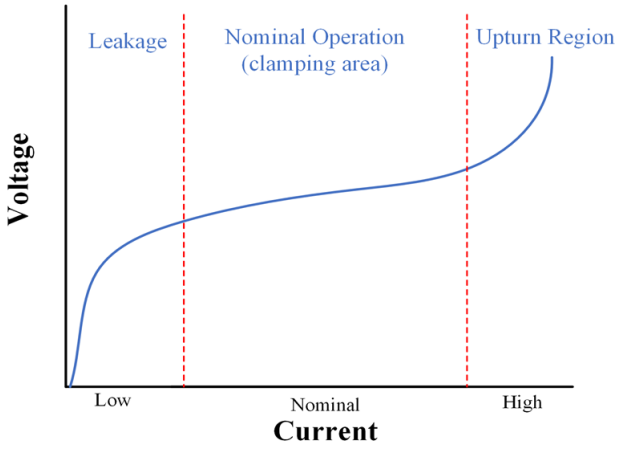
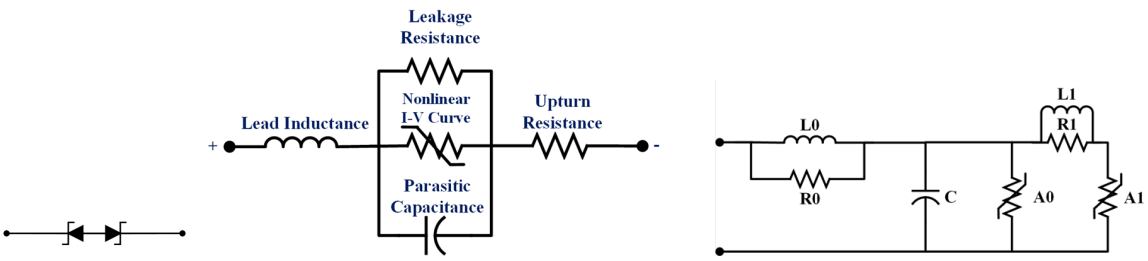


Figure 3.1: Generalized IV curve of MOV operating regions

voltage (IV) behavior of a MOV is represented in Fig. 3.1. In the low current regime, the MOV voltage is below the knee-voltage of the MOV and it appears as a large resistance. Only extremely small leakage current conducts through the device. At this stage, it appears as a near-open circuit. Beyond the knee voltage, the varistor quickly transitions to a low resistance and conducts significant current. This region is extremely nonlinear and is responsible for the MOV's voltage clamping ability. For very high currents and voltages, the MOV transitions to its upturn region. Here, the MOV no longer clamps but behaves as a low resistance of a few ohms.

Three models can be considered for the MOV, which are described in Fig. 3.2. A model of Zener diodes can approximate the behavior of the MOV. If two are used in anti-series and their reverse bias voltages are set to the clamping voltages of the MOV,



(a) Zener (b) IV model (c) IEEE model

Figure 3.2: MOV and SA Models

then the clamping behavior at those voltages is approximated. This model is shown in Fig. 3.2a. This approach has benefits in ease of implementation and low computational burden. However, the model neglects the leakage and upturn regions and only simulates a drastically simplified version of the nominal region. Also, MOV devices are frequency dependent, and there is an inherent body capacitance and current lag. The Zener diode approximation also neglects this. The other models, Fig. 3.2b and 3.2c, can be used to include the frequency dependency and all operational regions. The IV model approximates the current lag by using a lead inductance. For greater accuracy, the IEEE [38] or any of its modified models [39] can be used. However, the frequency dependency is not typically needed in switching surge studies since the pulse time is much longer than lightning surges, so the lag becomes insignificant. For this reason frequency dependence is not a requirement for circuit breaker modeling. The IV model, as detailed in [40–42], can be utilized in this case and is easily adapted from MOV datasheet information. The IEEE model is sized by using rated SA datasheet values, so it is more suited to modeling SAs than MOVs.

The 2.4 kV aircraft application uses a MOV, so the IV model is used. It consists of three branches: the leakage, nonlinear, and capacitive region. The lead inductance is responsible for the frequency dependence between current and voltage, and the series resistor corresponds to the upturn region. Typically, the upturn resistance is less than a few Ohms. The upturn resistance also tends to help with simulation convergence since it decreases unnecessary oscillations. The leakage resistance models the low-voltage regime and controls the magnitude of leakage resistance. This is a constant resistance and is set very high (1000 $M\Omega$). Next is the nonlinear region, and it is modeled using a linear-piecewise variable resistor. This is set with sampled data points from the provided IV curve on the MOV's datasheet. Once the knee

point of the MOV is passed, this resistance becomes small compared to the leakage resistor and it draws in significant current. The parasitic capacitance accounts for the structural capacitance of the MOV disks. In reality, this capacitance is also frequency dependent. However, it is neglected as a constant in this model. The lead inductance can be increased to model the current lag, but it is not directly needed for switching surge studies. Thus, it can be neglected.

MOVs are typically rated for lower voltages, so many would have to be layered in series and parallel to account for the increased demand of the 20 kV shipboard system. Therefore, a SA is instead utilized and modeled with the IEEE model. Some of the benefits of this model are the added fidelity and frequency dependence. The more drastic the surge current lags behind the SA voltage, the more severe the overvoltage will be. This is especially important in very fast transients (under a few μs), but it can be neglected for larger pulse duration (above several μs). The frequency dependence is accomplished through the RL filters R_0, L_0 and R_1, L_1. The voltage clamping is modeled by the nonlinear resistors A_0 and A_1. The RL filters are low-pass, so they appear as a low impedance for slow transients. This puts A_0 and A_1 in parallel. At fast transients, L_1 and R_1 are a high impedance so all surge current will flow through A_0. A_0 has higher voltage characteristics which leads to the more drastic overvoltage at fast transients. Finally, like the IV model, the structural capacitance, C, is approximated as constant. The IEEE model can easily be tuned for its rated 8/20 waveform for any SA. For instance, the ABB Polim-H (4.7 kV MCOV) [43] SA is modeled for the 20 kV simulation, so the model is tuned such that it replicates its rated 8/20 waveform at 20 kA. Considering the rated MCOV of this SA, five arresters are needed in series to accommodate the 20 kV DC bus. This provides an overvoltage protection to approximately 3.1 pu DC bus voltage.

Table 3.2: Simulation Parameters of MOV IV Model for Aircraft System

Device	Littlefuse V242BB60 (MCOV: 3 kV [44])
Structural Capacitance	1000 pF
Leakage Resistance	1000 $M\Omega$
Upturn Resistance	1 Ω
Lead Inductance	0 H, negligible

Table 3.3: Simulation Parameters of SA IEEE Model for Shipboard System

Device	ABB Polim-H..ND (4.7 kV MCOV) [43]
L_0	42.0 nH
R_0	21.0 Ω
L_1	0.28 μH
R_1	13.65 Ω
C	476.19 pF

The simulation parameters for the MOV IV model used in the aircraft application and the SA IEEE Model in shipboard application are provided in Table 3.2 and Table 3.3, respectively.

3.4 Simulation Results

3.4.1 Simulation Circuit

The RCS-HDCB is to be installed near-to-source in an electrified transportation distribution system (e.g., aircraft and shipboard). The breaker protects the DC bus from any faults between the power electronic converters and the distribution loads. This environment is modeled in PLECS simulation software and its high-level circuit schematic is provided in Fig. 3.3.

The DC bus is modeled as an ideal voltage source with a line resistance and inductance. This represents the equivalent impedance of the distribution system. Since the parameters of the distribution systems are unknown, then the resistance

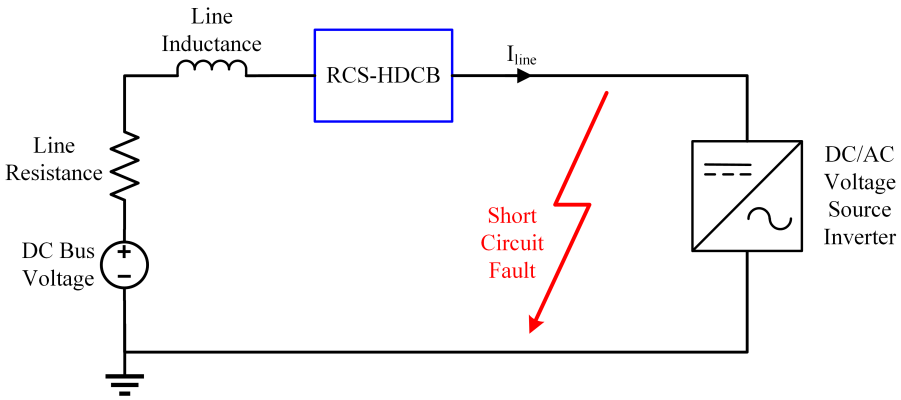


Figure 3.3: High-level simulation circuit topology of RCS-HDCB

is varied to control the fault current to a specific magnitude for simulation. The capacitance, in this case, is neglected since the main contributor to fault behavior is the resistance and inductance. When a fault occurs, the magnitude is limited by system resistance. The rise time and post-interruption transient overvoltage is limited by the inductance. The value of the line resistance is set such that it limits the magnitude of the fault to the desired level. Note that the magnitude could also be limited, within a certain time period, by using an appropriately sized current choke varying the system impedance. This approach could be favorable in a physical application since it would limit fault current magnitudes and rise time while limiting the increase in line resistance. It may also have a negative effect on the energy dissipation mode of the circuit breaker. The load of the system is modeled as a 3-phase voltage source inverter that pulls 675 A from the DC bus during normal conditions. Two RCS models are used in both the 2.4 kV aircraft and 20 kV shipboard applications, and one MOV is used for the aircraft MVDC system while 5 in-series surge arresters are used for shipboard MVDC system. The parameters set for the RCS modules in each application are provided in Table 3.4. GaN MOSFETs are used for the aircraft system while SiC MOSFETs are used in the shipboard applications to enable higher RCS source voltage and higher RCS current.

Table 3.4: RCS Module Simulation Parameters

Category	**2.4 kV Aircraft**	**20 kV Shipboard**
WBG Device	EPC2022 GaN MOSFET [24]	Cree CAS325M12HM2 SiC MOSFET Module [25]
Source Capacitance, C_s	6.00 mF	6.00 mF
C_s Initial Voltage	151 V	540 V
Equivalent Inductance	2.53 μH	2.53 μH
Equivalent Capacitance	1.00 μF	1.00 μF
Resonant Frequency	100 kHz	100 kHz
Reversals	27	15

The overall interruption speed of the breaker is limited by how quickly the contacts of the VI can open. This is because mechanical contacts gain greater ability to isolate by greater separation, and the ramping of the RCS is much faster than the opening speed of the mechanical switch. Utilizing an actuator with both Thomson coils and permanent magnets, the expected opening speed of the breaker is <500 μs. Therefore, the RCS in simulation coordinates its peak reversal with 500 μs after the VI starts to actuate. At this point, the dielectric recovery ability of the contacts is at its greatest. However, recent hardware experimentation in [45] shows promising results, albeit at lower power, that the RCS can be used to quench arcs before the VI is fully open. This would significantly improve the fault interruption speed of the breaker. The RCS is much faster than the opening speed of the VI, so it is free to utilize many reversals to interrupt fault current. This allows for lower source voltages and current differentials between reversals. At 100 kHz, the RCS can achieve 100 reversals before the VI fully opens. Realistically, this is further limited by the thermal behavior of the MOSFETs and the saturation rate of the RCS.

The key parameters of each model are listed in Table 3.5. The fault is set to initiate 10 ms after the simulation starts. Note that the simulated waveforms of the WBG switches are given referring to S1 or S2 in the first RCS module. This is done

Table 3.5: Circuit Parameters for RCS-HDCB Fault Interruption Simulation

Category	**2.4 kV Aircraft**	**20 kV Shipboard**
DC Bus Voltage	2.4 kV	20 kV
Line Inductance	3.33 μH	111 μH
VI Opening Time	500 μs	500 μs
Fault Initiation Time	10 ms	10 ms
Peak Fault Current	9.4 kA	19 kA

for brevity since all other switch waveforms are identical or inverted (e.g. voltage, current, junction temperature, etc).

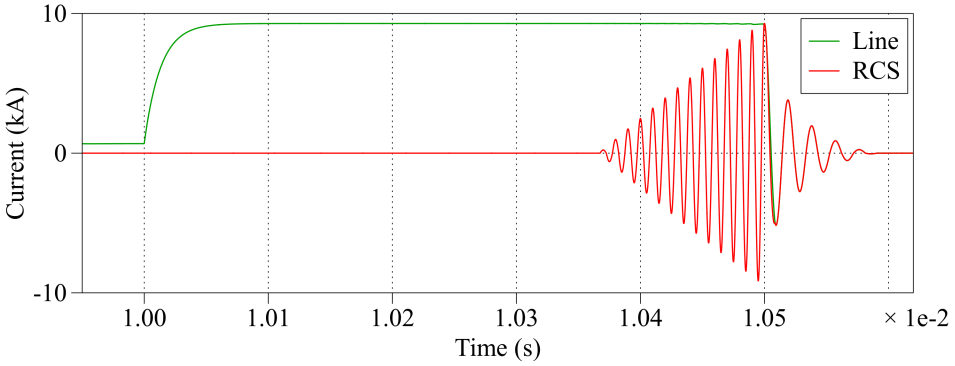
3.4.2 2.4 kV Electric Aircraft Application

The details of fault operation shown in Figs. 3.4 - 3.6 are explained as follows:

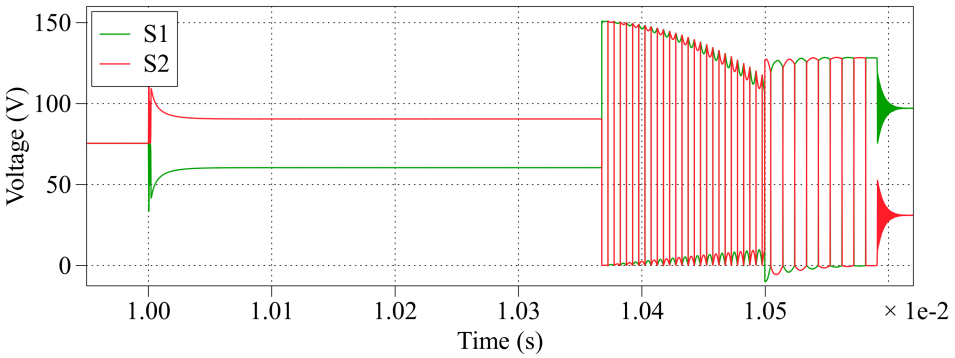
1. *Normal Operation Mode (<10ms):* Normal load current, 675 A, flows through the line and VI as shown in Fig. 3.4a and 3.5a. The ultra-low contact resistance (1 $\mu\Omega$) leads to negligible on-state losses and high efficiency (99.99%). The MOV is a high impedance and only conducts negligible leakage current, 16.7 nA. The RCS modules do not conduct and await the fault.

2. *Turn-off Commutation Mode (10-10.5 ms):* The DC bus is shorted, and a 9.3 kA fault current many magnitudes higher than the load flows through the line. The VI is commanded to open, and an arc is established across its contacts, as shown in Fig. 3.5. This arc appears as a low resistance and the fault continues to flow through it. The rise time of the fault is limited by the line inductance between the source and fault location, and the final magnitude is limited by the line and arc resistance. The arc introduces a low voltage across the breaker that can be observed in Fig. 3.5c. The voltage initially spikes, and then the arc stabilizes to a low voltage and low resistance (30.1 V, 3.24 $m\Omega$). This is analagous

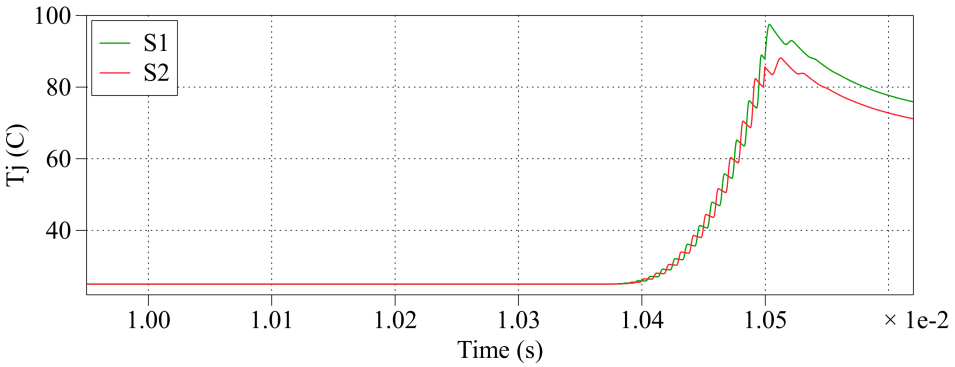
to the breaking of the VI molten bridge. After a time delay calculated from the desired reversals, the H-bridge oscillates its source voltage at the resonant frequency. This builds the current through the RCS, and it ramps from zero to the magnitude of the fault current starting at at 10.365 ms. The peak of



(a) Line and RCS current during fault

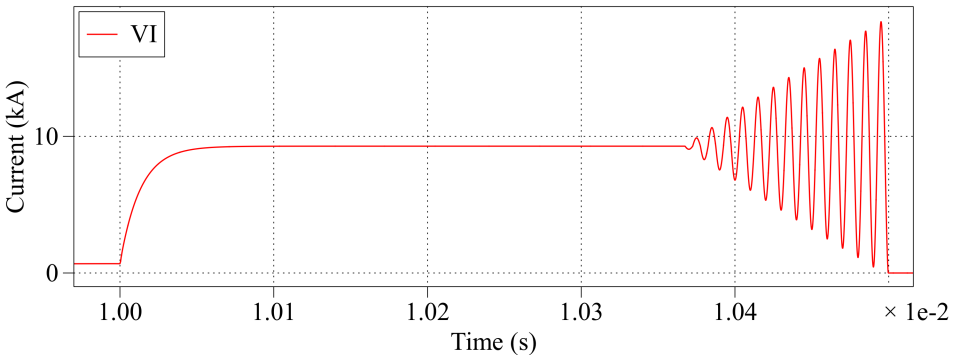


(b) GaN MOSFET voltage

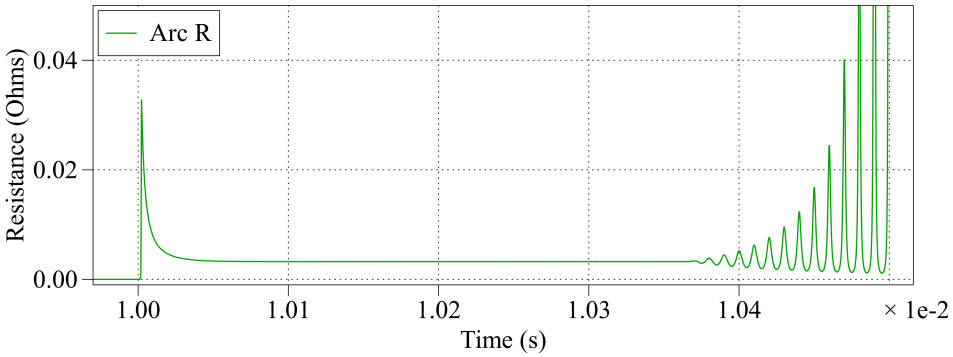


(c) GaN MOSFET junction temperature

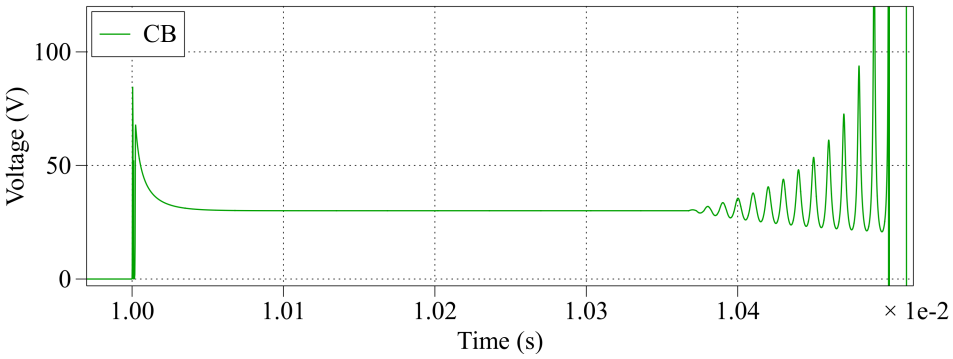
Figure 3.4: 2.4 kV RCS-HDCB fault interruption operation waveforms



(a) VI current



(b) Arc resistance



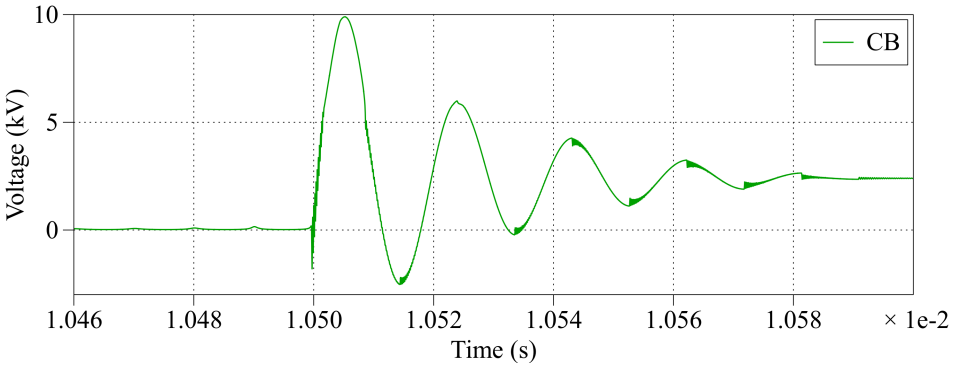
(c) CB voltage during arc

Figure 3.5: 2.4 kV RCS-HDCB arc waveforms during fault

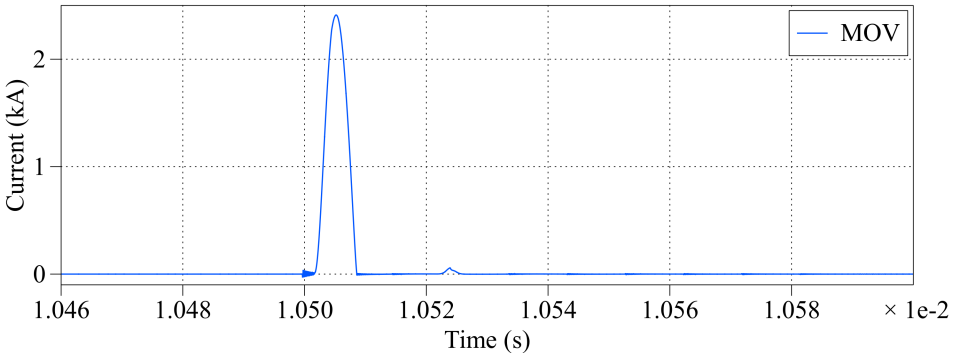
the 27th reversal occurs at the fully open point of the VI 500 μs after the fault initiates. During oscillation, the peak junction temperature of the GaN devices reaches 97.5 $°C$. This operational mode is concluded when the RCS current induces the zero current crossing and quenches the arc in the VI at 10.5 ms.

3. *Arc Extinguishment (10.5 ms):* The resistance of the arc, shown in Fig 3.5b, can be seen changing as the RCS injects current into the VI. As the RCS current increases, the current commutates away from the VI and into the commutation branch. This de-stabilizes the arc, and its resistance increases. As the RCS continues to ramp, the resistance of the arc peaks higher with lower VI current. At the peak reversal, the RCS resonant current fully opposes the fault current, and the current crosses zero inside the VI. This zero crossing gives the opportunity for the arc to quench. The resistance of the arc increases rapidly to an effective open circuit (160 $M\Omega$). The arc is considered quenched, the contacts of the VI are an open circuit, and the fault current transfers into the commutation branch.

4. *Energy Dissipation and Fault Isolation (>10.5 ms):* The fault flows briefly through the commutation branch through the GaN devices' antiparallel diodes. This is beneficial to recharge the source capacitor and regain some of the energy lost during current ramping. As this occurs, a voltage transient grows rapidly across the breaker as shown in Fig. 3.6a. Once the overvoltage passes the knee voltage of the MOV, it switches from a high to low resistance. The fault current then transfers into the energy dissipation branch and flows through the MOV, as shown in Fig. 3.6b. This clamps the overvoltage to 9.89 kV. It should be noted that the choice of upturn resistance controls the peak overvoltage during MOV conduction. If the resistance is decreased, then the clamped voltage decreases and becomes flatter. In other words, the clamping behavior becomes more ideal. The IV model of the MOV needs some upturn resistance to avoid erroneous oscillation. Once all residual energy in the line inductance and RCS is dissipated, the MOV stops conducting and resumes high impedance. The



(a) Circuit breaker voltage



(b) MOV discharge current

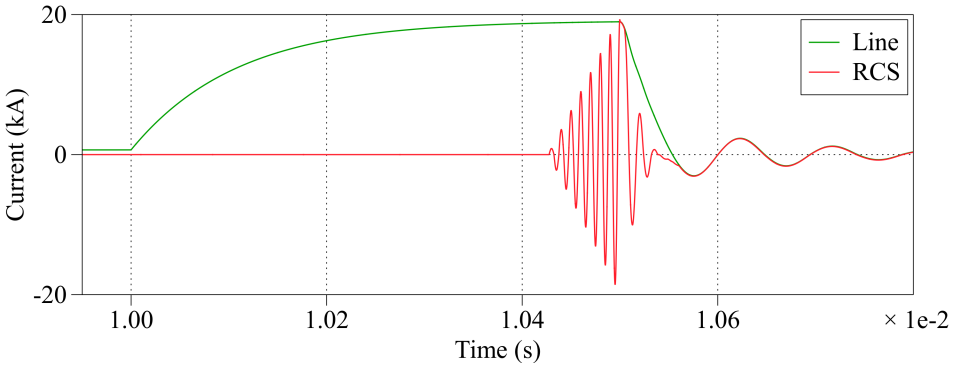
Figure 3.6: 2.4 kV RCS-HDCB post-interruption overvoltage waveforms

voltage undergoes a short transient and gradually relaxes to the nominal DC bus voltage. At this point the fault is fully isolated and all circuit breaker operation ceases.

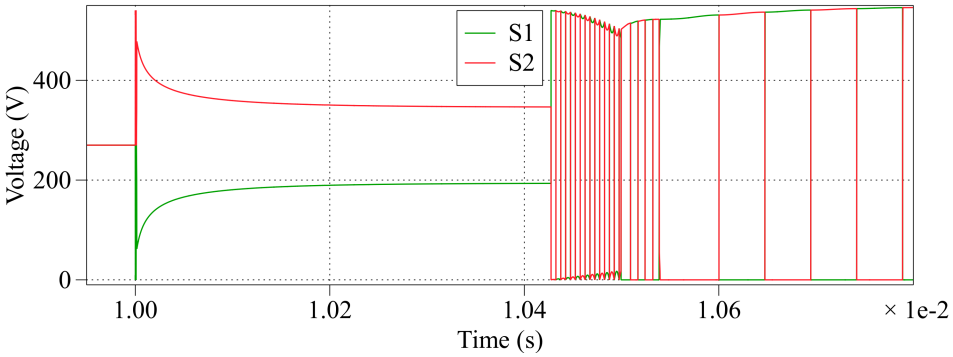
3.4.3 20 kV Electric Shipboard Application

The details of the fault operation simulation in Fig. 3.7 - 3.9 are described below.

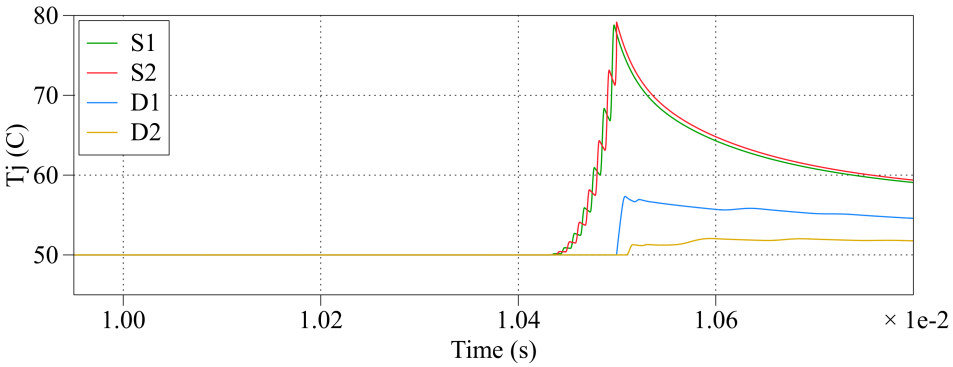
1. *Normal Operation Mode (<10ms):* The breaker is in steady state, and the load current from the line flows only through the VI in the conduction branch, as shown in Fig. 3.7a and 3.8a. The low losses are attributed to the low contact resistance, set to 1 $\mu\Omega$, of the VI. The losses can easily be neglected and the circuit breaker achieves high efficiency during normal operation of 99.99%. Neither the



(a) Line and RCS current during fault



(b) SiC MOSFET voltage

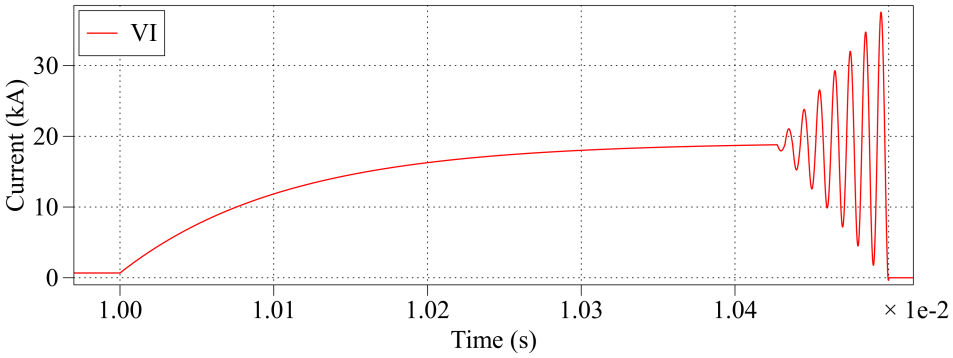


(c) SiC MOSFET junction temperature

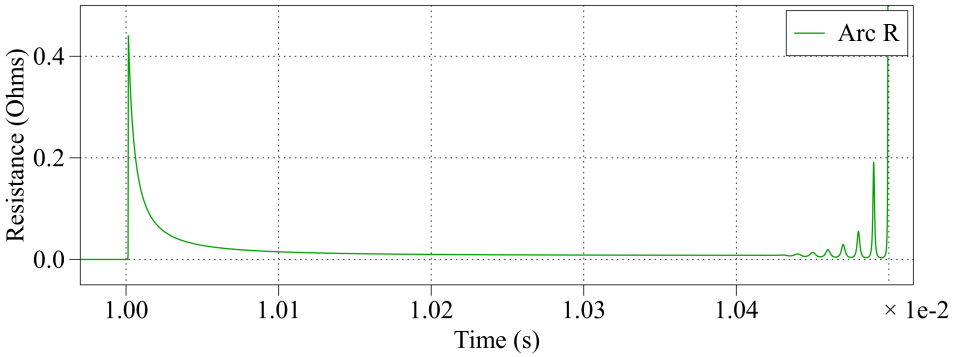
Figure 3.7: 20 kV RCS-HDCB fault interruption operation waveforms

commutation nor energy dissipation branch conducts significant current. The RCS lies dormant waiting for a fault, and the SA array appears as an effective open circuit. Only leakage current flows through the SA at such a low voltage.

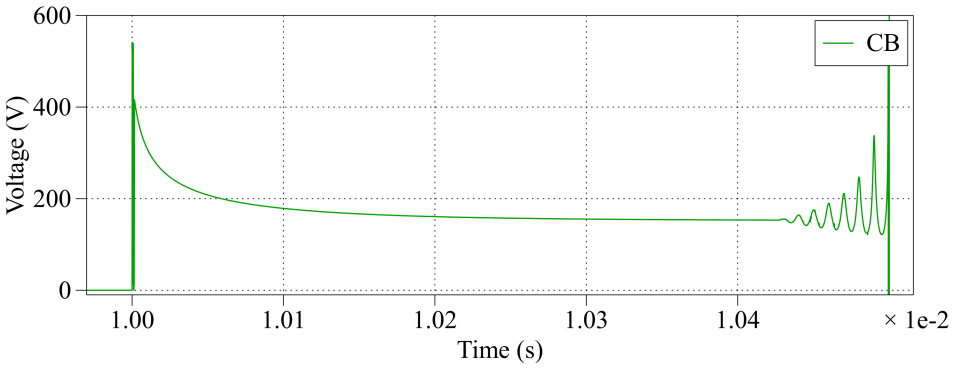
2. *Fault Operation/Commutation Mode (10-10.5 ms):* The fault occurs at 10 ms where the DC bus is shorted far from source, and the VI is commanded to start opening, which begins the fault operational mode. As the VI contacts separate, an arc is established with a small resistance and low voltage (0.08



(a) VI current



(b) Arc resistance

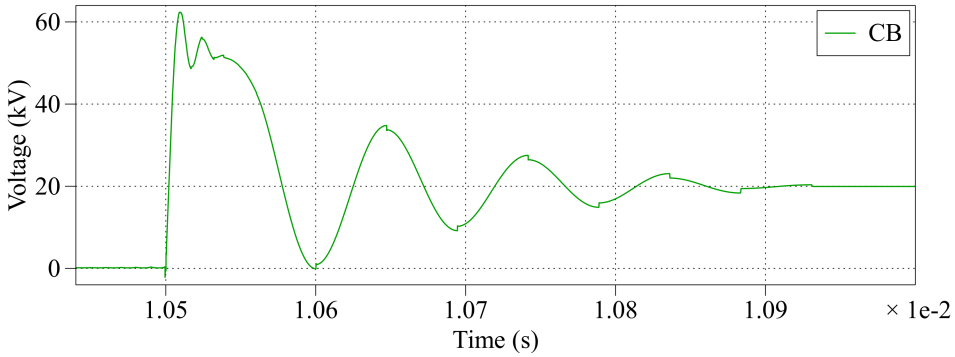


(c) CB voltage during arc

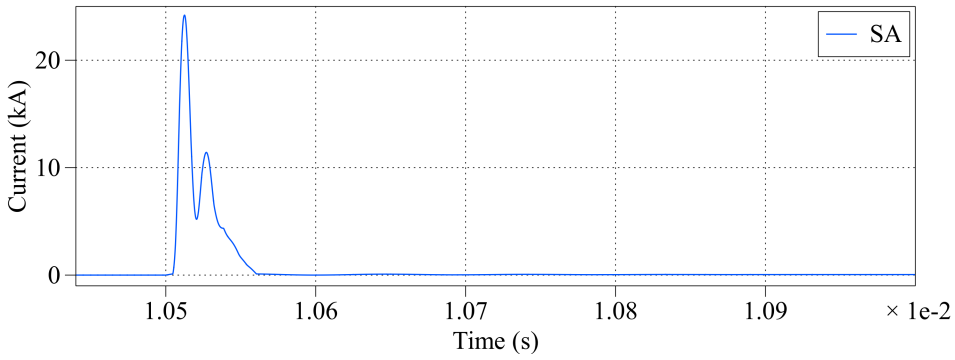
Figure 3.8: 20 kV RCS-HDCB arc waveforms during fault

Ω, 153 V), as shown in Fig 3.8b and 3.8c. The resistance of the arc peaks and then stabilizes, which is analogous to the breaking of the contacts' molten bridge. The fault current continues to conduct through this arc and reaches a peak magnitude of 18.98 kA, as shown in Fig. 3.8a. The RCS coordinates its peak reversal, set here to the 15th reversal, with the fully open time of the VI. The RCS commences oscillating at 10.428 ms. As the resonant current ramps continuously, the current can be observed commuting from the VI, and the arc resistance in turn increases as it destabilizes. As the RCS resonates, the SiC MOSFETs reach a peak junction temperature of approximately 80°C.

3. *Arc Extinguishment (10.5 ms):* At the final reversal, the current zero is achieved



(a) Circuit breaker voltage



(b) SA discharge current

Figure 3.9: 20 kV RCS-HDCB post-interruption overvoltage waveforms

in the VI, and the arc's resistance increases rapidly to an effective open circuit (250 $M\Omega$). The arc is quenched, and the current commutates away from the VI into the commutation branch. Fault interruption is therefore achieved in 500 μs. During this time, a transient overvoltage builds across the breaker due to the attempted interruption in line current, as shown in Fig. 3.9a. The fault current flows briefly through the antiparallel diodes of the RCS and recharges its voltage source.

4. *Energy Absorption and Fault Isolation (>10.5 ms):* Once the voltage surpasses the knee voltage of the SA array, it becomes resistively small. This transfers all fault current into the energy dissipation branch, and the residual energy left in the line and RCS modules discharge through it, as shown in Fig. 3.9b. This clamps the overvoltage across the breaker, as shown in Fig. 3.9a. The discharge current through the SA roughly resembles an 8/20 waveform with a superimposed ripple due to the RCS resonant component discharge. Since the IEEE model is used, the SA current lag behind the voltage is observable. The peak overvoltage is approximately the rated 8/20 waveform at 20 kA from the POLIM-H datasheet increased by a factor of 5 (i.e., the number of SA's used in series). Once the current is discharged through the absorption branch, the energy left in the system is dissipated and the voltage across the breaker relaxes to the nominal DC bus after a short transient. At this point, the fault is fully isolated and the breaker has completed all fault operational modes.

3.5 Conclusion

The conventional hybrid breaker combines a mechanical switch and semiconductor switches to compromise the benefits and drawbacks of mechanical and solid state breakers. While the efficiency is improved compared to the SSDCB, the losses are not negligible due to the semiconductive switches still present in the conduction path. The fault interruption speed is improved over the PRMDCB, but it is on the order of several ms and still too slow for adequate DC protection. Therefore, a fast-actuating VI and RCS can be utilized such that normal operation mode losses are negligible and the interruption speed is improved. Simulation results show that the proposed RCS-HDCB interrupted a DC bus fault within 500 μs in both the 2.4 kV aircraft and 20 kV shipboard MVDC systems. Also, the WBG semiconductor devices in the RCS modules did not exceed $100°C$ peak junction temperature. The benefits of this topology include fast interruption speed, high normal operation efficiency, ability to use relatively low voltage devices in the RCS modules, and modular and scalable circuit topology.

Chapter 4 HTS Fault Current Limiter Based Solid State DC Breaker

4.1 Circuit Description

Despite the stellar interruption speed, the main drawback for SSDCBs is the relatively low on-state efficiency during normal operation. This is due to the many solid state components needed to accommodate the DC bus voltage and the expected fault current magnitude. This drives the motivation of hybrid breakers to minimize or eliminate the number of solid state devices in the conduction path. In those cases, it is accomplished via mechanical switches or smart current commutation. However, the SSDCB itself can be enhanced without switching to hybrid topologies. The losses and number of devices needed can be improved in other ways by limiting the fault current and utilizing the emerging WBG switches.

The magnitude of the fault current can be controlled with a fault current limiter (FCL). It can be implemented simply by a sizeable inductance on the line (i.e., a current choke) or by a sophisticated solid state FCL. Using these, the peak magnitude of the fault current can be reduced. This benefits the solid state breaker since many less solid state switches are needed to account for the lowered fault current. This improves efficiency, power density, and losses. However, one of the main concerns of using these fault current limiters are their additional losses which affect the system efficiency. Likewise, solid state FCLs are active components so they need their own power and controls. This motivates the use of a highly efficient FCL with little to no controls.

One device that can be leveraged is the superconductive cable. When at normal

temperatures, superconductors are a significant resistance which can be used to constrain the fault current. At cryogenic temperatures (4.2 K for liquid Helium) the material presents zero resistance, which can be utilized for the normal conduction mode. High temperature superconductors (HTS) utilize the same concept, but are kept at "high" temperatures relative to others in cryogenics (77 K with liquid nitrogen). HTS cables are suited well for fault limiting applications since they exhibit zero resistance for load currents. Once a fault occurs, the current causes their junction temperature to quickly raise and exit the superconduction mode. This changes them from zero to significant resistance, which effectively inserts a large resistance that limits the magnitude of the fault. This is accomplished by the natural properties of HTS, so no controls are needed. Thus, the HTS cable can be used to make a highly efficient and passive FCL.

The HTS-FCL based solid state DC circuit breaker (HTS-FCL-SSDCB) leverages the naturally fault limiting capabilities of HTS cables. Its high level topology is provided in Fig. 4.1 [46]. The breaker can be broken into two sections: the FCL and the SSDCB. The FCL is made of an off-the-shelf HTS cable with liquid nitrogen cryogenic cooling. Like other breakers of its type, the SSDCB portion has a conduction and energy dissipation path. The main conduction path is an array of SiC MOSFET modules. This can be made to handle bidirectional currents if the MOSFETs were

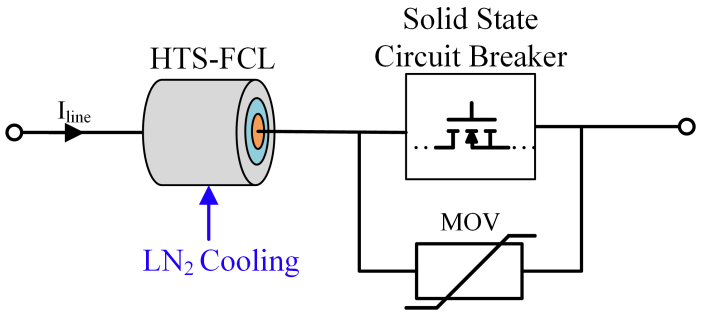


Figure 4.1: High-level topology of HTS-FCL-SSDCB

configured in anti-series connection to handle voltage and current in both directions. The energy dissipation branch is composed of a MOV device.

It should be mentioned that the quenching and recovery speed of HTS cables are not instantaneous. In fact, this is one of the main challenges when applying a HTS-FCL in MVDC systems [47]. The quenching speed is heavily dependent upon the thermal properties of the specific material and cable. For second generation HTS, the quenching speed is typically within 0.5-1 ms [48]. However, experimental results in [49] have shown promising quench speeds of 10 μs.

The HTS-FCL-SSDCB detailed and simulated in the following chapters is designed for 20 kV shipboard applications, and it shares the same system ratings as the previous RCS-HDCB shipboard application.

4.2 Topology

The detailed topology of the HTS-FCL-SSDCB is provided in Fig. 4.2. The breaker consists of two sections: the fault current limiting and the circuit breaking. In the current limiting section is a HTS cable used as a passive resistive FCL. The HTS cable needs a shunt resistance, R_{shunt}. The shunt is a necessity as it allows the HTS cable to evenly disperse its junction temperature across the cable. Without it, the HTS

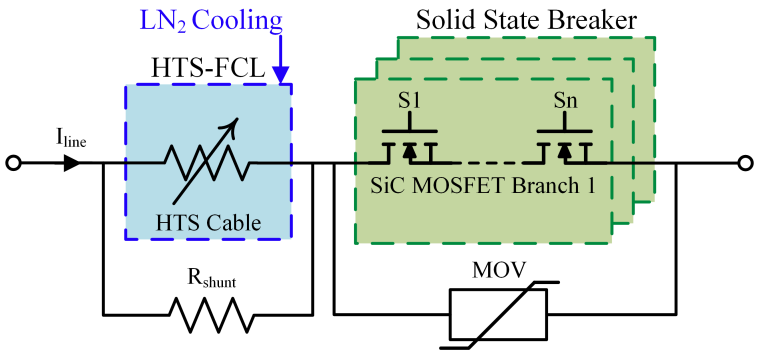


Figure 4.2: Detailed topology of HTS-FCL-SSDCB

cable would develop hot spots when exiting superconduction [50]. During normal operation, the shunt resistance is neglected since the superconductive resistance of the HTS is much less than the shunt. The circuit breaking section features an array of SiC MOSFETs that interrupt fault currents. In parallel is a MOV device to clamp inductive kicks and dissipate residual energy.

4.3 Operating Principle

The system can be represented by the equivalent circuit in Fig. 4.3. The circuit breaker is shown on the positive pole of the DC bus. Its equivalence is represented by a variable resistance for the HTS-FCL and a constant resistance for the SSDCB. The resistance of the HTS cable is controlled by its three operational regions: flux creep (superconductive), flux flow (transition), and normal (resistive). The resistance of each zone can vary due to changing junction temperature or current. For the purpose of describing the operating principle, it is convenient to think of it as a piecewise resistance as in Equation 4.1.

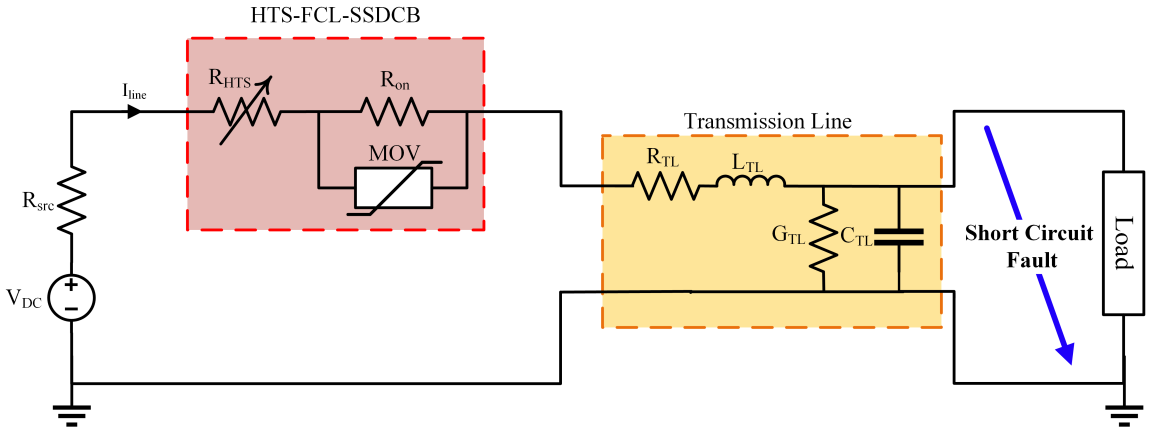


Figure 4.3: Equivalent circuit of system with HTS-FCL-SSDCB

$$R_{HTS} = \begin{cases} R_{sc} & \text{if } T_{HTS} < T_c,\ I_{HTS} < I_c \\ R_{tran} & \text{if } T_{HTS} < T_c,\ I_{HTS} \geq I_c \\ R_{shunt} & \text{if } T_{HTS} \geq T_c,\ I_{HTS} \geq I_c \end{cases} \tag{4.1}$$

where:

- T_{HTS}: HTS cable junction temperature (K)

- I_{HTS}: HTS-FCL cable current (A)

- T_c: critical temperature of HTS cable material (K)

- I_c: critical current of HTS cable (A)

- R_{sc}: flux creep/superconductive resistance (Ω)

- R_{tran}: flux flow/transition resitance (Ω)

- R_{shunt}: shunt resistance of HTS-FCL

During normal operation, the load current flows through the HTS cable and the SiC breaker. The magnitude of the load current can be written as Equation 4.2:

$$I_{line} = V_{DC} \left(R_{src} + R_{HTS} + R_{on} + R_{TL} + R_{Load} \right)^{-1} \tag{4.2}$$

where:

- I_{line}: line current (A)

- V_{DC}: DC bus voltage (V)

- R_{src}: source resistance (Ω)

- R_{HTS}: HTS-FCL variable resistance (Ω)

- R_{on}: on-state resistance of SiC MOSFET array (Ω)

- R_{TL}: transmission line resistance (Ω)

- R_{Load}: load resistance (Ω)

The load resistance is the most significant in the normal operational mode, so

it dictates load current magnitude. The HTS cable is superconductive, so R_{sc} is near zero. The relatively low load current ensures that the HTS cable's junction temperature stays below its critical temperature (e.g., 93 K for YBCO material) and at the temperature of the liquid nitrogen cooling at 77 K. The HTS-FCL allows for the minimization of SiC devices, so the SSDCB portion features less losses than a standalone SSDCB. The only significant losses of this breaker are due to the SiC MOSFETs conducting load current. Once a fault occurs, the load is shorted and replaced by a low resistance fault. The current flowing through the line increases rapidly by orders of magnitude. This causes the HTS cable to start increasing junction temperature. The cable will exit superconductive mode when both the junction temperature and current surpass the cable's critical temperature and critical current. As current increases, there is a short transition between superconductive and resistive modes. This occurs when critical current is exceeded but not critical temperature. This period is typically short, so it can sometimes be neglected. Once both critical parameters have been exceeded, the HTS cable exits superconduction and becomes a large resistance. Since the HTS cable's resistance is much larger than the shunt resistor's, the equivalent resistance is essentially R_{shunt}. This inserts a significant resistance into the system and attenuates the peak magnitude of the fault current. The fault, due to the resistive mode of the FCL, becomes more manageable and is orders of magnitude less than the unlimited fault current. This fault is inevitably less damaging to the system and easier to interrupt.

An example of typical fault waveforms is shown in Fig. 4.4. There are three faults shown on the figure: only SSDCB, FCL without SSDCB, and FCL with SSDCB. As seen, the fault with no current limitation is much larger than the other faults. Once the fault initiates, the FCL conducts the fault as normal until the critical

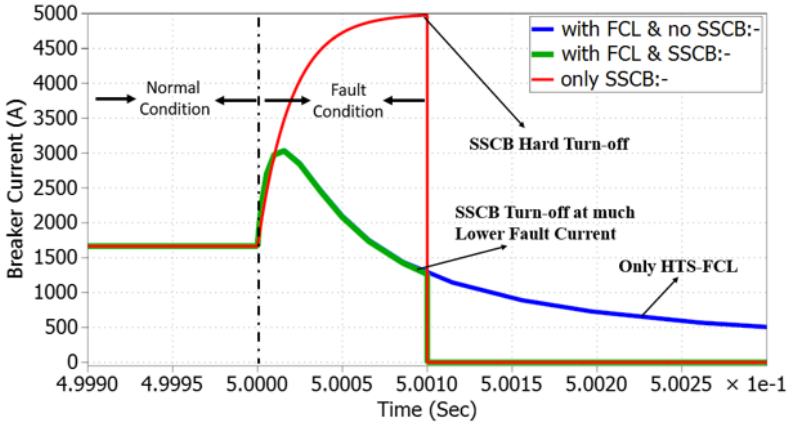


Figure 4.4: Typical line current during a fault with and without FCL and SSDCB

current and temperature of the HTS cable material is surpassed. After that, the cable exits superconduction and the fault is effectively attenuated without need for complex controls. Comparing the current at the time of interruption between the FCL+SSDCB and the only SSDCB the difference is 3.75 kA. Many more devices would need to be added in parallel to account for this increase in conduction and switching losses.

Once the fault has been attenuated, the SSDCB can safely interrupt the current. The gates of the MOSFET array are shut off simultaneously, and the fault is interrupted. The speed of interruption is comparable to that of the SSDCB. After the fault is interrupted, in the line's inductance current causes an inductive kick and a transient overvoltage builds across the SSDCB. After the knee point of the MOV device is surpassed, it changes from an near-open circuit to a very small resistance. This conducts the fault current, clamps the overvoltage across the breaker, and dissipates the residual energy left in the system.

After all energy is dissipated and the MOV returns to a high impedance, the fault is isolated. The HTS-FCL's junction temperature cools and relaxes back to the temperature of liquid nitrogen (77 K). In doing so, the FCL naturally becomes

superconductive again.

The benefits of this breaker include an improvement in SSDCB losses and efficiency, passive current limiting capabilities with no insertion loss, and fault interruption speeds comparable to conventional SSDCBs. This comes with drawbacks in the additional cryogenics and non-negligible solid state conduction losses that are normally associated with a SSDCB topology. Therefore, it is most realistic to implement this breaker in a system with an already existing cryostat.

4.4 Conclusion

Thanks to recent advances in power electronics, the SSDCB can be improved upon to provide high quality DC circuit protection. WBG devices can replace conventional Silicon transistors to significantly reduce switching and conduction losses. These losses, and the number of devices needed, can be further reduced by attenuating the magnitude of the fault. This is accomplished straightforwardly by utilizing a HTS-FCL. This FCL, contrary to conventional solid state FCLs, is passive with no need for control and has zero insertion losses in its superconductive state. This device enables the reduction in solid state devices in the SSDCB by limiting fault current to a manageable level. In doing so, the HTS-FCL-SSDCB has fault interruption speeds comparable to a conventional SSDCB while improving its efficiency.

Chapter 5 Modeling and Simulation of HTS Fault Current Limiter Based Solid State DC Breaker

5.1 SiC MOSFET Modeling

Like the case of the RCS-HDCB, the WBG MOSFETs must be modeled to analyze their junction temperature profile during operation and to ensure the reliability of the breaker concept. In doing so, we can be sure that their rated junction temperature is not exceeded during fault interruption. The expected fault current is the main design consideration since nominal load current is much less in magnitude and therefore less stressful. Again, like the RCS-HDCB, the main consideration in sizing the WBG devices is the current carrying capability. However, high voltage capabilities are desired as well, since the array of WBG switches needs to block full system voltage and transient overvoltage. SiC MOSFET modules are used for their high current and voltage capabilities. Using SiC MOSFETs has the added benefit of decreased on-state resistance, conduction/switching losses, and power density than conventional Silicon devices. Half-bridge modules are utilized such that the parasitic inductance among devices inside the array is minimized for a physical application.

The number of MOSFET modules needed to conduct the load and fault current can be estimated using the following equations, in which passive cooling is assumed. All parameters can be found directly from the manufacturer's datasheet of the devices. Equation 5.1 shows the calculation for the number of parallel devices needed to conduct the rated load current.

$$P_{load} = \frac{I_{load}\frac{1}{m}}{\sqrt{dT/(R_{ds,max}R_{ds,norm}R_{jc})}} \tag{5.1}$$

where:

- P_{load}: number of MOSFETs in parallel to conduct rated current

- I_{load}: rated current of system (A)

- m: load current safety margin (%)

- dT: allowable change in junction temperature ($^{\circ}C$)

- $R_{ds,max}$: rated maximum on-state resistance (Ω)

- $R_{ds,norm}$: normalization factor of $R_{ds,max}$ at steady state junction temperature

- R_{jc}: junction-to-case thermal resistance ($\frac{^{\circ}C}{W}$)

Then the number of MOSFETs needed to conduct the fault current can be estimated using Equation 5.2. Typically, this requires many more modules than the load current criteria, which makes Equation 5.1 insignificant in this scenario.

$$P_{fault} = \frac{I_{fault}\frac{1}{m}}{\sqrt{\left(T_{max} - (T_{amb} + dT)\right)/(R_{ds,max} * R_{ds,norm} * Z_{jc})}} \tag{5.2}$$

where:

- P_{fault}: number of MOSFETs needed in parallel for fault current conduction

- I_{fault}: prospective fault current limited by HTS-FCL (A)

- m: fault current safety margin (%)

- T_{max}: maximum rated or allowable junction temperature ($^{\circ}C$)

- T_{amb}: ambient temperature ($^{\circ}C$)

- $R_{ds,norm}$: normalization factor of $R_{ds,max}$ at T_{max}

- Z_{jc}: transient junction to case thermal impedance for time length of fault conduction ($\frac{^{\circ}C}{W}$)

Finally, the number of MOSFETs needed in series can be estimated in Equation 5.3. The total devices needed in the SSDCB portion of this breaker is the number in parallel multiplied by the number in series. The variable V_{max} should be appropriately set for either discrete MOSFETs or across modules.

$$S_{block} = \frac{V_{DC}}{mV_{max}} \tag{5.3}$$

where:

- S_{block}: number of series MOSFETs/modules for DC bus voltage
- V_{DC}: DC bus voltage (V)
- m: voltage safety margin (%)
- V_{max}: maximum rated drain-source voltage (V)

The theoretical equations provided tend to be an overestimation, so the amount of devices can be modified by evaluating the specific simulation or experimental results.

In the upcoming simulation, the Microsemi half-bridge module (Part Number: MSCSM120AM03CT6LIAG) is utilized [51]. The number of MOSFET modules needed in parallel is estimated to 5 modules with an 80% safety margin for 8 kA fault current. To account for the DC bus with a safety margin of 83.3%, only 10 modules are needed in series. However, this is not sufficient margin for the transient overvoltages that occur post-interruption. Thus, an extra 5 modules are added in series to make 15 in-series modules. This brings the maximum voltage blocking capabilities to 36 kV, or 1.8 pu DC bus. This results in many devices, 75 modules to be exact, and highlights the necessity of high performance switches. For SSDCB applications, the MOSFETs must have both high voltage and current capabilities such that the need for layering many devices is reduced. The use of WBG devices,

such as SiC, and the FCL assist in reducing the total number of solid state switches necessary.

5.2 High Temperature Superconductor Modeling

The HTS is a complex device due to the material properties and operating condition. For the purposes of circuit modeling, the HTS can be modeled as a current and temperature dependent resistance. Various different models can be used to accomplish this with varying degrees of complexity, computational burden, and approximation, which is elaborated as follows:

5.2.1 Resistance as a Function of Current

The first and most straightforward model of the HTS is a current dependent resistance. This neglects temperature dependency and only considers the current. This category can be further subdivided into different types of models such as current/voltage dependent resistance and a time dependent resistance. The latter is the most simplistic. The transition from superconductive to normal mode is a preprogrammed transition. The response is akin to the step response of a capacitor, and it can be modeled as such in Equation 5.4 [29]. The quenching speed is set via the time constant τ_c. The limitations of this model are readily apparent. It can only be accurate for the situation in which it was programmed, so despite the benefits of simplicity and computational burden, it lacks fidelity and dynamics.

$$R_{HTS} = R_{max}\left(1 - e^{-t/\tau_c}\right) \tag{5.4}$$

where:

R_{HTS}: transient resistance of HTS cable (Ω)

R_{max}: max resistance of transient (Ω)

τ_c: time constant (s)

The variable resistance is more preferred since its resistance can change with different circuit conditions. While not as high fidelity as other models, such as the power law, it has more fidelity and dynamic properties than the time transient model. In the upcoming fault interruption simulation, this model will be utilized for its benefits in ease of implementation, low computational burden, and relative fidelity. In practice, one of the downsides to using this model is the need for prudent initial condition setting. This is especially true for large simulations as erroneous initial conditions may be calculated or may not converge. This is not an issue so long as one knows the initial conditions of the simulation beforehand.

As detailed in [52], the resistance of the HTS can be modeled as dependent on current alone. The resistance curve for the current dependent resistance model is provided in Fig. 5.1. The IV curve is nonlinear and represents the superconduction for

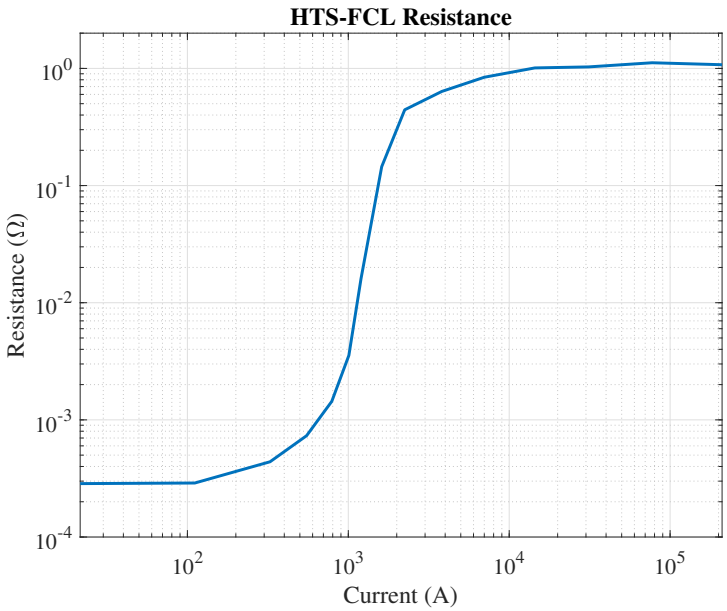


Figure 5.1: Resistance curve of the variable resistance HTS-FCL model

low currents, transition, and normal resistive mode for high currents. The nonlinear curve can be normalized by its critical current, then scaled to account for any application to model a generic HTS cable. The resistive mode's resistance approaches the shunt's resistance. Three modules are used in series in the upcoming fault simulation for a maximum fault operation resistance of 3.35 Ω.

5.2.2 Power Law Model

This next model is commonly used in literature especially when the parameters of the HTS cable are already known [53–55]. Power law models are common to use for nonlinear devices, such as MOVs or the Schwarz arc model. Applying this type of model can accurately replicate the behavior of the HTS cable in many conditions.

The block diagram of the model schematic is represented in Fig. 5.2. The equations used in this model are found in Equations 5.5-5.7 [55]. Despite the added complexity, this model has relatively low computational burden while retaining high fidelity. For example, the lag in superconductive quenching from the initiation of a fault to the time at which critical temperature is surpassed can be observed. Likewise, the exponent, n, can be changed to model the nonlinearity at each operational

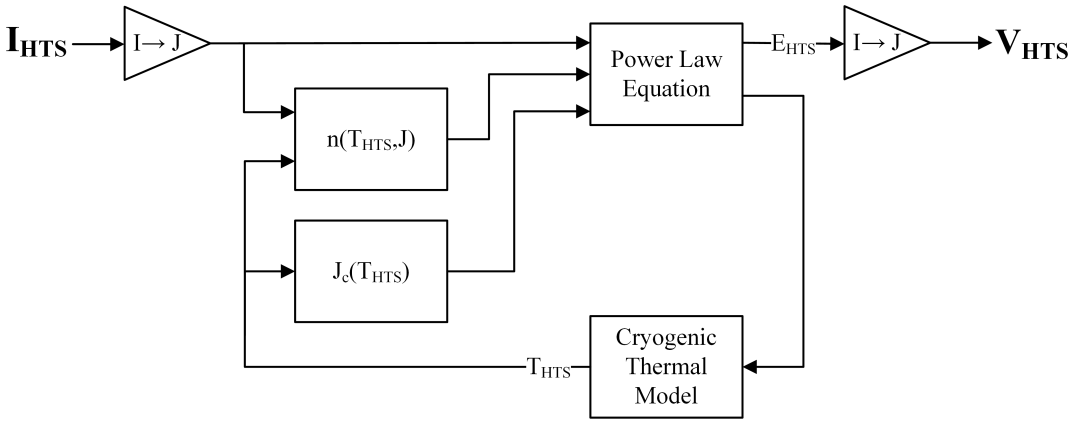


Figure 5.2: Block diagram of a power law model for HTS cables

mode. Note that the model itself uses the current density and electric field of the HTS cable, but the voltage and current can be easily calculated knowing the physical dimensions of the HTS tape in the cable. The model must also be interfaced with a suitable thermal model to calculate the junction temperature.

$$E_{HTS} = E_c \left(\frac{J}{J_c\left(T_{HTS}\right)} \right)^{n(T_{HTS},J)} \tag{5.5}$$

$$J_c\left(T_{HTS}\right) = J_c \left(\frac{T_c - T_{HTS}}{T_c - 77} \right) \tag{5.6}$$

$$n\left(T_{HTS}, J\right) = \begin{cases} n_1 & \text{if } T_{HTS} < T_c,\ J_{HTS} < J_c \\ n_2 & \text{if } T_{HTS} < T_c,\ J_{HTS} \geq J_c \\ n_3 & \text{if } T_{HTS} \geq T_c,\ J_{HTS} \geq J_c \end{cases} \tag{5.7}$$

where:

- E_{HTS}: HTS cable electric field($\frac{V}{m}$)

- E_c: critical electric field= $1\frac{\mu V}{cm}$

- J: HTS cable current density ($\frac{A}{m^2}$)

- $n\left(T_{HTS}, J\right)$: temperature dependent degree of nonlinearity

- $J_c\left(T_{HTS}\right)$: temperature dependent critical current density of HTS cable ($\frac{A}{m^2}$)

- n_1: flux creep (superconductive) exponent (typically a few tens)

- n_2: flux flow (transition) exponent (typically $n_2 \approx 4$)

- n_3: normal (resistive) exponent (n_3=1)

Sweeps of this model are included in a separate section of the simulation results to showcase the added fidelity that this model can provide. Using this model, varying temperature and current can represent all three operational modes of the HTS cable. For the simulation results, the AMSC Amperium Stainless Steel Wire Type 8612

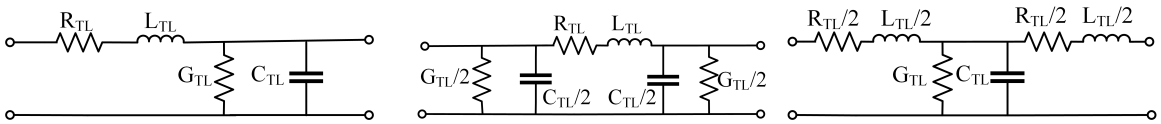
Table 5.1: HTS-FCL Power Law Model Parameters

Critical Current	500 A
Critical Temperature	92 K
Temperature of LN_2	77 K
Cross-sectional Area	$3.99\times10^{-6}\ m^2$
Length	1.0 m
n_1	25
n_2	4.0
n_3	1.0

cable [56] is modeled for its high fault current limiting capabilities. All parameters needed for this model can be found in the datasheet with the exception of the thermal modeling. The parameters are provided in Table 5.1.

5.3 Transmission Line Lumped Parameter Model

When lines are electrically short (i.e., line length≪wavelength), they can be modeled using a lumped parameter model [57]. At DC excitation, the wavelength is very long, so a lumped parameter model can be used to better approximate the impedance of the distribution line from source to load. Since the line is electrically small, the distribution line can be represented by one distinct lumped parameter model. Common model configurations for transmission lines are provided in Fig. 5.3. Any of the models are acceptable for transmission lines, but different configurations offer benefits at higher frequencies and different loads. The backward-Γ is used in the upcoming simulations to facilitate simulation convergence. Since the capacitance of the line is



(a) Backward-Γ model (b) Pi model (c) T model

Figure 5.3: Lumped parameter models of transmission lines in base units

placed at the end for this model, the load-side fault must have a small resistance.

To approximate the impedance of the distribution line, parallel separated 1 AWG copper wire is used as a reference. The line length is set to 30.5 meters (i.e., 33.3 yards) with 1 meter separation. The separation of the wires is much greater than the radii of the wire cross-section. Equations 5.8-5.10 are used to derive the parameters of the lumped parameter model.

$$r_{TL} = \left(\sigma \pi r_w^2\right)^{-1} \tag{5.8}$$

$$c_{TL} = \frac{\pi \epsilon_0}{\ln\left(s/r_w\right)} \tag{5.9}$$

$$l_{TL} = \frac{\mu_0}{\pi} \ln\left(s/r_w\right) \tag{5.10}$$

where:

- r_{TL}: per unit length (pul) resistance (Ω/m)
- σ: material conductivity (S/m)
- r_w: wire cross-sectional radius (m)
- c_{TL}: pul capacitance (F/m)
- ϵ_0: permittivity of free space (F/m)
- s: wire-to-wire separation (m)
- l_{TL}: pul inductance (H/m)
- μ_0: permeability of free space (H/m)

The key parameters for the transmission line model are provided in Table 5.2

Table 5.2: Transmission Line Simulation Model Parameters

r_{TL}	0.41 $^{m\Omega}/_{m}$
l_{TL}	2.24 $^{\mu H}/_{m}$
g_{TL}	5.00 $^{\mu S}/_{m}$
c_{TL}	4.96 $^{pF}/_{m}$
s	1.00 m
Line Length	30.5 m

5.4 Simulation Results

The simulation circuit schematic is provided in Fig. 5.4. The simulation parameters of the circuit are provided in Table 5.3. The breaker is installed on the positive pole of the DC bus and consists of three in-series HTS-FCL modules, an array of SiC MOSFETs for the SSDCB, and a MOV for overvoltage protection. Overvoltage protection is especially important for SSDCBs since it clamps high voltages at current interruption, and therefore minimizes excessive switching losses. In the simulation, the MOV is modeled using a linear varistor from MATLAB's Simscape library with

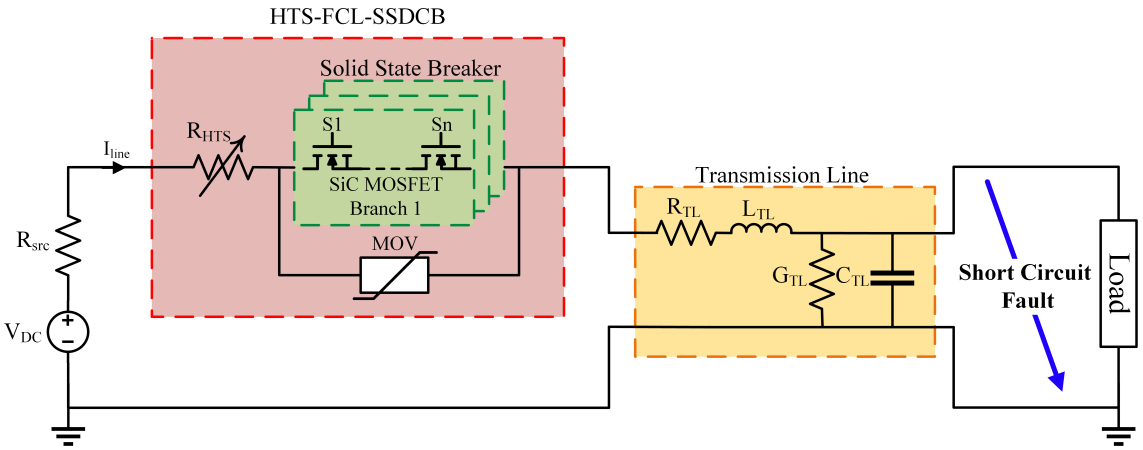


Figure 5.4: Circuit schematic of HTS-FCL-SSDCB system for fault interruption

Table 5.3: HTS-FCL-SSDCB Fault Interruption Circuit Parameters

Source Voltage, V_{dc}	20 kV
Source Resistance, R_{src}	1.00 $m\Omega$
Load	1 kA, 20 MW
Fault Initiation	0.20 s

a knee voltage set to 24.0 kV and an upturn resistance of 1 Ω. The DC bus voltage is modeled as an ideal voltage source with a series resistance. The circuit breaker is installed next to source and far from load. In between the breaker and load is a long parallel wire distribution line. The load is a simple resistive load that draws approximately 1 kA (20 MW) from the DC bus. A very small resistance fault is initiated at the terminals of the load that shorts the DC bus. This causes the line current to increase drastically and initiates the fault interruption process.

In this case, the simulated fault happens at the terminals of the load. This includes the source and line impedance at the onset of the fault. However, the worst case scenario is if the DC bus was shorted at the terminals of the breaker itself. The impedance present in the circuit would depend on where the breaker is installed. For instance, if a fault occurred at the terminals of the breaker in Fig. 5.4, then it would be limited by the equivalent series resistance of the DC bus capacitor bank until the HTS-FCL transitions into the normal resistive mode. In other words, the HTS-FCL would still have fault current limiting capabilities even in the worst case scenario. This specific scenario is not simulated in the upcoming section, and the fault occurs far-from-source.

5.4.1 Fault Interruption Simulation Results

The fault interruption waveform figures are separated to showcase the entire interruption operation, see Fig. 5.5; and the zoomed in transient overvoltage, see Fig. 5.6. The fault operation is summarized as follows:

1. *Normal Operation Mode (<200 ms):* The system is in steady state, and the nominal load current (≈1 kA, 20 MW) flows through the superconductive HTS-FCL and the SSDCB. Both elements of the breaker feature low or negligible

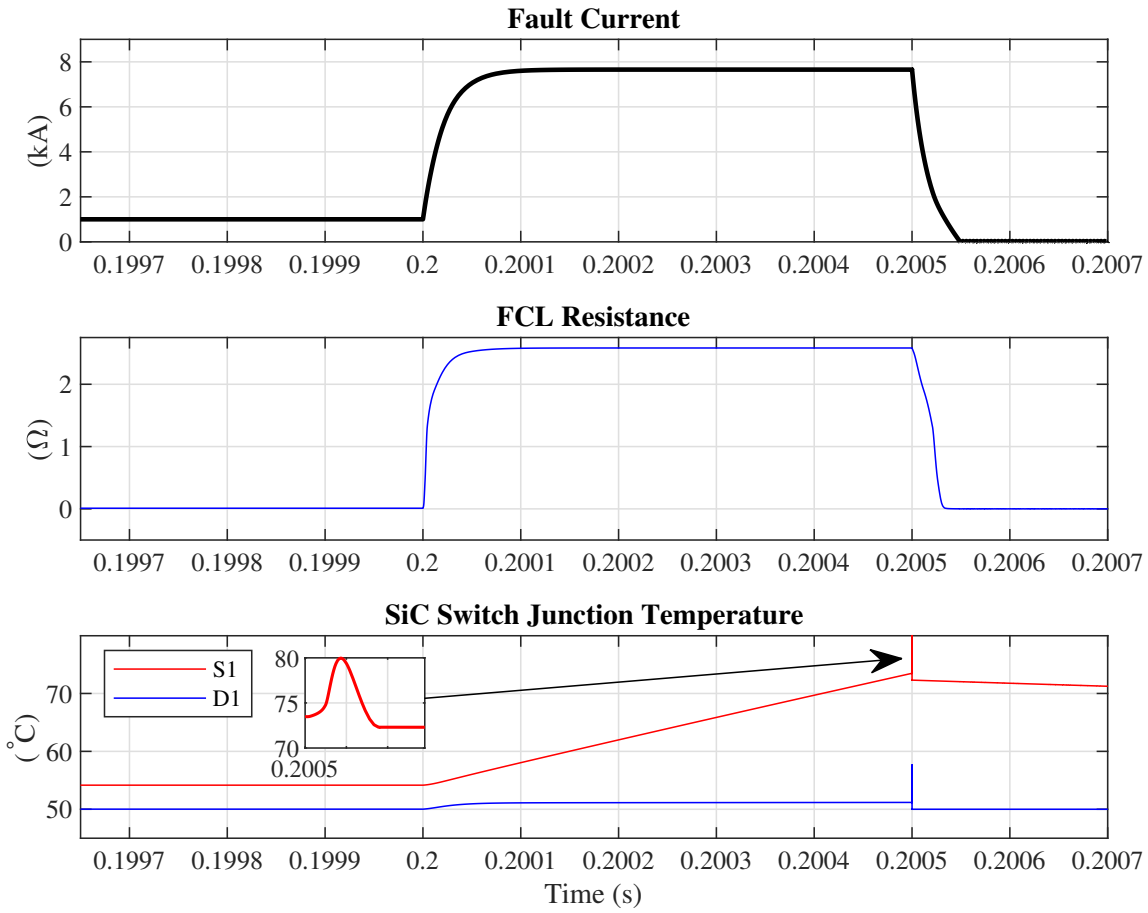


Figure 5.5: Fault interruption waveforms of HTS-FCL-SSDCB from top to bottom: fault current, FCL resistance, and SiC MOSFET junction temperature

resistance, and high efficiency is achieved of 99.92%. This efficiency includes only the in-circuit resistive losses and does not account for any overhead losses such as cryogenic cooling. In a physical application, such losses would lower the efficiency. The MOV is a high impedance at this time since the voltage drop across the SSDCB is low, so it is considered an open circuit. The temperature deviation of the SiC switches inside the SSDCB is $4.2°C$ above the ambient temperature of $50°C$. This is far below the maximum allowable junction temperature of $175°C$.

2. *Fault Conduction (200-200.5 ms):* The fault is initiated in which the DC bus is

short circuited at the terminals of the load. The line current increases rapidly to many times the nominal load current, as shown in Fig. 5.5. For a short time, the fault current increases at such a rate as it would without the presence of the HTS-FCL. The growth is limited in speed by the line inductance and equivalent system resistance. The fault continues until the current surpasses the critical current of the HTS cable. This causes the HTS-cable to leave superconduction mode and enter the normal resistive mode. It then naturally responds to the rising current by increasing its resistance significantly. In Fig. 5.5, the resistance of the FCL follows the increase in line current before saturating to a peak of 2.58 Ω. This effectively inserts its shunt resistance into the line impedance, which limits the severity of the fault to 7.7 kA.

3. *Fault Interruption (200.5 ms):* The SSDCB interrupts the fault, and the gate signal to shut off is applied to all SiC MOSFETs in the array. The devices' junction temperature jumps from $73.5°C$ to its maximum of $80.0°C$ due to the switching losses associated with the interruption. If no overvoltage protection was used, this switching loss would be exacerbated due to the excessive overvoltage.

4. *Energy Dissipation and Fault Isolation (>200.5 ms):* The interruption in the system inductance current causes an overvoltage to rapidly build across the SSDCB portion of the breaker. The energy dissipation portion of the waveform can be seen in Fig. 5.6. The SSDCB endures this voltage until the knee voltage of the MOV is surpassed. At that point, they switch from an open circuit to a low resistance. This causes the fault current to commutate through the MOV. This clamps the overvoltage to a peak of 31.6 kV and dissipates the residual

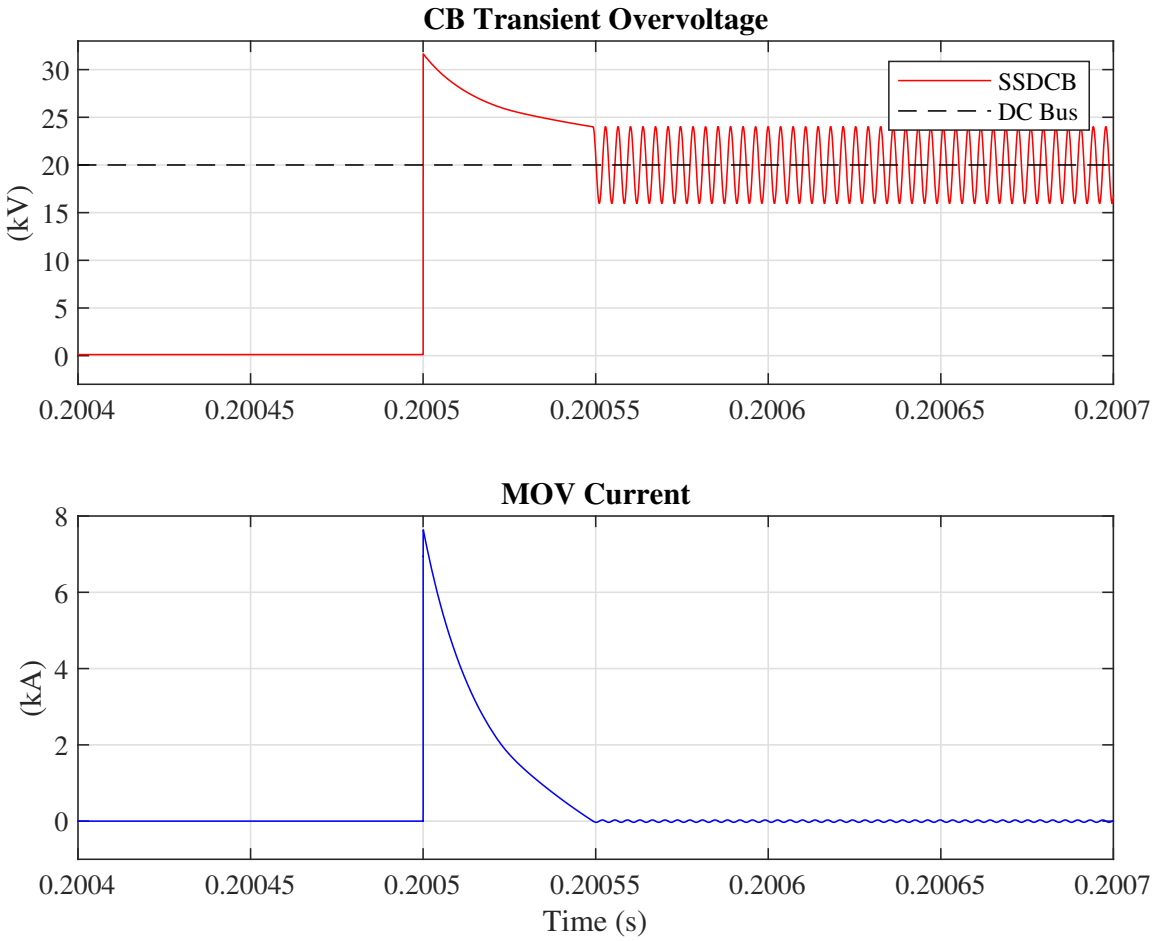
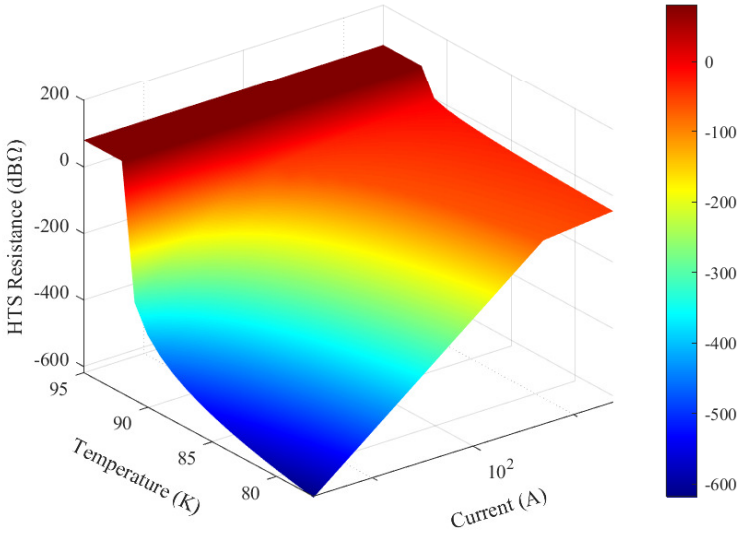


Figure 5.6: Overvoltage waveforms post-interruption of HTS-FCL-SSDCB from top to bottom: CB post-interruption voltage and MOV discharge current

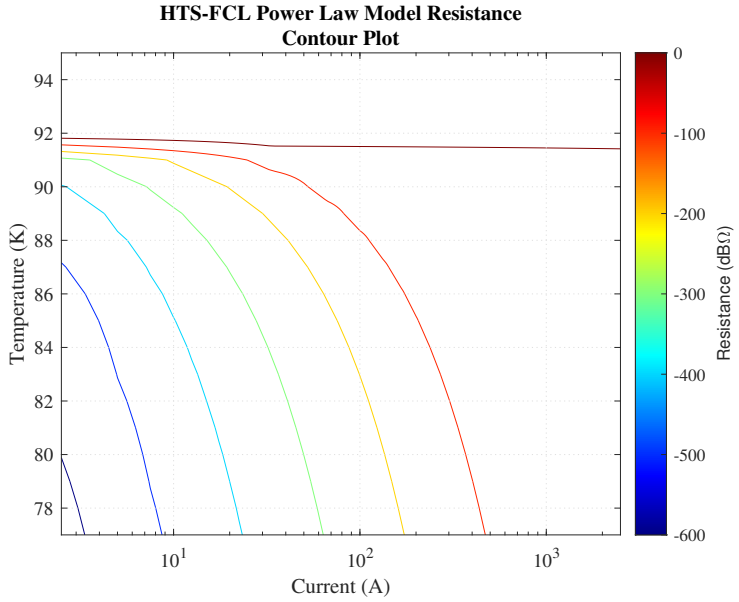
energy still left in the line impedance. Once the energy dissipates, the MOV resumes high impedance operation and the CB voltage relaxes to the DC bus nominal voltage after ringing.

5.4.2 HTS Cable Power Law Model Sweep

The power law is a powerful way to model nonlinear devices. In this section, the usefulness of the power law model is explored for the use of the HTS-FCL. The parameters of the simulated model are provided in the datasheet of the AMSC Type 8612 cable [56].



(a) 3D resistance plot versus temperature and current



(b) contour plot of resistance

Figure 5.7: HTS-FCL power law model resistance sweep

The inputs of current and temperature are swept and shown in Fig. 5.7. The contour plot is provided for clarity around the transitions. For low temperatures and low currents, the resistance is extremely low (i.e., 4.77e-63 Ω). This value is so small that it can most certainly be neglected and considered zero resistance. The model

is superconductive, highly nonlinear, and in the flux creep region of operation. In normal load conditions, the HTS cable should operate within this region.

If the temperature is held low and the current continues to increase, the model also increases its resistance. After the critical current is surpassed, the model transitions to its flux flow state. The resistance here is much less nonlinear than in flux creep, so the resistance appears as saturated. The temperature dependency of the critical current can also be observed. The edge of the fall off between flux flow and flux creep shifts into lower currents as the junction temperature increases. As the temperature approaches the critical temperature, the critical current becomes very small and the model transitions quickly. Above the critical temperature, the model saturates to a large constant resistance. The model is no longer nonlinear and enters the normal resistive operation. Note that this models the resistance of the FCL itself, so the shunt resistance is not represented here.

One design parameter for the HTS-FCL is the length of cable used. The effects of varying the length can be observed in Fig. 5.8. Here, the current and length is varied while the temperature of the cable is held constant. Resistance at superconducting temperature, just below critical temperature and just above is shown. Like in Fig. 5.7, the resistance increases with the temperature and the nonlinearity decreases. It is easy to see the relationship between length and resistance by looking at the edge of each temperature's trace at low current. For low temperatures, the resistance versus length increases and follows an exponential function. This eventually saturates for large lengths. For high temperatures above the critical temperature, the length of the superconductor does not affect the resistance of the model as significantly. There is a very slight positive linear relationship, but the effects are negligible at this temperature. Therefore, the length of the superconductor has a positive relationship

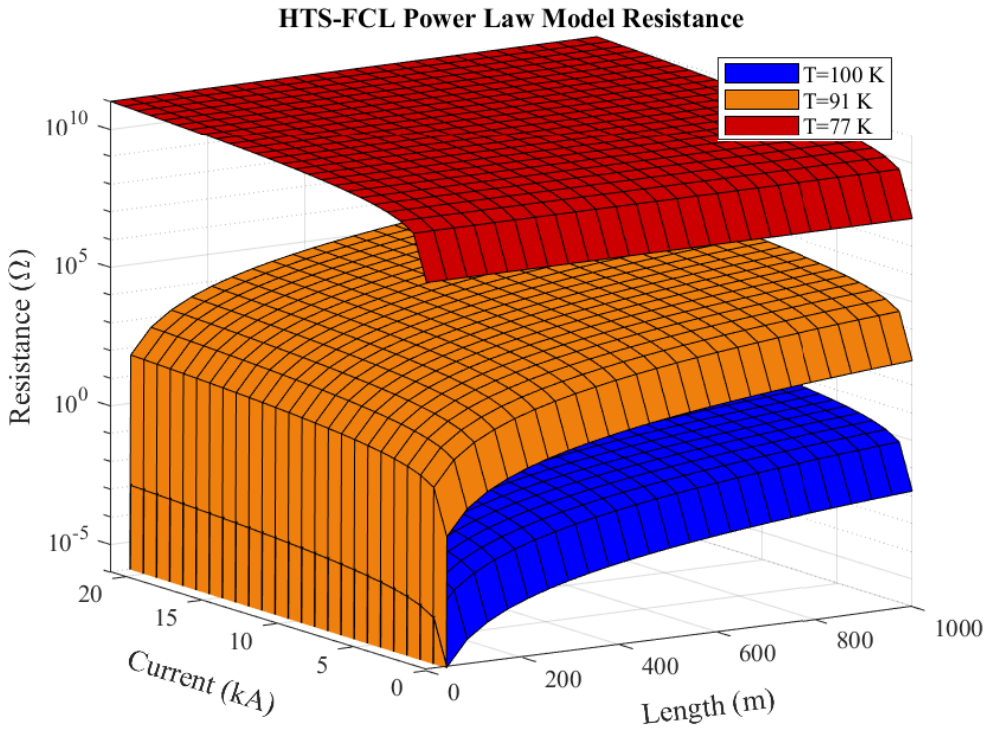


Figure 5.8: Resistance of HTS power law model versus length and current

with resistance below the critical temperature, but is not a concern in temperatures above critical.

5.5 Conclusion

The main drawback with conventional SSDCBs is the significant losses during load current conduction. This can be improved by utilizing WBG devices which exhibit lower on-state resistance than conventional Si counterparts. Likewise, the number of devices required to achieve safe fault interruption can be minimized by decreasing the magnitude of the prospective fault. This is accomplished by utilizing a superconductive FCL that is based upon the natural current limiting properties of HTS cables. At normal load currents, the HTS-FCL is superconductive and there is insignificant losses due to its ultra-low resistance. Compared to Si transistor based SSDCBs, the

load current flows through the SiC MOSFET based SSDCB with decreased losses. The number of devices are decreased as well. During a fault, the current increases rapidly to a large magnitude, which is limited by the impedance of the system. The large current causes the HTS-FCL to exit superconduction which effectively inserts a significant resistance into the line impedance. This attenuates the magnitude of the fault to a value that is much less than without the FCL. Such a short-circuit fault can be interrupted by a reduced number of devices in the SSDCB. The lesser magnitude of the fault current is safer for the system itself as well. Using this topology, the HTS-FCL-SSDCB has the same benefits of the conventional SSDCB while improving its drawbacks. The normal load current losses are minimized while the fault interruption speed remains quick and comparable to the conventional SSDCB.

The HTS-FCL-SSDCB was simulated in a 20 kV shipboard MVDC distribution system. The triggered fault was attenuated to 7.7 kA. This was interrupted by using the SiC SSDCB of which reached a peak junction temperature of $80.0°C$. The peak overvoltage was 31.6 kV, which is below the absolute maximum voltage of the SiC array of 36 kV. The simulated interruption speed was 500 μs; however, this may be further limited by the quenching speed of the HTS-FCL in practical implementation.

The power law based model of the HTS cable is also explored to showcase its ability to recreate the three modes of operation: flux creep, flux flow, and normal resistive. The model's temperature and current variability is shown along with the effects of varying superconductor length. For future simulations involving the HTS-FCL, it is recommended to opt for the power law model for increased dynamics and fidelity. However, one of the main drawbacks of the power law model compared to the current dependent resistance model is the increased number of parameters needed.

Chapter 6 Conclusion and Future Work

6.1 Conclusion

There are many benefits to the increased electrification of our modes of transport. The greenhouse gas emissions of these aircraft and ships can be reduced or entirely eliminated. This has ramifications in air quality, acoustic noise level, and an enhancement in the system performance. MVDC distribution enables these benefits by providing a reduced weight, increased efficiency, and reliable electric distribution network. For this system to be feasible, high performance DC circuit protection is a necessity.

Circuit breakers in MVDC systems need fast interruption speed, high efficiency, high power density, high reliability, and cost-effectiveness. The theoretical research performed in this thesis explores the two promising conceptual breakers that can provide such fault protection for MVDC systems. The RCS-HDCB and HTS-FCL-SSDCB have high efficiency and ultra fast interruption speeds with the capability of high power density, in addition to the lower implementation cost due to the much lower number of semiconductor switches required. A summary of the performance of these two breaker concepts based on our studies can be found in Table 6.1. Both breakers were modeled and simulated in a MVDC distribution system of 2.4 kV aircraft or 20 kV shipboard systems. Each breaker has the ability of fast fault interruption and high efficiency. Because of the fast switching capabilities of SiC MOSFETs in the conduction path, it is possible that the interruption speed of the HTS-FCL-SSDCB can be further improved upon; however, this may ultimately be limited by

Table 6.1: Summary of Simulation Results for RCS-HDCB and HTS-FCL-SSDCB MVDC Circuit Breaker Concepts

Category	**2.4 kV Aircraft RCS-HDCB**	**20 kV Shipboard RCS-HDCB**	**20 kV Shipboard HTS-FCL-SSDCB**
Interruption Speed	500 μs	500 μs	500 μs (determined by HTS material)
Efficiency	99.99%	99.99%	99.92%
WBG Device Load Junction Temperature	ambient(dormant)	ambient(dormant)	4.2°C above ambient
WBG Device Peak Junction Temperature	97.5 °C	80 °C	80.0°C

the quenching speed of the HTS-FCL. During fault current interruption, the peak junction temperature of all devices did not exceed 100 °C. They also exhibited high efficiency of above 99% during normal operation.

6.1.1 Resonant Current Source Hybrid DC Breaker

The motivation of the RCS-HDCB is to improve upon the existing conventional HDCB. The goal of this concept is to incorporate a fast-actuating VI with a solid state RCS to have high efficiency, high power density, scalability through modularity, and ultra-fast interruption. Since the RCS uses a decoupled low voltage source, the WBG devices in the H-bridge of the RCS are decoupled from the voltage of the DC bus in a fault. This enables the use of low voltage rated devices and decreases the cost of each RCS module. The main consideration for the WBG devices is the ability to conduct high pulse currents. Likewise, the voltage isolation of the WBG switches results in the breaker being less sensitive to overvoltages. A modular approach is used such that many RCS modules can be stacked for different application ratings. The control of the RCS is relatively simple compared to other solid state inverters, and it

is naturally zero-current switching. This means that the junction temperature of the switches is mainly a result of conduction losses. By using WBG MOSFETs, the RCS can increase power density, decrease losses, and enable high frequencies of resonant current. This facilitates the fast interruption of faults. Finally, the interruption speed is largely limited by the opening speed of the VI, so a fast-actuator is utilized to open within 500 μs.

The RCS-HDCB concept was simulated in a 2.4 kV electric aircraft system and 20 kV shipboard distribution system. Thermal modeling was used for the WBG switches to monitor their junction temperatures during interruption. An IV model represented the MOV, and the IEEE model was used for the SA. The breaker was placed on the positive pole of the DC bus and successfully interrupted a 9.3 kA fault for the aircraft, and a 19 kA fault for the shipboard system. BBAM was used to model the behavior of the arc inside the VI and its effects on interruption. The RCS commutated fault current and induced a current zero to quench the VI arc within 500 μs. The peak junction temperature of the GaN MOSFETs in the aircraft application was 97.5 $°C$ for an ambient temperature of 25 $°C$, and the peak junction temperature of the SiC MOSFETs for the shipboard application was 80 $°C$ for the worst case scenario at an ambient temperature of 50 $°C$. Once the fault was interrupted, the peak overvoltage was 9.89 kV for the aircraft application and 62.4 kV for shipboard.

6.1.2 HTS Fault Current Limiter Solid State DC Breaker

The HTS-FCL-SSDCB utilizes an in-series HTS-FCL in order to limit fault currents to a manageable level. Without this component, the fault would be magnitudes larger and require a solid state circuit breaker with many more switching devices. Therefore, the FCL enables a reduction in the number of semiconductive switches

needed. In doing so, the power density is improved over the conventional SSDCB along with efficiency. SiC MOSFETs are used to further increase power density and efficiency. The HTS-FCL naturally limits fault currents and requires no controls. It is superconductive at load currents, so there is no insertion losses and quickly transitions to a significant resistance when a fault occurs. By using both the HTS-FCL and SSDCB, the fault interruption speed is comparable to that of the conventional SSDCB.

The HTS-FCL-SSDCB requires cryogenic cooling in order to maintain the FCL's superconductance. This may add additional weight and reduce power density. Therefore, it would be realistic to implement this breaker concept in a megawatt-scale propulsion system with an already existing cryostat. As well, the WBG switches in the SSDCB must block the full system voltage upon fault interruption. This makes the breaker more susceptible to overvoltages since the switches can be easily damaged due to voltage stress or excessive switching losses. Therefore, the energy dissipation branch is much more critical to consider than with the RCS-HDCB.

Simulation results have been presented that depict the HTS-FCL-SSDCB interrupting a fault in a 20 kV shipboard distribution system. A lumped parameter model is used to estimate the impedance between the source and the fault. A current dependent resistance models the HTS-FCL, and this limited the fault to 7.7 kA. A passive cooling thermal model was utilize along with parameters from the datasheet to model the SiC MOSFETs in the SSDCB. The steady state normal operation mode junction temperature was 54.2 $^{\circ}C$, and the peak at fault interruption was 80.0$^{\circ}C$. The energy dissipation branch was modeled by a linear varistor with a knee voltage 1.2 pu DC bus. After interruption, the overvoltage was clamped to a peak of 31.6 kV.

6.2 Future Work

There is much work to be conducted on the two breaker concepts to further verify their functionality and characterize the performance. The simulation modeling and results have been completed in this thesis for interrupting faults, but hardware prototyping is a necessity to experimentally prove and characterize these conceptual breaker topologies.

6.2.1 Resonant Current Source Hybrid DC Breaker

As discussed in Chapters 2 and 3, the RCS in the RCS-HDCB does not require complicated control schemes. The duty cycle of 50% with the resonant frequency control scheme has the benefit of inherent zero-current switching. However, this does not imply that the breaker cannot benefit from more advanced controls. For instance, new PWM strategies could be used to limit the RCS current to a certain sustained magnitude along with closed loop control. This can be used for arcs that fail to quench after the first current zero. In order to implement this, the switching losses must be carefully considered. Zero-voltage or zero-current switching schemes could also prove beneficial in this case.

Hardware implementation of the RCS-HDCB prototype must be undertaken to corroborate the simulated results. This is important to measure the protection speed, peak junction temperature, controls, and verify the safe clearing of faults. Of particular interest is the timing of the RCS in tandem with the progressive opening of the VI. The work herein assumes an opening speed of 500 μs, and the RCS is timed such that it delivers a zero current at that exact moment. This is because the VI reaches peak voltage isolation capabilities when the contacts are fully open, but it may be

possible to quench the arc inside the VI before this point. Doing so could enable even faster interruption speeds, but may lead to arc restrikes.

Lastly, a MVDC circuit breaker for electrified transportation must have a high reliability. This is especially true for aircraft applications. The operation of the entire vehicle depends on a robust power distribution network. Therefore, lifetime aging acceleration testing must be performed at various temperature and altitude, such that the breaker can be guaranteed to meet the reliability standards.

6.2.2 HTS Fault Current Limiter Solid State DC Breaker

The power law model was explored in this thesis to present its usefulness for modeling the behavior of HTS cables. In future simulations, this model should be utilized for its high fidelity, current dependence, and temperature dependence. However, more parameters must be known about the HTS cable and its cryogenic cooling. The MOV model used in the HTS-FCL-SSDCB fault simulation is a simple linear varistor model. Replacing this with a higher fidelity model would be beneficial for analyzing post-interruption transient overvoltages.

The simulation results must be compared and verified against experimental results. A breaker prototype must be built such that the controls, junction temperature, and the limiting factors for practical fault interruption speed can be verified. It is presumable that the interruption speed of this breaker can be further improved depending on the SiC MOSFETs switching speed and HTS-FCL quenching speed.

On the other hand, to minimize the conduction losses of the breaker, the operation ambient temperature for the SiC MOSFET modules can be further optimized by sharing and controlling the cryogenic temperature designed for the HTS-FCL. For instance, much lower conduction losses may be dissipated if the SiC MOSFET

modules are held around 0 $^{\circ}C$ by smartly using the existing cryostat. This depends on the specific output characteristics and overall performance of the semiconductor modules.

Finally, a circuit breaker with a high reliability is a necessity for MVDC distribution for transportation. The reliability of this design must be modeled and verified against lifetime aging acceleration testing for aviation and marine operating environment.

Bibliography

[1] E. P. Agency, "Fast facts on transportation greenhouse gas emissions," Dec 2021. [Online]. Available: https://www.epa.gov/greenvehicles/fast-facts-transportation-greenhouse-gas-emissions

[2] T. I. E. Agency, "Greenhouse gas emissions from energy data explorer – analysis," Nov 2021. [Online]. Available: https://www.iea.org/articles/greenhouse-gas-emissions-from-energy-data-explorer

[3] X. Ye, A. Savvarisal, A. Tsourdos, D. Zhang, and G. Jason, "Review of hybrid electric powered aircraft, its conceptual design and energy management methodologies," *Chinese Journal of Aeronautics*, vol. 34, no. 4, pp. 432–450, 2021.

[4] A. Tessarolo, S. Castellan, R. Menis, and G. Sulligoi, "Electric generation technologies for all-electric ships with medium-voltage dc power distribution systems," in *2013 IEEE Electric Ship Technologies Symposium (ESTS)*. IEEE, 2013, pp. 275–281.

[5] J. Benzaquen, J. He, and B. Mirafzal, "Toward more electric powertrains in aircraft: Technical challenges and advancements," *CES Transactions on Electrical Machines and Systems*, vol. 5, no. 3, pp. 177–193, 2021.

[6] D. Zhang, J. He, and D. Pan, "A megawatt-scale medium-voltage high-efficiency high power density "sic+si" hybrid three-level anpc inverter for aircraft hybrid-electric propulsion systems," *IEEE Transactions on Industry Applications*, vol. 55, no. 6, pp. 5971–5980, 2019.

[7] J. Woudstra, P. van Willigenburg, B. Groenewald, H. Stokman, S. De Jonge, and S. Willems, "Direct current distribution grids and the road to its full potential," in *2013 Proceedings of the 10th Industrial and Commercial Use of Energy Conference*. IEEE, 2013, pp. 1–7.

[8] Y. Liu, J. Deng, C. Liu, and S. Li, "Energy optimization analysis of the more electric aircraft," in *IOP Conference Series: Earth and Environmental Science*, vol. 113, no. 1. IOP Publishing, 2018, p. 012152.

[9] ABB, "Vision of the fjords," 2016. [Online]. Available: https://new.abb.com/marine/marine-references/vision-of-the-fjords

[10] ——, "Abb technology to support iconic u.s. ferry's move to hybrid-electric operations," Mar 2021. [Online]. Available: https://new.abb.com/news/detail/75390/abb-technology-to-support-iconic-us-ferrys-move-to-hybrid-electric-operations

[11] C. B. Lines, "A vessel with voltage: A look inside our new battery-powered ferry," May 2021. [Online]. Available: https://www.cascobaylines.com/blog/a-vessel-with-voltage-a-look-inside-our-new-battery-powered-ferry/

[12] M. Callavik, A. Blomberg, J. Häfner, and B. Jacobson, "The hybrid hvdc breaker," ABB Grid Systems Technical Paper, Tech. Rep., Nov 2012.

[13] L. Chan, "Dc circuit breaker theory and uses you never know," Aug 2018. [Online]. Available: https://www.linkedin.com/pulse/dc-circuit-breaker-theory-uses-you-never-know-lily-chan

[14] X. Pei, O. Cwikowski, D. S. Vilchis-Rodriguez, M. Barnes, A. C. Smith, and R. Shuttleworth, "A review of technologies for mvdc circuit breakers," in *IECON 2016-42nd Annual Conference of the IEEE Industrial Electronics Society*. IEEE, 2016, pp. 3799–3805.

[15] D. Jovcic and B. Wu, "Fast fault current interruption on high-power dc networks," in *IEEE PES General Meeting*. IEEE, 2010, pp. 1–6.

[16] R. Rodrigues, T. Jiang, Y. Du, P. Cairoli, and H. Zheng, "Solid state circuit breakers for shipboard distribution systems," in *2017 IEEE Electric Ship Technologies Symposium (ESTS)*. IEEE, 2017, pp. 406–413.

[17] P. Cairoli, L. Qi, C. Tschida, V. Ramanan, L. Raciti, and A. Antoniazzi, "High current solid state circuit breaker for dc shipboard power systems," in *2019 IEEE Electric Ship Technologies Symposium (ESTS)*. IEEE, 2019, pp. 468–476.

[18] L. Ängquist, S. Norrga, and T. Modéer, "A new dc breaker with reduced need for semiconductors," in *2016 18th European Conference on Power Electronics and Applications (EPE'16 ECCE Europe)*. IEEE, 2016, pp. 1–9.

[19] T. Arvin, J. He, and N. Weise, "Modeling and simulation of an ultra-fast resonant dc circuit breaker based on current source module," in *2020 IEEE 9th International Power Electronics and Motion Control Conference (IPEMC2020-ECCE Asia)*. IEEE, 2020, pp. 146–153.

[20] ——, "Modeling and simulation of an ultra-fast resonant dc circuit breaker based on current source module," *Transactions on Techniques in STEM Education*, vol. 6, no. 1, pp. 102–112, Oct 2020.

[21] T. Arvin, J. He, N. Weise, and T. Zhao, "Modeling and simulation of a 20kv ultra-fast dc circuit breaker for electric shipboard applications," in *2020 IEEE Transportation Electrification Conference & Expo (ITEC)*. IEEE, 2020, pp. 795–801.

[22] L. Ängquist, S. Nee, T. Modeer, A. Baudoin, S. Norrga, and N. Belda, "Design and test of vsc assisted resonant current (varc) dc circuit breaker," in *15th IET International Conference on AC and DC Power Transmission (ACDC 2019)*. IET, 2019.

[23] J. Ruggles, "Experimental controls method for rcs," Oct 2020, powerpoint slides.

[24] EPC, "Epc 2022-enhancement mode power transistor," 2020.

[25] Cree, "Cas325m12hm2 all-silicon carbide high-performance, half bridge module c2m mosfet and z-rec diode," 2018.

[26] P. G. Slade, "Opening electrical contacts: The transition from the molten metal bridge to the electric arc," *IEICE transactions on electronics*, vol. 93, no. 9, pp. 1380–1386, 2010.

[27] ——, *Electrical contacts: principles and applications*. CRC press, 2017.

[28] M. M. Walter and C. M. Franck, "Optimal test current shape for accurate arc characteristic determination," *IEEE Transactions on Power Delivery*, vol. 29, no. 4, pp. 1798–1805, 2014.

[29] J.-G. Lee, U. A. Khan, H.-Y. Lee, and B.-W. Lee, "Impact of sfcl on the four types of hvdc circuit breakers by simulation," *IEEE Transactions on Applied Superconductivity*, vol. 26, no. 4, pp. 1–6, 2016.

[30] K.-H. Park, I. Kwon, Y.-J. Kwak, and B.-w. Lee, "Evaluation of black-box arc model for dc circuit breaker and comparative analysis of arc characteristic parameters," in *2022 6th International Conference on Electric Power Equipment - Switching Technology (ICEPE-ST)*, 2022, pp. 121–126.

[31] K.-H. Park, H.-Y. Lee, M. Asif, B.-W. Lee, T.-Y. Shin, and C.-W. Gu, "Assessment of various kinds of ac black-box arc models for dc circuit breaker," in *2017 4th international conference on electric power equipment-switching technology (ICEPE-ST)*. IEEE, 2017, pp. 465–469.

[32] S.-W. Lim, U. A. Khan, J.-G. Lee, B.-W. Lee, K.-S. Kim, and C.-W. Gu, "Simulation analysis of dc arc in circuit breaker applying with conventional black box arc model," in *2015 3rd International Conference on Electric Power Equipment–Switching Technology (ICEPE-ST)*. IEEE, 2015, pp. 332–336.

[33] T. Gammon, W.-J. Lee, Z. Zhang, and B. C. Johnson, "A review of commonly used dc arc models," *IEEE Transactions on Industry Applications*, vol. 51, no. 2, pp. 1398–1407, 2015.

[34] L. Ghezzi and A. Balestrero, "Modeling and simulation of low voltage arcs," Ph.D. dissertation, Delft University of Technology, Oct 2010.

[35] J. Andrea, P. Besdel, O. Zirn, and M. Bournat, "The electric arc as a circuit component," in *IECON 2015-41st Annual Conference of the IEEE Industrial Electronics Society*. IEEE, 2015, pp. 003 027–003 034.

[36] S.-W. Lim, U. A. Khan, J.-G. Lee, B.-W. Lee, K.-S. Kim, and C.-W. Gu, "Simulation analysis of dc arc in circuit breaker applying with conventional black box arc model," in *2015 3rd International Conference on Electric Power Equipment–Switching Technology (ICEPE-ST)*. IEEE, 2015, pp. 332–336.

[37] I. Pramudya, M. W. Hadi, J. Koo, B. Lee, U. A. Khan *et al.*, "Modelling of high voltage ac circuit breaker based on circuit breaker's technical data: Using schwarz black box arc model," in *2017 International Conference on High Voltage Engineering and Power Systems (ICHVEPS)*. IEEE, 2017, pp. 83–86.

[38] R. Jones, P. Clifton, G. Grotz, M. Lat, F. Lembo, D. Melvold, D. Nigol, J. Skivtas, A. Sweetana, D. Goodwin *et al.*, "Modeling of metal-oxide surge arresters," *IEEE Transactions on Power Delivery*, vol. 7, no. 1, pp. 302–309, 1992.

[39] A. Meister, R. Shayani, and M. De Oliveira, "Comparison of metal oxide surge arrester models in overvoltage studies," *International Journal of Engineering, Science and Technology*, vol. 3, no. 11, pp. 35–45, 2011.

[40] J. G. Zola, "Simple model of metal oxide varistor for pspice simulation," *IEEE Transactions on computer-aided design of integrated circuits and Systems*, vol. 23, no. 10, pp. 1491–1494, 2004.

[41] C. Mihalache, S. Nitu, and F. Ionescu, "Varistor modeling for power electronics applications simulations," *Journal of optoelectronics and advanced materials*, vol. 10, no. 5, pp. 1272–1276, 2008.

[42] Littlefuse, "Product catalog & design guide varistor metal-oxide varistor (mov)," pp. 11–13, 2017.

[43] ABB, "Surge arrester polim-h..nd," 2013.

[44] Littlefuse, "'metal-oxide varistors (movs) industrial high energy terminal varistors > ba/bb series," 2020.

[45] M. R.-U. Rahman and N. Weise, "Modeling, simulation and hardware implementation of the gan based resonance current source for the ultra-fast mvdc circuit breaker," in *2021 IEEE 8th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*. IEEE, 2021, pp. 220–225.

[46] T. Arvin, J. He, and K. Waters, "Solid-state dc circuit breaker based on hts fault current limiter and sic mosfet modules," 2022, accepted by 2022 IEEE Transportation Electrification Conference & Exp (ITEC).

[47] D. Li and A. Ukil, "Adaptive solid-state circuit breaker without varistors in vsc-interfaced dc system," *IEEE Transactions on Industrial Electronics*, vol. 69, no. 5, pp. 4824–4835, 2022.

[48] Y. Y. Xie, K. Tekletsadik, D. Hazelton, and V. Selvamanickam, "Second generation high-temperature superconducting wires for fault current limiter applications," *IEEE Transactions on Applied Superconductivity*, vol. 17, no. 2, pp. 1981–1985, 2007.

[49] A. Usoskin, A. Rutt, B. Prause, R. Dietrich, and P. Tixador, "Coated conductor based fcl with controllable time response," *IEEE Transactions on Applied Superconductivity*, vol. 17, no. 2, pp. 3475–3478, 2007.

[50] R. Sharifi and H. Heydari, "Electro-thermal modeling and optimization algorithm of resistive superconducting fault current limiters," in *2010 IEEE International Energy Conference*. IEEE, 2010, pp. 814–819.

[51] Microsemi, "Mscsm120am03ct6liag datasheet very low stray inductance phase leg sic mosfet power module," Jan 2020.

[52] B. Hodges, J. Dvorak, and C. Braun, "A fault control system using solid state circuit breakers and high temperature superconducting fault current limiters," in *Proceedings of 1996 International Power Modulator Symposium*. IEEE, 1996, pp. 232–234.

[53] R. Sharifi and H. Heydari, "Optimal design of superconducting fault current limiters for electrical systems," in *2010 Second International Conference on Engineering System Management and Applications*. IEEE, 2010, pp. 1–6.

[54] J. Langston, M. Steurer, S. Woodruff, T. Baldwin, and J. Tang, "A generic real-time computer simulation model for superconducting fault current limiters and its application in system protection studies," *IEEE transactions on applied superconductivity*, vol. 15, no. 2, pp. 2090–2093, 2005.

[55] W. De Sousa, A. Polasek, F. Silva, R. Dias, A. Jurelo, and R. De Andrade, "Simulations and tests of mcp-bscco-2212 superconducting fault current limiters," *IEEE Transactions on Applied Superconductivity*, vol. 22, no. 2, pp. 5 600 106–5 600 106, 2012.

[56] AMSC, "Amperium stainless steel laminated wire type 8612 with double hts layers," 2014.

[57] C. R. Paul, *Introduction to electromagnetic compatibility*. John Wiley & Sons, 2006.

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- T. Arvin, J. He, N. Weise and T. Zhao, "Modeling and Simulation of a 20kV Ultra-Fast DC Circuit Breaker for Electric Shipboard Applications," 2020 IEEE Transportation Electrification Conference & Expo (ITEC), 2020, pp. 795-801.

- M. T. Fard, T. Arvin and J. He, "Improved Short-Circuit Capability with "Si+SiC" Hybrid 5-Level Active NPC Converter for Electric Aircraft Propulsion," 2021 AIAA/IEEE Electric Aircraft Technologies Symposium (EATS), 2021, pp. 1-6.

- T. Arvin, J. He, and K. Waters "Solid-State DC Circuit Breaker Based on HTS Fault Current Limiter and SiC MOSFET Modules," accepted by 2022 IEEE Transportation Electrification Conference & Expo (ITEC), 2022.