10-2-2014

Atomic Layer Deposition of High Quality HfO_2 Using In-Situ Formed Hydrophilic Oxide as an Interfacial Layer

Lei Han
University of Kentucky, lei.han@uky.edu

Jie Pan
University of Kentucky, jie.pan@uky.edu

Qinglin Zhang
University of Kentucky, qinglinzhang@uky.edu

Shibin Li
University of Electronic Science and Technology of China, China, shibinli@uestc.edu.cn

Zhi Chen
University of Kentucky, zhi.chen@uky.edu

Atomic Layer Deposition of High Quality HfO_2 Using In-Situ Formed Hydrophilic Oxide as an Interfacial Layer

Digital Object Identifier (DOI)
https://doi.org/10.1149/2.0041412jss

Notes/Citation Information
Published in *ECS Journal of Solid State Science and Technology*, v. 3, issue 12, p. N155-N160.

Atomic Layer Deposition of High Quality HfO_2 Using In-Situ Formed Hydrophilic Oxide as an Interfacial Layer

Lei Han,[a,*] Jie Pan,[b,*] Qinglin Zhang,[b,*] Shibin Li,[c] and Zhi Chen[a,c,,z]**

[a]*Department of Electrical & Computer Engineering and Center for Nanoscale Science and Engineering, University of Kentucky, Lexington, Kentucky 40506, USA*
[b]*Department of Chemical & Materials Engineering, University of Kentucky, Lexington, Kentucky 40506, USA*
[c]*School of Optoelectronic Information and State Key Lab of Electronic Thin Films and Integrated Devices, University of Electronic Science & Technology of China, Chengdu, Sichuan 610054, People's Republic of China*

High-quality HfO_2 cannot be grown directly on Si substrate using atomic layer deposition (ALD), and an interfacial oxide layer is needed. Traditionally, interfacial oxide layer is formed either in SC1 solution (2 NH_4OH: 4 H_2O_2: 200 H_2O) or by ozonated water spraying. A highly hydrophilic SiO_2 interfacial layer was in-situ formed in the ALD chamber using 1 cycle of ozone and water. The HfO_2 deposited on this interfacial layer showed great growth linearity. The gate leakage current is comparable to that formed using chemical oxide as the interfacial layer. The capacitance-voltage (C-V) curves have negligible frequency dispersion and hysteresis, which suggest high quality in both the interface and electrical properties. The in-situ formation of hydrophilic interfacial layer have advantages over the traditional interfacial layer. This might be useful for formation of interfacial layer on sophisticated 3-D MOS structures such as FinFETs and nanowire FETs. In addition, the chemical oxidation step can be eliminated from the integrated circuits manufacturing processes, which is economically beneficial to the industry.

Manuscript submitted July 22, 2014; revised manuscript received September 19, 2014. Published October 2, 2014.

After a decade of investigation, atomic layer deposition (ALD) of high dielectric constant (high-k) material HfO_2 became the mainstream manufacturing processing in semiconductor industry. This is because the superior quality of HfO_2 films obtained by ALD. ALD provides precise control of film thickness and uniformity at the atomic scale, due to its self-limiting surface reaction. However, not all surfaces are suitable for ALD deposition.

Extensive work has been done to explore the proper interface conditions for ALD of metal oxides. It is widely accepted that non-oxide like Si surface creates barrier for initial cycles of ALD, results in growth incubation period.[1–3] Researchers such as E. P. Gusev, etc. and R. L. Puurunen, etc. explored the ALD nucleation of ZrO_2, Al_2O_3, TiO_2 and HfO_2 on Si surface, and proved that comparing to nucleation on SiO_2 surface, nucleation on H-terminated Si surface is characterized by non-uniformity, island-like morphology, poor metal oxide qualities, and metal diffusion at high temperature.[4–11] Plus, underlying SiO_2 would grow at the Si/metal oxide interface at moderate temperature, which is harmful to the scaling of MOS devices.[12,13] This has been proved by infrared spectroscopy.[14] There are also researches on nucleation of HfO_2 on Si (110) and Si (111),[15] and Ge surface,[16,17] which is a potential substrate material with high mobility. L. Nyns, etc. further explored the initial few cycles of the ALD process on H-terminated, OH-terminated Si surface and different Si orientations.

High-quality HfO_2 can only be grown using ALD on hydrophilic surface, i.e. OH terminated surface. OH termination of Si is crucial for the chemical attachment of metal precursors onto Si surface.[1,18–22] It was found that the density of –OH groups on Si surface has an effect on the atomic surface roughness and dielectric leakage current of HfO_2. Green et al. demonstrated that chemical oxide grown by SC1 solution ($2NH_4OH{:}5H_2O_2{:}200H_2O$) is full of –OH groups and works effectively as an interfacial layer for ALD growth of HfO_2.[23] Ozone based wet chemical oxidation and ozonated water spraying are widely used in industry for ALD growth of HfO_2.[24,25] The growth of the interfacial layer was controlled by ozone concentration in water. However, in 3-D silicon MOS devices structures, such as FinFETs and nanowire FETs, it is difficult to allow uniform oxide formation on the sides of the fins and underneath the nanowire in wet chemical solution or by spraying.

In this work, we report an ALD-based in-situ formation of SiO_2 interfacial layer using one cycle of ozone and water. The interfacial layer formed is highly hydrophilic, and the ALD HfO_2 grown on this interfacial layer has comparable qualities to HfO_2 grown on SC1 chemical oxide. The interfacial layer was in-situ formed in the ALD chamber. This method might be used in sophisticated 3-D MOS structures because ALD allows molecules to be deposited on the surface that cannot be accessible using other methods. In addition, the chemical oxidation step can be eliminated from the integrated circuits manufacturing processes, which is economically beneficial to the industry.

Experimental

Boron doped p type Si(100) wafers with a resistivity of 1–20 Ω cm were used as substrates. The substrates were cleaned using Radio Corporation of America (RCA) cleaning to remove organic and ionic contaminations. H-terminated Si surface was achieved by immersing Si substrates into BOE (buffered oxide etch) solution. BOE etching is preferred to diluted HF etching because Si surface etched by BOE is more smooth. After BOE etching, Si substrate was loaded into ALD chamber (Cambridge Nanotech Inc) immediately at 100°C. Then the surface was exposed to 1 ALD cycle of ozone (O_3) and deionized water (DI H_2O), which were introduced into ALD chamber sequentially with ozone coming first. O_3 was produced from O_2 by an ozone generator (A2Z Ozone Inc.). It was found that after this process, an ultrathin layer of SiO_2 was thermally grown on Si substrate, and the surface of the SiO_2 is highly hydrophilic. Usually Si could not be effectively oxidized by O_2 at temperature below 500°C; O_3 is a strong oxidant, and can grow desired ultrathin oxide layer with only one pulse. The H_2O pulse was supplied to provide –OH groups on the interfacial layer surface. The details of this process are listed as following: O_3 pulse time is 0.3 second, exposure time is 30 seconds, pump time is 23 seconds; H_2O pulse time is 0.5 second, exposure time is 15 seconds, pump time is 20 seconds. The pulse and exposure times of ozone and DI water were carefully chosen to minimize the thickness of the SiO_2 layer, so that the equivalent oxide thickness (EOT) of the gate dielectric stack is minimal. Without taking the sample out of the chamber, HfO_2 was deposited on this interfacial layer using tetrakis(dimethylamino)hafnium (TDMAH) and DI water at 300°C, and the pulse times were chosen to meet the saturation requirement of ALD (TDMAH and H_2O pulse time: 0.5 second. Exposure time: 0 second. Pump time: 5 seconds). It took about 20 minutes to increase

*Electrochemical Society Student Member.
**Electrochemical Society Active Member.
zE-mail: zhi.chen@uky.edu

the chamber temperature from 100°C to 300°C in our ALD system. As a control sample, chemical oxide was also grown using SC1 solution ($NH_4OH:H_2O_2:H_2O = 2:4:200$) at 60°C for 2 minutes, and HfO_2 was deposited using the same parameters as the ones used with the in-situ formed interfacial layer. This component ratio of SC1 solution was developed by M. L. Green, etc.,[23] and was modified in our previous work to be an effective method to grow interfacial layer for ALD of high quality HfO_2.[26] Multi-angle spectroscopic ellipsometry (J. A. Woollam M3000V) was used to measure the physical thickness and characterize the optical properties of the thin films.

MOS capacitors were fabricated to electrically evaluate the effectiveness of the interfacial layer/HfO_2 stacks as gate dielectric materials. Titanium (Ti, 100 Å) and nickel (Ni, 1000 Å) were deposited by electron-beam evaporation as gate metals, because Ti enhances adhesion between the gate metal and the dielectric stacks. The metal gates were patterned by photolithography and wet etching. The gate patterns were circles and the diameter was 100 μm. The back side of the Si substrates was coated by aluminum (1000 Å). The samples were then annealed at 450°C in forming gas ($N_2:H_2 = 10:1$) for 30 minutes to create Ohmic contact between Al and bulk Si. The capacitance-voltage (C-V) curves of the MOS capacitors were measured using an Agilent 4284A LCR meter at multi-frequencies, and the current-voltage (I-V) curves were measured using an Agilent 4155B semiconductor parameter analyzer. Equivalent oxide thickness (EOT) and flatband voltage (V_{FB}) were extracted by fitting the 100 KHz C-V curves with the theoretical quasi-static C-V simulation (UC Berkeley's quantum-mechanical C-V simulator).

Results and Discussion

Characterization of the in-situ formed interfacial layer.— The growth of chemical oxide in SC1 solution has been extensively investigated in our laboratory before.[26] The physical thickness of the ultrathin chemical oxide grown at the condition described above was ~4.5 Å. The chemical oxide thin film was full of –OH groups and highly hydrophilic on the surface. Our in-situ formed SiO_2-based interfacial layer grown by 1 ALD cycle of O_3 and H_2O had similar hydrophilic surface as chemical oxide based on observation. The physical thickness of the in-situ formed interfacial layer was ~3.5 Å measured by spectroscopic ellipsometry, which is ~1 Å thinner than that of the chemical oxide. This is beneficial to further scaling of the gate dielectric stack. Usually H-terminated Si surface would only be oxidized at elevated temperature (>600°C), not at the temperature (100°C) for our in-situ interfacial layer formation process. The H-termination of Si surface could remain for about 10 minutes in air at room temperature. The successful growth of our in-situ interfacial layer is because O_3 is a stronger oxidant than O_2, and the oxygen atoms dissociated from O_3 molecules directly attack the back bonds of Si.[27] The thin oxide film grown by O_3 was also reported with a stable Si-O-Si network even formed at low temperature.[27] The mean square error (MSE) of the spectroscopic ellipsometry measurements of the chemical oxide and the in-situ interfacial layer were comparable. This suggests that the theoretically calculated ideal SiO_2 model fits well with these SiO_2-based interfacial layers. Therefore, the qualities of our newly developed in-situ interfacial layer is not degraded in its oxide properties comparing to the chemical oxide.

The interfacial layers prepared by different methods before depositing HfO_2 were characterized by the Thermo Scientific K-Alpha X-ray Photoelectron Spectrometer (XPS) using an Aluminum Kα micro-focused monochromatic X-ray source with a 400 μm spot size. The depth profile was obtained by an Ar Ion gun of 1000 eV energy with 5 seconds for each layer (the estimated etching speed is 0.5 nm/s for Ta_2O_5).

Figure 1 is the main atomic percentage change of main components (Si and O) of chemical oxide interface and $O_3 + H_2O$ interface from XPS depth profiling (layer1: the bare surface, layer3: the most in-depth layer). In layer 1, the Si and O atomic percentages of the two interfacial layers are similar to each other. The ratio of Si: O is far away from the ideal 1:2 of SiO_2 and the Si amount is much higher. This phenomenon could be attributed to following reasons: (1) the interfacial layers are ultrathin (<5 Å), X-ray could easily penetrate through, and the signal would be affected by the Si substrate. (2) Si substrate cannot be fully oxidized by either the chemical oxidation method or the $O_3 + H_2O$ method. (3) Estimation of atomic percentage by XPS is a rough method, the results could be significantly affected by contamination and equipment limitation. From layer 1 to layer 3, the Si:O ratio increases faster in O_3 and H_2O formed interfacial layer, which is because the O_3 and H_2O formed interfacial layer is thinner than the chemical oxide, so the X-ray arrives the Si substrate sooner.

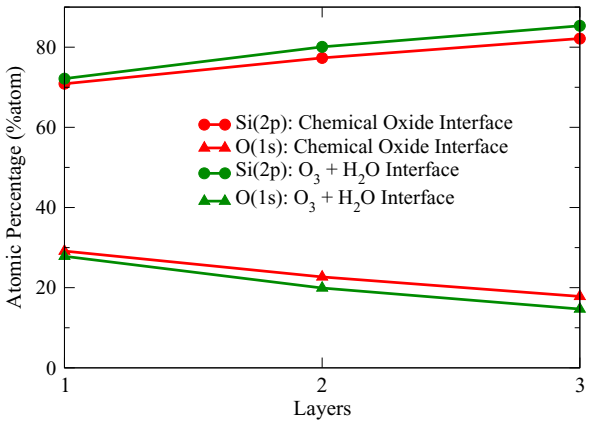

Figure 1. The main atomic percentage change of main components (Si and O) of chemical oxide interface and $O_3 + H_2O$ interface from XPS depth profiling (layer1: the bare surface, layer3: the most in-depth layer).

Figure 2 displays the oxygen 1s spectrum of the surface of interfacial layers from different treatments before depositing HfO_2. Figure 2a is from chemical oxide interface, Figure 2b is from $O_3 + H_2O$ interface, and Figure 2c is from the surface of Si after only one pulse of O_3. Our O-1s spectrum show that the main chemical states of oxygen on the surface are hydroxyl (~531.5 eV),[28] Si-O(~532.5 eV)[28] and H_2O (~534 eV),[29] but their amounts (the area under each peak) on the surfaces vary between different preparation methods.

Comparing chemical oxide (Figure 2a) and $O_3 + H_2O$ (Figure 2b) methods, the amount of –OH group on the surface interface from $O_3 + H_2O$ method (area under –OH peak : area under Si-O peak is 0.24) is smaller than that on the interface from chemical oxide method (area under –OH peak : area under Si-O peak is 0.57). Introducing H_2O in the end of O_3 process is necessary, since the amount of –OH group on the interface from $O_3 + H_2O$ process is increased comparing with O_3 only method (area under –OH peak : area under Si-O peak is 0.17).

Growth linearity of ALD HfO_2 on in-situ formed interfacial layer.— After formation of the interface layer, the substrate temperature was increased to 300°C. During the temperature ramping up, the samples remained in the ALD vacuum chamber, so there was no unwanted SiO_2 re-growth. Therefore, it is an in-situ deposition process. At 300°C, HfO_2 was deposited on the samples by ALD for 15, 21, 24, 35, 50, 100, 150 and 200 cycles. The physical thicknesses were measured using spectroscopic ellipsometry as shown in Figure 3a with square marks. The measurement error is within 3% of the measured thickness. The growth of HfO_2 shows excellent linearity even during the starting cycls, suggesting a stable atomic-layer-by-atomic-layer deposition. The deposition rate of ~1 Å/cycle was extracted by calculating the slope of the straight growth line. MOS capacitors were fabricated using the interfacial layer/HfO_2 stacks as the gate dielectric. The EOTs of the gate dielectric stacks were extracted from the C-V curves measured at high frequency (100 KHz), which were plotted in Figure 3a with triangle marks. Several devices were measured for each number of ALD cycles, and the EOTs have variation <2 Å among all

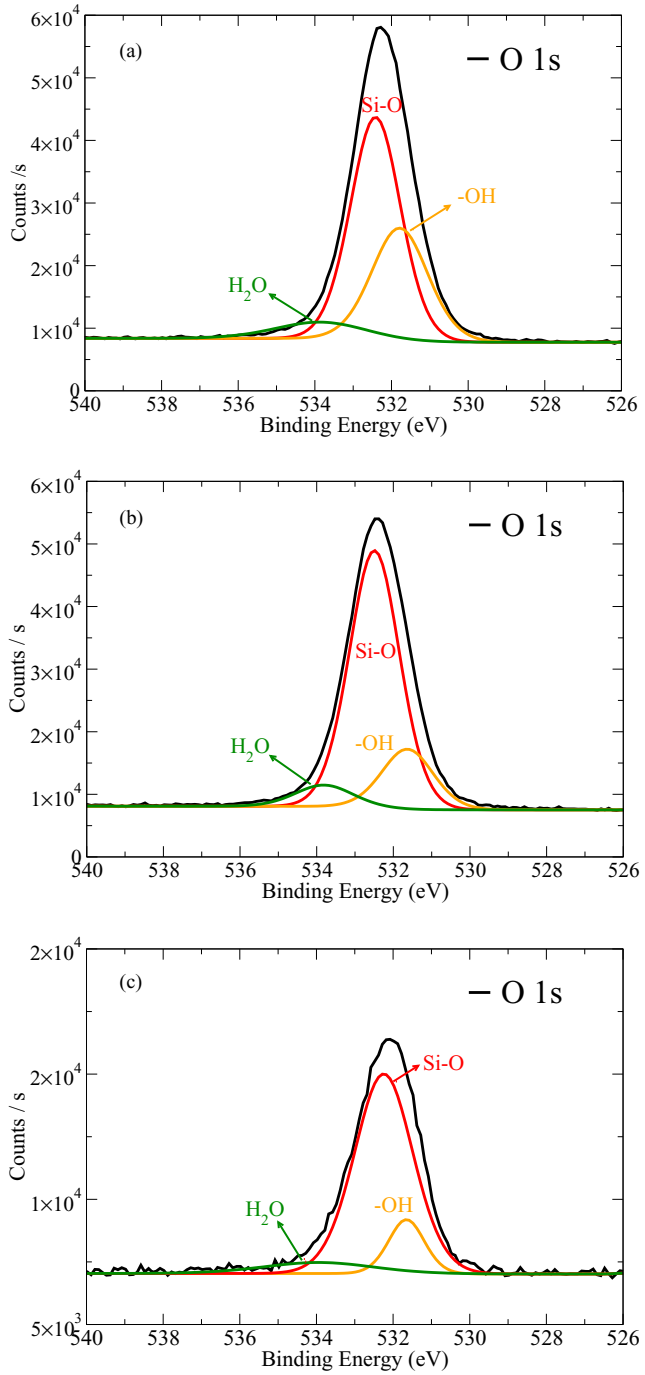

Figure 2. (a)-(c): The oxygen 1s spectra of the interfacial layers from different treatments before depositing HfO_2. (a) Chemical oxide interface. (b) $O_3 + H_2O$ interface. (c) only O_3 grew interface.

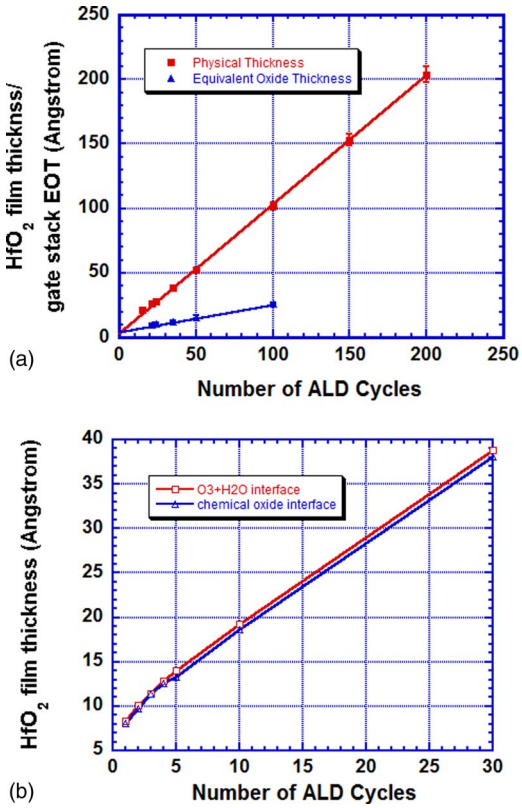

Figure 3. (a) Square: Physical thickness of ALD HfO_2 thin films deposited for 15, 21, 24, 35, 50, 100, 150, and 200 cycles. Triangle: Equivalent Oxide Thickness (EOT) extracted from high-frequency (100 KHz) capacitance-voltage (C-V) curves of the MOS capacitors using the interfacial layer/HfO_2 as the gate stacks. The interfacial layer was grown by 1 ALD cycle of O_3 and DI H_2O at 100°C. Physical thicknesses of the HfO_2 thin films were obtained by spectroscopic ellipsometry. (b) ALD of HfO_2 on chemical oxide interface and $O_3 + H_2O$ interface for 1, 2, 3, 4, 5, 10, and 30 cycles.

the measured devices. The linearity of EOT vs. ALD cycle numbers will be discussed in details later.

Figure 3b shows the physical thickness of HfO_2 deposited for 1, 2, 3, 4, 5, 10 and 30 cycles on chemical oxide interface and $O_3 + H_2O$ interface. During 1-5 cycles, the growth of HfO_2 is not linear. The HfO_2 growth tracks on these two interfacial layers are similar, which implies the $O_3 + H_2O$ interface is as effective as the chemical oxide interface. The measurement error in this thickness range is ~0.5 Å, and the error bar would mix together with the data point mark, so it is not shown in Figure 3b.

Electrical characterization of MOS capacitors.— Figures 4 and 5 are the high frequency (100 KHz) Capacitance density-Voltage (C-V) curves of the MOS capacitors using the in-situ formed interfacial layer/ALD HfO_2 as the gate dielectric stacks. HfO_2 was deposited for 21 cycles on the sample shown in Figure 4, and 24 cycles on the sample shown in Figure 5. In Figure 4, the C-V curve of the MOS capacitor using ALD HfO_2 deposited for 21 cycles on the chemical oxide is also plotted as a reference. The dots are the measurement data (circles are data from the chemical oxide sample and squares are data from the in-situ formed interfacial layer sample), and the solid curves are the theoretical quasi-static C-V simulation that takes quantum effects into consideration. In all the C-V results, the deviation of capacitance density is under 5×10^{-8} F/cm^2. This is too small to be drawn as an error bar, since the error bar would mix together with the data point. The fitting of the simulation to the measurement data is precise in the depletion region and in the initial part of the accumulation region. In the high-voltage part of the accumulation region, the measurement data have deformation and the capacitance value drops. This is because the interfacial layer plus the 21-cycle-ALD HfO_2 stack is ultrathin with its physical thickness of <3 nm, so that the direct tunneling current through the dielectric stack is high, which causes C-V deformation in the high gate voltage region.[30] By fitting the measurement data with simulation, we extracted the flatband voltage (V_{FB}) and the EOT of the capacitors. The physical thicknesses of the HfO_2 thin films are also marked in the Figures. The physical thicknesses of the HfO_2 films on these two samples are 2.59 nm and 2.79 nm, separately, and the corresponding EOTs are 0.86 nm and 0.98 nm. The HfO_2 physical thickness of the in-situ formed interfacial layer sample is

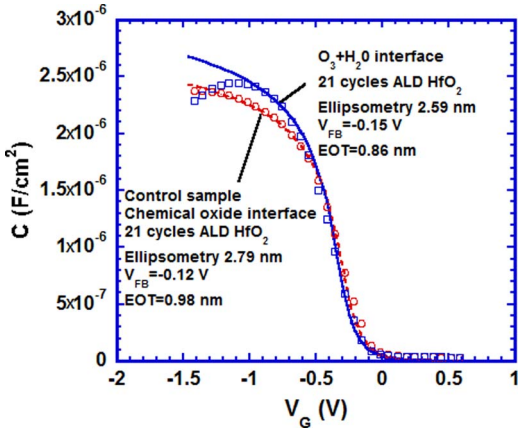

Figure 4. Experimental (dots) and simulated (lines) C-V curves of Ni/Ti/HfO_2/interfacial layer/p-Si MOS capacitors. The experimental C-V curves were measured at 100 KHz. The interfacial layers were grown by SC1 chemical oxidation and 1 ALD cycle of O_3 and DI H_2O at 100°C, separately. The HfO_2 films were deposited for 21 cycles.

2 Å thinner than that of the chemical oxide sample, which was caused by experiment variation. The 2 Å difference in physical thickness corresponds to 0.4 Å difference in EOT, but the EOT of the in-situ interfacial layer sample is 1.2 Å thinner than that of the chemical oxide sample. This extra 0.8 Å less EOT should be attributed to the thinner interfacial layer comparing to chemical oxide.

The C-V curve of the MOS capacitors using the in-situ formed interfacial layer plus the 24- cycle-ALD HfO_2 gate stack is plotted in Figure 5. The physical thickness of HfO_2 on this sample is almost the same as that of the chemical oxide sample, and the EOT is slightly thinner (0.4 Å) than that of the chemical oxide sample. The thickness of interfacial layers is slightly less than 5 Å. The EOTs of the samples in both Figures 4 and 5 suggest that the quality of HfO_2 deposited on the in-situ formed interfacial layer is comparable to that deposited on the chemical oxide.

MOS capacitors were fabricated using samples with 35, 50 and 100 ALD cycles of HfO_2. The samples were analyzed in the same way as described above, and the EOT vs. cycle number is plotted in Figure 3a with the triangle mark. The C-V curves of the capacitors using HfO_2 with cycle numbers of <21 have large deformation in the accumulation region due to large leakage current. The linearity of EOT vs. ALD cycle numbers is excellent, suggesting that it is a true ALD process.

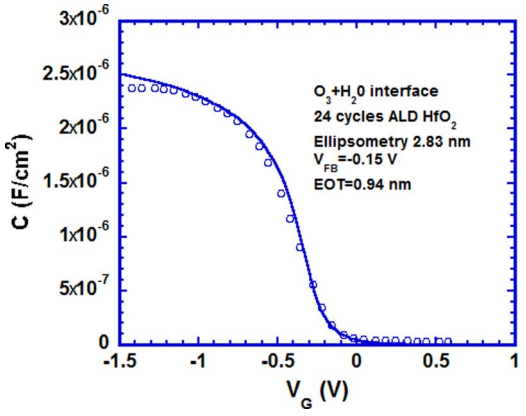

Figure 5. Experimental (dots) and simulated (lines) C-V curves of Ni/Ti/HfO_2/interfacial layer/p-Si MOS capacitors. The interfacial layers were grown by 1 ALD cycle of O_3 and H_2O at 100°C. The HfO_2 were deposited for 24 cycles.

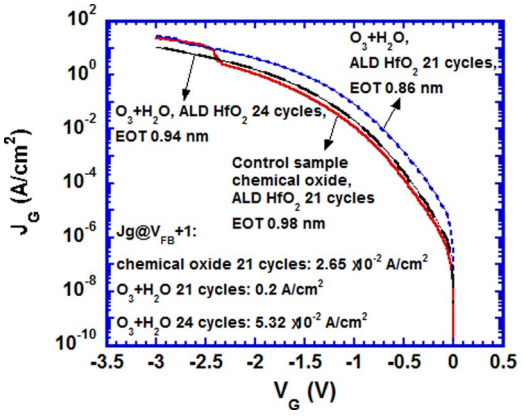

Figure 6. Leakage current density curves of the same MOS capacitors as shown in Figures 2 and 3.

Figure 6 shows the Current density-Voltage (J-V) curves of the capacitors discussed above. The J-V curve of the chemical oxide sample is also plotted as a reference. In all the J-V results, the deviation of the current density is within half order. The uniformity is pretty good among all the measured devices. The gate leakage current is evaluated at $V_G = V_{FB} + 1V$. At this gate voltage, the leakage current of the chemical oxide sample is 2.65×10^{-2} A/cm^2, which matches with the previously reported results.[31,32] The leakage current of the in-situ interfacial layer sample with 21-cycle-ALD HfO_2 is 0.2 A/cm^2, which is 1-order-of-magnitude higher than that of the chemical oxide sample. This is because the EOT of the in-situ interfacial layer sample is 1.2 Å thinner than that of the chemical oxide sample. The physical thickness and EOT of the 24 cycles ALD HfO_2 sample are almost the same as those of the chemical oxide sample, and its gate leakage current is 5.32×10^{-2} A/cm^2, which is also comparable to that of the chemical oxide sample. The gate leakage current of HfO_2 grown by ALD could be affected by the interfacial layer because the initial nucleation is dependent on the interfacial layer. If the interfacial layer is lack of –OH groups, or is not hydrophilic, there are not enough sites on the sample surface for molecules of TDMAH to attach to, so that nucleation is disturbed. In this case, the molecules might be stacked on each other randomly, resulting in HfO_2 films with non-stoichiometry and defects. The gate leakage current of the dielectric stacks using the in-situ formed interfacial layers comparable to that using chemical oxide interfacial layer suggests that this method is useful.

Frequency dispersion and hysteresis of MOS capacitors.— In order to further understand the trap charges in the interface and in the HfO_2 thin film, we carried out measurement of frequency dispersion and hysteresis behaviors of the C-V curves, the results are shown in Figure 7. The chemical oxide/21-cycles-ALD HfO_2 sample was used as a reference, and the in-situ interfacial layer/24-cycle-ALD HfO_2 sample was studied, because the two samples have the same EOT. Figure 7a shows three C-V curves of MOS capacitor on the chemical oxide sample, measured at 10 KHz, 100 KHz and 1 MHz, separately. The three curves overlap with each other in depletion region with the same V_{FB}. The C-V curve in accumulation region at 1 MHz does not match with the curves at 10 kHz and 100 kHz. This phenomenon is not caused by interfacial traps, but by the series resistance of the gate electrode.[33–35] The samples were kept in air for months before we measured the C-V frequency dispersion, and a thin layer of Ni_xO_y would have already formed on the Ni gate surface, which increases the gate series resistance. The C-V curves at 10 kHz and 100 kHz overlapping with each other suggests that there is no frequency dispersion and the interfacial quality is very good. Figure 7b shows the C-V hysteresis behavior of the same capacitor at 100 KHz. The solid curve in the figure was measured from depletion to accumulation, and the dash curve was measured from accumulation to depletion. The two curves overlap with each other and the V_{FB} shift is negligible, suggesting

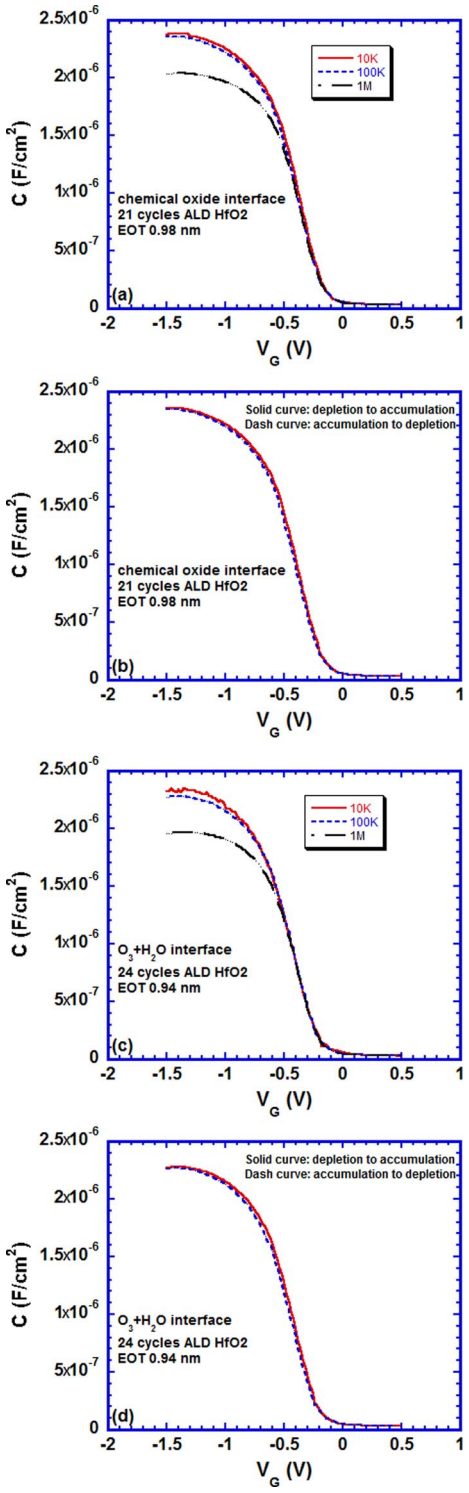

Figure 7. (a) Frequency dispersion (10 KHz, 100 KHz, 1 MHz) of C-V curve of MOS capacitor using chemical oxide/21-cycle-ALD HfO_2 as gate dielectric. (b) Hysteresis behavior of 100 KHz C-V curve of the MOS capacitor in Figure 5a. (c) Frequency dispersion (10 KHz, 100 KHz, 1 MHz) of C-V curve of MOS capacitor using ALD O_3 + H_2O interface/24-cycle-ALD HfO_2 as gate dielectric. (d) Hysteresis behavior of 100 KHz C-V curve of the MOS capacitor in Figure 5c.

the mobile charge in the HfO_2 thin film is small. Figures 7c and 7d are the C-V frequency dispersion and hysteresis behavior of the in-situ interfacial layer/ALD HfO_2 sample. Figures 7c and 7d show C-V curves similar to those in Figures 7a and 7b: the C-V curves measured at different frequencies are all smooth; the C-V curves measured at different frequencies have the same V_{FB}; the hysteresis behavior is negligible. Therefore, we conclude that the ALD in-situ formed interfacial layer provides comparable interfacial quality and dielectric stack quality to that of the chemical oxide interface.

Conclusions

In summary, a highly hydrophilic SiO_2-based interfacial layer was in-situ formed in the ALD chamber using 1 cycle of O_3 and DI H_2O. HfO_2 was deposited on this interfacial layer using a conventional ALD process. Studies of interfacial layer characterization, HfO_2 growth linearity, EOT of the stack, gate leakage current, and frequency dispersion and hysteresis behavior of the C-V curves suggest that the in-situ formed interfacial layer can result in the same high-quality HfO_2 dielectric layers as the chemical oxide interfacial layer. Using this approach, the wet chemical oxidation step can be eliminated from the processes of deposition of high-k gate stacks.

Acknowledgment

This research was supported by University of Kentucky Research Support Grant, and was partially supported by the National Science Fundation EPSCoR Grant 0814194. S.B.L. and Z.C. were also supported by University of Electronic Science & Technology of China.

References

1. Y. Morita, A. Hirano, S. Migita, H. Ota, T. Nabatame, and A. Toriumi, *Applied physics express*, **2**, 011201 (2009).
2. J. C. Hackley, J. D. Demaree, and T. Gougousi, *Journal of Vacuum Science & Technology A*, **26**, 1235 (2008).
3. K. Li, S. Li, N. Li, D. A. Dixon, and T. M. Klein, *The Journal of Physical Chemistry C*, **114**, 14061 (2010).
4. E. Gusev, C. Cabral Jr., M. Copel, C. D'Emic, and M. Gribelyuk, *Microelectronic Engineering*, **69**, 145 (2003).
5. M. Copel, M. Gribelyuk, and E. Gusev, *Applied Physics Letters*, **76**, 436 (2000).
6. E. Gusev, E. Cartier, D. Buchanan, M. Gribelyuk, M. Copel, H. Okorn-Schmidt, and C. D'emic, *Microelectronic Engineering*, **59**, 341 (2001).
7. S. Guha, E. Gusev, H. Okorn-Schmidt, M. Copel, L.-A. Ragnarsson, N. Bojarczuk, and P. Ronsheim, *Applied Physics Letters*, **81**, 2956 (2002).
8. R. L. Puurunen, W. Vandervorst, W. F. Besling, O. Richard, H. Bender, T. Conard, C. Zhao, A. Delabie, M. Caymax, and S. De Gendt, *Journal of applied physics*, **96**, 4878 (2004).
9. P. Kirsch, M. Quevedo-Lopez, H.-J. Li, Y. Senzaki, J. Peterson, S. Song, S. Krishnan, N. Moumen, J. Barnett, and G. Bersuker, *Journal of applied physics*, **99**, 023508 (2006).
10. W. Tsai, R. Carter, H. Nohira, M. Caymax, T. Conard, V. Cosnier, S. DeGendt, M. Heyns, J. Petry, and O. Richard, *Microelectronic Engineering*, **65**, 259 (2003).
11. R. Methaapanon and S. F. Bent, *The Journal of Physical Chemistry C*, **114**, 10498 (2010).
12. M. Copel, E. Cartier, E. Gusev, S. Guha, N. Bojarczuk, and M. Poppeller, *Applied Physics Letters*, **78**, 2670 (2001).
13. E. Gusev, M. Copel, E. Cartier, I. Baumvol, C. Krug, and M. Gribelyuk, *Applied Physics Letters*, **76**, 176 (2000).
14. M.-T. Ho, Y. Wang, R. Brewer, L. Wielunski, Y. Chabal, N. Moumen, and M. Boleslawski, *Applied Physics Letters*, **87**, 133103 (2005).
15. M. Yang, E. P. Gusev, M. Ieong, O. Gluschenkov, D. C. Boyd, K. K. Chan, P. M. Kozlowski, C. P. D'Emic, R. M. Sicina, and P. C. Jamison, *Electron Device Letters, IEEE*, **24**, 339 (2003).
16. E. Gusev, H. Shang, M. Copel, M. Gribelyuk, C. DEmic, P. Kozlowski, and T. Zabel, *Applied physics letters*, **85**, 2334 (2004).
17. A. Delabie, R. L. Puurunen, B. Brijs, M. Caymax, T. Conard, B. Onsia, O. Richard, W. Vandervorst, C. Zhao, and M. M. Heyns, *Journal of applied physics*, **97**, 064104 (2005).
18. K. Kukli, J. Aarik, A. Aidla, H. Siimon, M. Ritala, and M. Leskelä, *Applied surface science*, **112**, 236 (1997).
19. R. L. Puurunen, *Journal of applied physics*, **95**, 4777 (2004).
20. R. L. Puurunen, *Applied surface science*, **245**, 6 (2005).
21. J. C. Hackley, T. Gougousi, and J. D. Demaree, *Journal of Applied Physics*, **102**, 034101 (2007).
22. J. Molina, C. Zuniga, W. Calleja, P. Rosales, A. Torres, and A. Herrera-Gomez, *Journal of Vacuum Science & Technology A*, **31**, 01A132 (2013).
23. M. Green, M.-Y. Ho, B. Busch, G. Wilk, T. Sorsch, T. Conard, B. Brijs, W. Vandervorst, P. Räisänen, and D. Muller, *Journal of Applied Physics*, **92**, 7168 (2002).

24. W. Tsai, L.-A. Ragnarsson, L. Pantisano, P. Chen, B. Onsia, T. Schram, E. Cartier, A. Kerber, E. Young, and M. Caymax, in *Electron Devices Meeting, 2003. IEDM'03 Technical Digest. IEEE International*, p. 13.2. 1 (2003).
25. B. Onsia, M. Caymax, T. Conard, S. De Gendt, F. De Smedt, A. Delabie, C. Gottschalk, M. M. Heyns, M. Green, and S. Lin, *Solid State Phenomena*, **103**, 19 (2005).
26. S. Li, L. Han, and Z. Chen, *Journal of The Electrochemical Society*, **157**, G221 (2010).
27. S. Ichimura, A. Kurokawa, K. Nakamura, H. Itoh, H. Nonaka, and K. Koike, *Thin Solid Films*, **377**, 518 (2000).
28. J. F. Moulder, W. F. Stickle, P. E. Sobol, and K. D. Bomben, *Handbook of X-ray photoelectron spectroscopy*, Perkin Elmer Eden Prairie, MN (1992).
29. E. McCafferty and J. Wightman, *Surface and Interface Analysis*, **26**, 549 (1998).
30. B. Brar, G. Wilk, and A. Seabaugh, *Applied physics letters*, **69**, 2728 (1996).
31. B. H. Lee, L. Kang, R. Nieh, W.-J. Qi, and J. C. Lee, *Applied Physics Letters*, **76**, 1926 (2000).
32. E. Gusev, D. Buchanan, E. Cartier, A. Kumar, D. DiMaria, S. Guha, A. Callegari, S. Zafar, P. Jamison, and D. Neumayer, in *Electron Devices Meeting, 2001. IEDM'01. Technical Digest. International*, p. 20.1. 1 (2001).
33. D. Barlage, R. Arghavani, G. Dewey, M. Doczy, B. Doyle, J. Kavalieros, A. Murthy, B. Roberds, P. Stokley, and R. Chau, in *Electron Devices Meeting, 2001. IEDM'01. Technical Digest. International*, p. 10.6. 1 (2001).
34. D. W. Barlage, J. T. O'Keeffe, J. T. Kavalieros, M. M. Nguyen, and R. S. Chau, *Electron Device Letters, IEEE*, **21**, 454 (2000).
35. J. D. Wiley and G. Miller, *Electron Devices, IEEE Transactions on*, **22**, 265 (1975).